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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

1N4728A SERIES

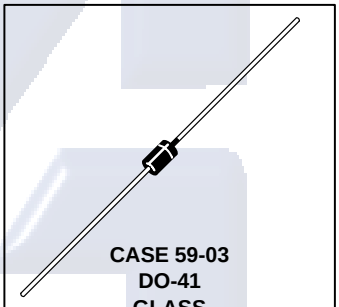
1–1.3 WATT DO-41 GLASS

1–1.3 Watt DO-41 Glass Zener Voltage Regulator Diodes

GENERAL DATA APPLICABLE TO ALL SERIES IN THIS GROUP

One Watt Hermetically Sealed Glass Silicon Zener Diodes

1 WATT
ZENER REGULATOR
DIODES
3.3–100 VOLTS



CASE 59-03
DO-41
GLASS

Specification Features:

- Complete Voltage Range — 3.3 to 100 Volts
- DO-41 Package
- Double Slug Type Construction
- Metallurgically Bonded Construction
- Oxide Passivated Die

Mechanical Characteristics:

CASE: Double slug type, hermetically sealed glass
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 230°C, 1/16″ from case for 10 seconds
FINISH: All external surfaces are corrosion resistant with readily solderable leads
POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode
MOUNTING POSITION: Any
WAFER FAB LOCATION: Phoenix, Arizona
ASSEMBLY/TEST LOCATION: Seoul, Korea

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Power Dissipation @ T_A = 50°C Derate above 50°C	P_D	1 6.67	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +200	°C

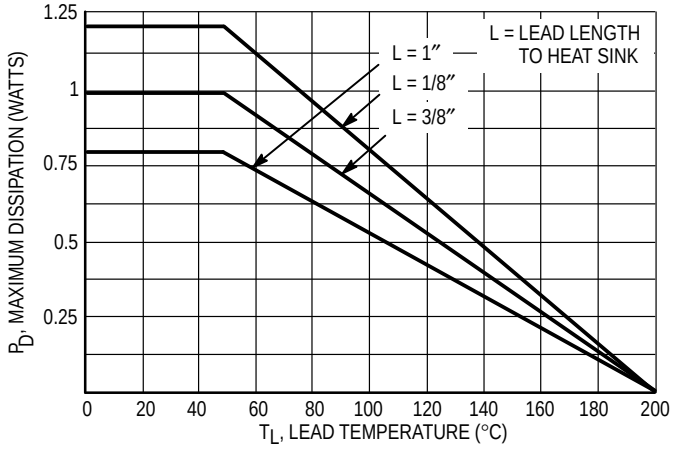


Figure 1. Power Temperature Derating Curve

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GENERAL DATA — 500 mW DO-35 GLASS

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted) V_F = 1.2 V Max, I_F = 200 mA for all types.

JEDEC Type No. (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Notes 2 and 3)	Test Current I_{ZT} mA	Maximum Zener Impedance (Note 4)			Leakage Current		Surge Current @ T_A = 25°C i_r – mA (Note 5)
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} Ohms	I_{ZK} mA	I_R µA Max	V_R Volts	
1N4728A	3.3	76	10	400	1	100	1	1380
1N4729A	3.6	69	10	400	1	100	1	1260
1N4730A	3.9	64	9	400	1	50	1	1190
1N4731A	4.3	58	9	400	1	10	1	1070
1N4732A	4.7	53	8	500	1	10	1	970
1N4733A	***5.1***	***49***	***7***	***550***	***1***	***10***	***1***	***890***
1N4734A	***5.6***	***45***	***5***	***600***	***1***	***10***	***2***	***810***
1N4735A	***6.2***	***41***	***2***	***700***	***1***	***10***	***3***	***730***
1N4736A	***6.8***	***37***	***3.5***	***700***	***1***	***10***	***4***	***660***
1N4737A	7.5	34	4	700	0.5	10	5	605
1N4738A	***8.2***	***31***	***4.5***	***700***	***0.5***	***10***	***6***	***550***
1N4739A	9.1	28	5	700	0.5	10	7	500
1N4740A	***10***	***25***	***7***	***700***	***0.25***	***10***	***7.6***	***454***
1N4741A	***11***	***23***	***8***	***700***	***0.25***	***5***	***8.4***	***414***
1N4742A	***12***	***21***	***9***	***700***	***0.25***	***5***	***9.1***	***380***
1N4743A	13	19	10	700	0.25	5	9.9	344
1N4744A	***15***	***17***	***14***	***700***	***0.25***	***5***	***11.4***	***304***
1N4745A	***16***	***15.5***	***16***	***700***	***0.25***	***5***	***12.2***	***285***
1N4746A	***18***	***14***	***20***	***750***	***0.25***	***5***	***13.7***	***250***
1N4747A	***20***	***12.5***	***22***	***750***	***0.25***	***5***	***15.2***	***225***
1N4748A	***22***	***11.5***	***23***	***750***	***0.25***	***5***	***16.7***	***205***
1N4749A	***24***	***10.5***	***25***	***750***	***0.25***	***5***	***18.2***	***190***
1N4750A	***27***	***9.5***	***35***	***750***	***0.25***	***5***	***20.6***	***170***
1N4751A	***30***	***8.5***	***40***	***1000***	***0.25***	***5***	***22.8***	***150***
1N4752A	***33***	***7.5***	***45***	***1000***	***0.25***	***5***	***25.1***	***135***
1N4753A	36	7	50	1000	0.25	5	27.4	125
1N4754A	39	6.5	60	1000	0.25	5	29.7	115
1N4755A	43	6	70	1500	0.25	5	32.7	110
1N4756A	47	5.5	80	1500	0.25	5	35.8	95
1N4757A	51	5	95	1500	0.25	5	38.8	90
1N4758A	56	4.5	110	2000	0.25	5	42.6	80
1N4759A	62	4	125	2000	0.25	5	47.1	70
1N4760A	68	3.7	150	2000	0.25	5	51.7	65
1N4761A	75	3.3	175	2000	0.25	5	56	60
1N4762A	82	3	200	3000	0.25	5	62.2	55
1N4763A	91	2.8	250	3000	0.25	5	69.2	50
1N4764A	100	2.5	350	3000	0.25	5	76	45

*Indicates JEDEC Registered Data.

NOTE 1. TOLERANCE AND TYPE NUMBER DESIGNATION

The JEDEC type numbers listed have a standard tolerance on the nominal zener voltage of ±5%. C for ±2%, D for ±1%.

NOTE 2. SPECIALS AVAILABLE INCLUDE:

Nominal zener voltages between the voltages shown and tighter voltage tolerances.

For detailed information on price, availability, and delivery, contact your nearest Motorola representative.

NOTE 3. ZENER VOLTAGE (V_Z) MEASUREMENT

Motorola guarantees the zener voltage when measured at 90 seconds while maintaining the lead temperature (T_L) at 30°C ± 1°C, 3/8″ from the diode body.

NOTE 4. ZENER IMPEDANCE (Z_Z) DERIVATION

The zener impedance is derived from the 60 cycle ac voltage, which results when an ac current having an rms value equal to 10% of the dc zener current (I_{ZT} or I_{ZK}) is superimposed on I_{ZT} or I_{ZK}.

NOTE 5. SURGE CURRENT (i_r) NON-REPETITIVE

The rating listed in the electrical characteristics table is maximum peak, non-repetitive, reverse surge current of 1/2 square wave or equivalent sine wave pulse of 1/120 second duration superimposed on the test current, I_{ZT}, per JEDEC registration; however, actual device capability is as described in Figure 5 of the General Data — DO-41 Glass.

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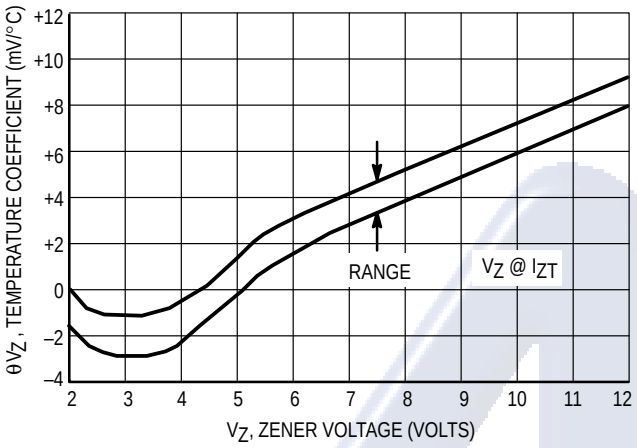
GENERAL DATA — 500 mW DO-35 GLASS

a. Range for Units to 12 Volts



b. Range for Units to 12 to 100 Volts

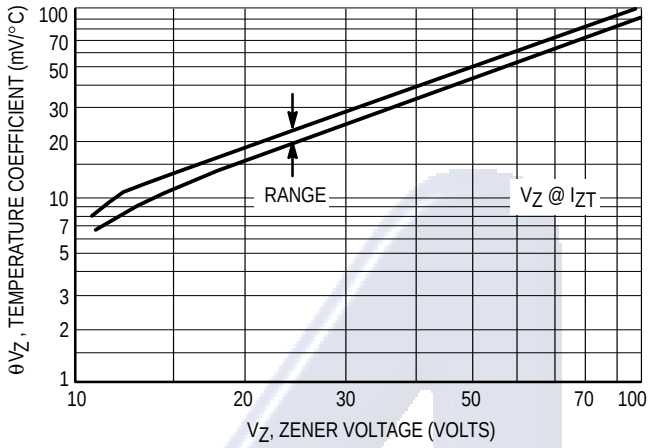


Figure 2. Temperature Coefficients
(–55°C to +150°C temperature range; 90% of the units are in the ranges indicated.)

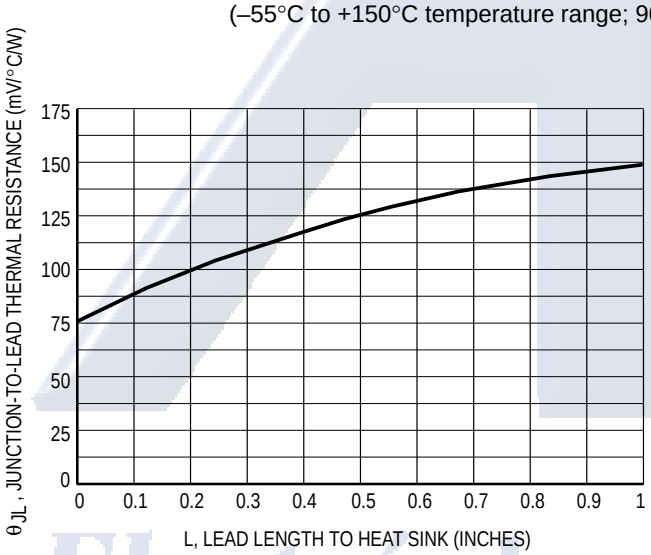


Figure 3. Typical Thermal Resistance versus Lead Length

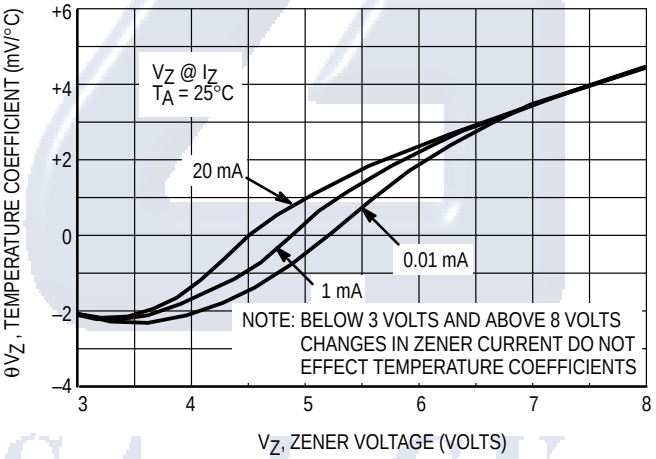
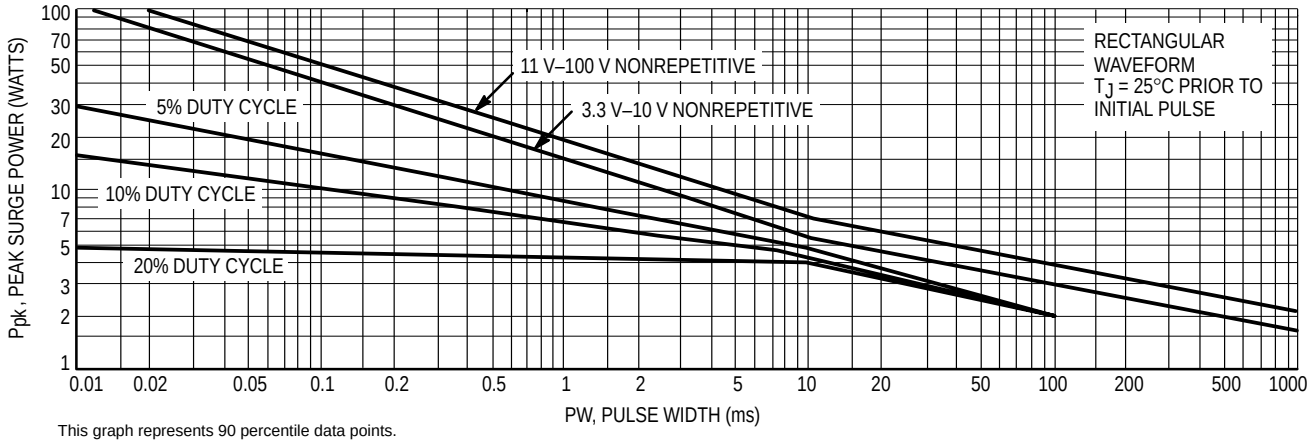


Figure 4. Effect of Zener Current



This graph represents 90 percentile data points.
For worst case design characteristics, multiply surge power by 2/3.

Figure 5. Maximum Surge Power

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GENERAL DATA — 500 mW DO-35 GLASS

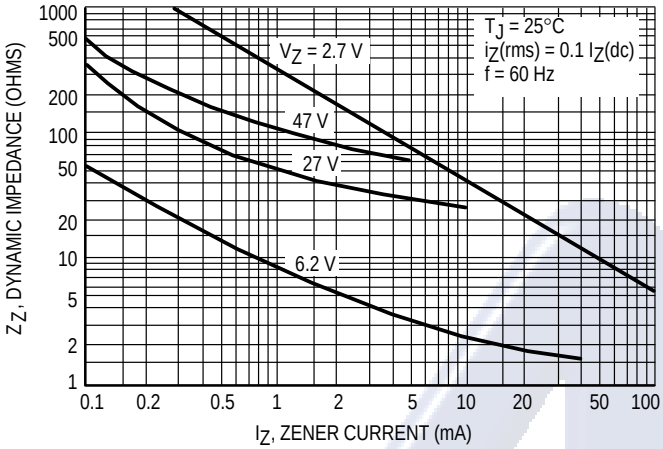

Figure 6. Effect of Zener Current on Zener Impedance

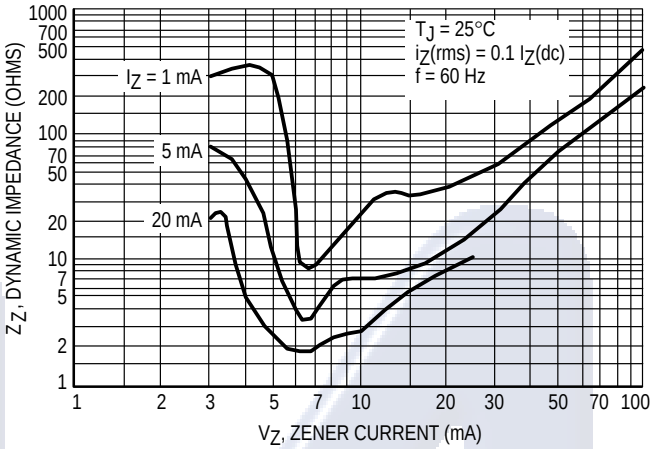

Figure 7. Effect of Zener Voltage on Zener Impedance

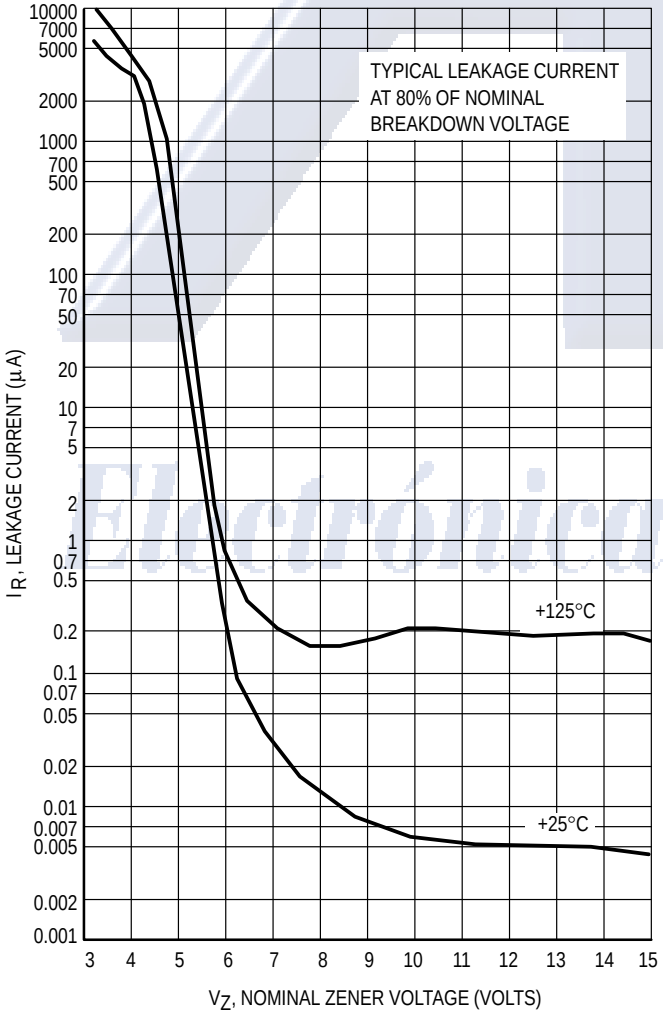

Figure 8. Typical Leakage Current

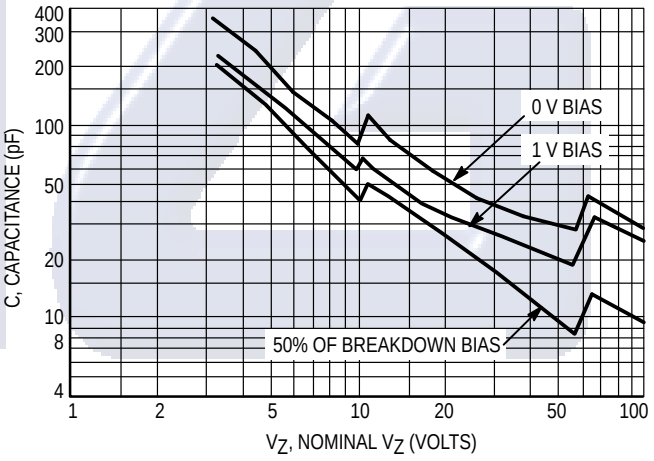

Figure 9. Typical Capacitance versus V_Z

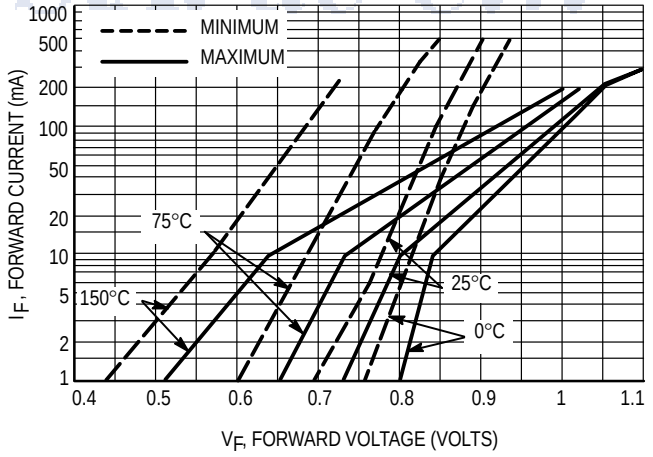

Figure 10. Typical Forward Characteristics

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APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A.$$

θ_{LA} is the lead-to-ambient thermal resistance (°C/W) and P_D is the power dissipation. The value for θ_{LA} will vary and depends on the device mounting method. θ_{LA} is generally 30 to 40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

The temperature of the lead can also be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}.$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found as follows:

$$\Delta T_{JL} = \theta_{JL} P_D.$$

θ_{JL} may be determined from Figure 3 for dc power conditions. For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of $T_J(\Delta T_J)$ may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J.$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figure 2.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Surge limitations are given in Figure 5. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots, resulting in device degradation should the limits of Figure 5 be exceeded.

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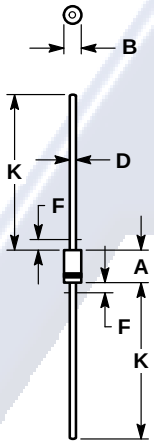
Zener Voltage Regulator Diodes — Axial Leaded

1–1.3 Watt DO-41 Glass



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO-41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN F DIMENSION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.07	5.20	0.160	0.205
B	2.04	2.71	0.080	0.107
D	0.71	0.86	0.028	0.034
F	—	1.27	—	0.050
K	27.94	—	1.100	—

CASE 59-03
DO-41
GLASS

(Refer to Section 10 for Surface Mount, Thermal Data and Footprint Information.)

MULTIPLE PACKAGE QUANTITY (MPQ) REQUIREMENTS

Package Option	Type No. Suffix	MPQ (Units)
Tape and Reel	RL, RL2	6K
Tape and Ammo	TA, TA2	4K

NOTE: 1. The “2” suffix refers to 26 mm tape spacing.

(Refer to Section 10 for more information on Packaging Specifications.)

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