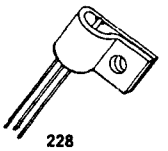
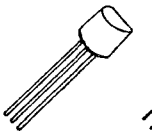
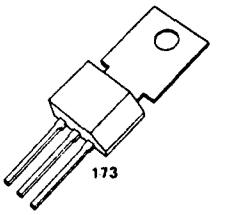


PHASE CONTROL SCR's
.5 TO 5 AMPERES





GE TYPE		C3	C103	C203	C5	C6	C7	–	C106	C107	C108
JEDEC		2N877-81[1]	–	2N5060-64	2N2322-29	–	2N2344-48	2N1595-99, A	–	–	–
ELECTRICAL SPECIFICATIONS											
VOLTAGE RANGE		30-200	30-200	30-400	25-400	25-400	25-200	50-400	15-600	15-600	15-600
FORWARD CONDUCTION											
$I_{T(RMS)}$	Max. RMS on-state current (A)	0.5	0.8	0.8	1.6	1.6	1.6	1.6	4.0	4.0	5.0
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C	0.32 @ 85°C	0.50 @ 25°C	0.50 @ 25°C	1.0 @ 85°C	1.0 @ 85°C	1.0 @ 55°C	1.0 @ 110°C	2.5 @ 30°C	2.5 @ 30°C	3.75 @ 30°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	7	8	8	15	10	15	15	20	15	30
I^2t	Max. I^2t for fusing for > 1.5 msec (A^2 sec)	–	–	–	0.5	0.5	–	0.5	0.5	0.5	1
V_{TM}	Max. peak on-state voltage @ 25°C, 180° conduction, rated $I_{T(AV)}$ (V)	1.6	1.5	1.5	2.2	1.4	2	2	2.2	2.5	1.35
$R_{\theta JC}$	Max. internal thermal resistance, dc junction-to-case (°C/W)	80	125	75	10	10	–	–	10	10	10
I_H	Max. holding current @ 25°C (mA)	5	5	5	2	5	1	–	3	6	3
t_q	Typical turn-off time (μsec) @ max. T_J	15	15	15	40	40	20	40	40	40	40
	Maximum turn-off time (μsec @ 110°C)	–	–	–	–	–	–	–	100	100	100
$t_d + t_r$	Typical turn-on time (μsec @ 110°C)	1	1.4	1.4	1.4	1.4	1.4	1.2	1	1	1
di/dt	Max. rate-of-rise of turned-on current (A/μsec)	–	–	–	50	–	–	–	50	50	50
T_J	Junction operating temperature range (°C)	–65 to 125	–65 to 125	–65 to 125	–65 to 125	–40 to 125	–65 to 100	–65 to 150	–40 to 110	–40 to 110	–40 to 110
BLOCKING											
dv/dt	Typical critical rate-of-rise of off-state voltage, exponential to rated V_{DRM} @ max. rated T_J (V/μsec)	40	20	20	20	20	20	20	8	8	8
FIRING											
I_{GT}	Max. required gate current to trigger (μA) @ –65°C	300	500	500	350	–	75	–	–	–	–
	@ –40°C	–	–	–	–	–	–	–	500	–	500
	@ 25°C	200	200	200	200	1000	20	10,000	200	500	200
V_{GT}	Max. required gate voltage to trigger (V) @ –65°C	–	1	1	1	1	1	–	–	–	–
	@ –40°C	–	–	–	–	1	–	–	1	–	1
	@ 25°C	0.8	0.8	0.8	0.8	0.8	0.8	3	0.8	0.8	0.8
V_{GT}	Min. required gate voltage to trigger (V) @ 110°C	–	–	–	–	–	–	–	0.2	0.2	0.2
	@ 125°C	0.05	0.1	0.1	0.1	0.1	–	–	–	–	–
VOLTAGE TYPES											
Repetitive Peak Forward and Reverse Voltages											
	15	–	–	–	–	–	–	–	C106Q1	C107Q1	C108Q1
	25	–	–	–	2N2322 C5U	C6U	2N2344	–	–	–	–
	30	2N877	C103Y	2N5060 C203Y	–	–	–	–	C106Y1	C107Y1	C108Y1
	50	–	–	–	2N2323* C5F	C6F	2N2345	2N1595, A	C106F1	C107F1	C108F1
	60	2N878	C103YY	2N5061 C203YY	–	–	–	–	–	–	–
	100	2N879	C103A	2N5062 C203A	2N2324* C5A	C6A	2N2346	2N1596, A	C106A1	C107A1	C108A1
	150	2N880	–	2N5063	2N2325 C5G	C6G	2N2347	–	–	–	–
	200	2N881	C103B	2N5064 C203B	2N2326* C5B	C6B	2N2348	2N1597, A	C106B1	C107B1	C108B1
	250	–	–	–	2N2327 C5H	–	–	–	–	–	–
	300	–	–	C203C	2N2328* C5C	C6C	–	2N1598, A	C106C1	C107C1	C108C1
	400	–	–	C203D	2N2329* C5D	C6D	–	2N1599, A	C106D1	C107D1	C108D1
	500	–	–	–	–	–	–	–	C106E1	C107E1	C108E1
	600	–	–	–	–	–	–	–	C106M1	C107M1	C108M1
PACKAGE OUTLINE NO.		112	195.1, 228	263	101	101	101	101	173	173	173

*JAN & JANTX types available.

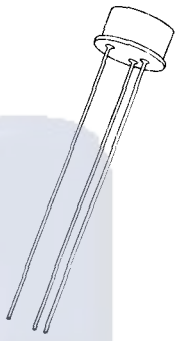
1. 2N885-89 available 20 mA max. I_{GT}.
2. 2N2322A-28A available 20 mA max. I_{GT}.

SCR

2N1595-99

2N929 SEE GES929
2N930 SEE GES930

The 2N1595 series of Silicon Controlled Rectifiers are planar-passivated, all-diffused, three junction, reverse blocking triode thyristors for low power switching and control applications. The 2N2322 series, which is also available, offers additional maximum specified electrical parameters.



- Painted external surface for maximum heat dissipation
- Single-ended package, ideal for printed circuit applications
- All-welded construction
- All-diffused, planar passivated
- Glass-to-metal seals

MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM}(1)	PEAK POSITIVE ANODE VOLTAGE PFV	REPETITIVE PEAK REVERSE VOLTAGE, V_{RRM}
	T_C = −65°C to +125°C		
2N1595	50 Volts*	500 Volts	50 Volts*
2N1596	100 Volts*	500 Volts	100 Volts*
2N1597	200 Volts*	500 Volts	200 Volts*
2N1598	300 Volts*	500 Volts	300 Volts*
2N1599	400 Volts*	500 Volts	400 Volts*

(1) Applies for 1000 ohms maximum, connected gate-to-cathode.

RMS On-State Current, $I_{T(RMS)}$ ..... 1.6 Amperes (all conduction angles)
Average On-State Current, $I_{T(AV)}$ ..... Depends on conduction angle (see Charts 3, 4, 5 and 6)
Peak One-Cycle Surge (Non-rep) On-State Current, I_{TSM} ..... 15 Amperes*
Peak Gate Power Dissipation, P_{GM} ..... 0.1 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 0.01 Watts
Peak Positive Gate Current, I_{GM} ..... 0.1 Amperes
Peak Positive Gate Voltage, V_{GM} ..... 6 Volts
Peak Negative Gate Voltage, V_{GM} ..... −6 Volts
Storage Temperature, T_{STG} ..... −65°C to +150°C*
Operating Temperature, T_J ..... −65°C to +150°C

* Indicates data included in JEDEC type number registration.

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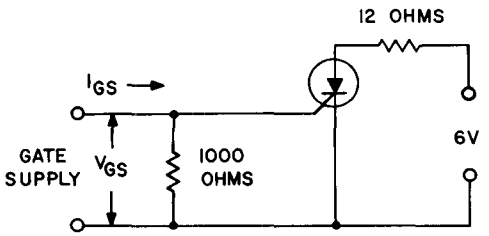
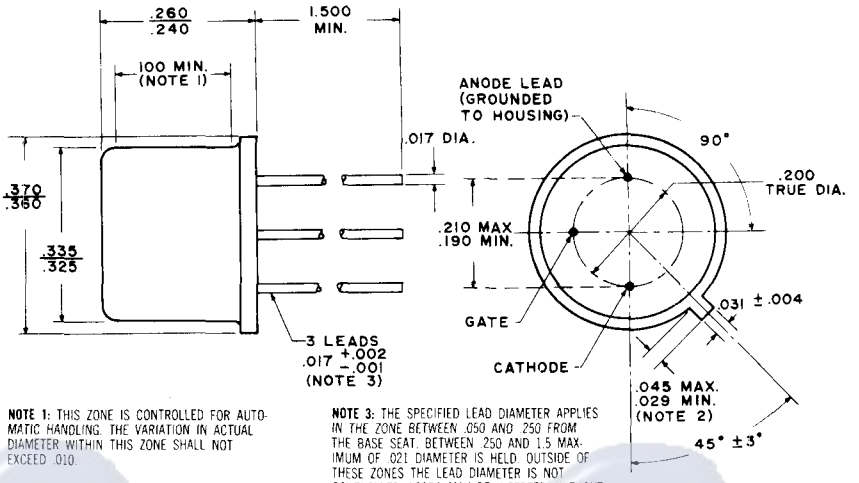
OUTLINE DRAWING
(Conforms to JEDEC TO-5 Package Outline)

2N1595-99





NOTE 1: THIS ZONE IS CONTROLLED FOR AUTOMATIC HANDLING. THE VARIATION IN ACTUAL DIAMETER WITHIN THIS ZONE SHALL NOT EXCEED .010.

NOTE 2: MEASURED FROM MAX. DIAMETER OF THE ACTUAL DEVICE.

NOTE 3: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN .050 AND .250 FROM THE BASE SEAT. BETWEEN .250 AND 1.5 MAXIMUM OF .021 DIAMETER IS HELD. OUTSIDE OF THESE ZONES THE LEAD DIAMETER IS NOT CONTROLLED. LEADS MAY BE INSERTED, WITHOUT DAMAGE, IN .031 HOLES WHILE DEVICE ENTERS .371 HOLE CONCENTRIC WITH LEAD HOLE CIRCLE.

APROX WEIGHT: .05 OZ
ALL DIMENSIONS IN INCHES

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Off-State and Reverse Current	I_{DRM} & I_{RRM}	— —	2.0 100	10 1000*	μA	$V_{DRM} = V_{RRM}$ = Rated volts peak, R_{GK} = 1000 ohms. $T_C = +25°C$ $T_C = +125°C$
D.C. Gate Trigger Current	I_{GS} (1)	—	0.9	10*	mAdc	$T_C = +25°C$, $V_D = 6$ Vdc, $R_L = 12$ ohms
D.C. Gate Trigger Voltage	V_{GT}	—	0.6	3.0*	Vdc	$T_C = +25°C$, $V_D = 6$ Vdc, $R_L = 12$ ohms
Peak On-State Voltage	V_{TM}	—	1.25	2.0*	Volts	$T_C = +25°C$, $I_{TM} = 1.0$ A peak, 1 msec. wide pulse. Duty cycle $\leqq 2\%$.
Holding Current	I_H	—	1.0	—	mAdc	$T_C = +25°C$, Anode Source Voltage = 12 Vdc, $R_{GK} = 1000$ ohms.
Circuit Commutated Turn-Off Time	t_q	—	40	—	μsec	$T_C = +125°C$, $I_{TM} = 1.0$ A peak. Rectangular current pulse, 50 μsec duration. Rate of rise of current < 10A/μsec. Commutation rate $\leqq 5$ A/μsec. Peak reverse voltage = Rated V_{RRM} volts max. Reverse voltage at end of turn-off time interval 15 volts. Repetition rate = 60 pps. Rate of rise of re-applied off-state voltage (dv/dt) = 20 V/μsec. Off-state voltage = Rated V_{DRM} volts. Gate bias during turn-off time interval = 0 volts, 100 ohms.
Turn-On Time	$t_d + t_r$	—	1.2	—	μsec	$T_C = +25°C$, V_D = Rated V_{DRM} value. $I_{TM} = 1.0$ A. Gate trigger pulse = 6 volts, 300 ohms, 5 μsec wide, 0.1 μsec rise time. Gate bias = 0 volts, 300 ohms.

* Indicates data included in JEDEC type number registration.
NOTE: (1) I_{GS} is defined in the circuit below:

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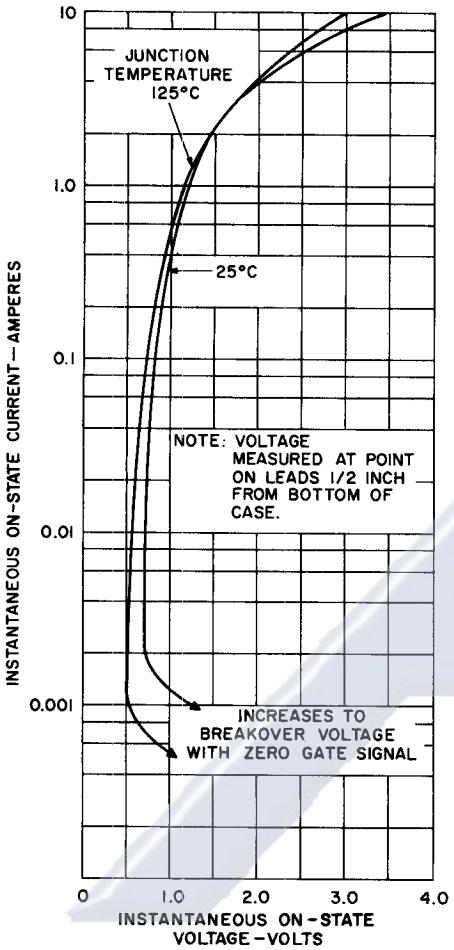
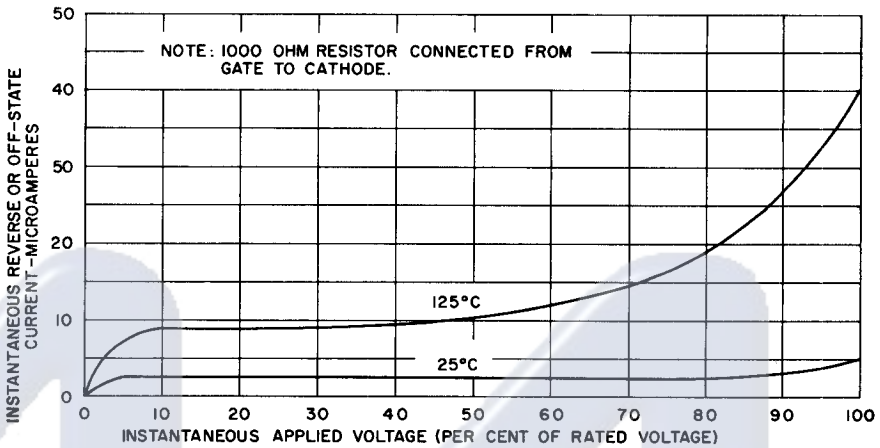
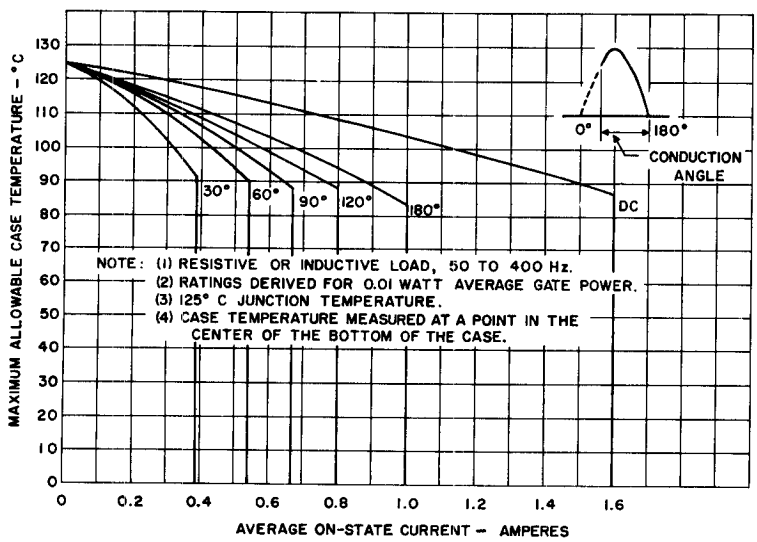


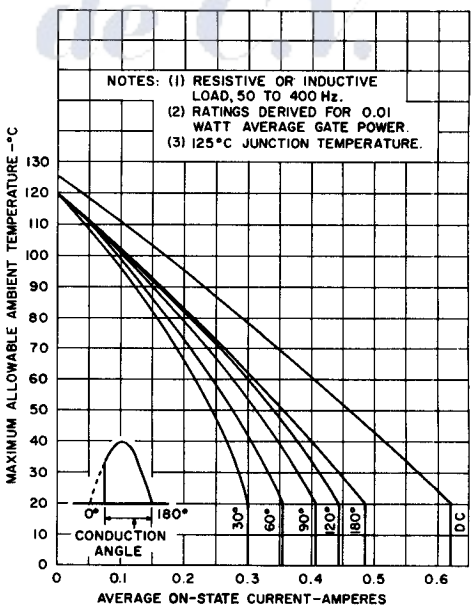
1. TYPICAL ON-STATE CHARACTERISTICS



2. TYPICAL OFF-STATE AND REVERSE BLOCKING CHARACTERISTICS

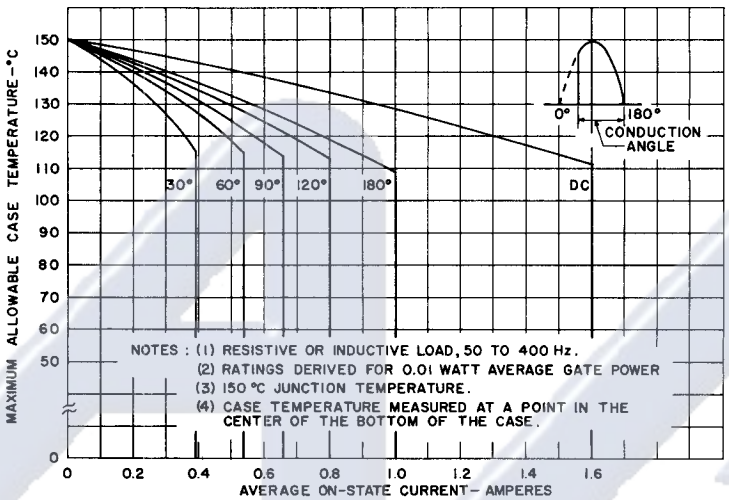


3. MAXIMUM ALLOWABLE CASE TEMPERATURE (150°C Junction Temp.)

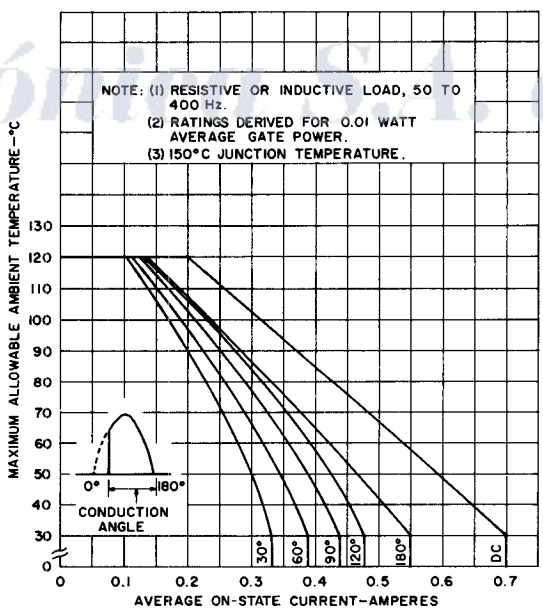


4. MAXIMUM ALLOWABLE AMBIENT TEMPERATURE (125°C Junction Temp.)

Charts 5 and 6 apply to latching applications where SCR need not block off-state voltage after being turned on, since the V_{DRM} specification does not apply above + 125°C junction temperature. SCR will again block rated off-state voltage after junction temperature drops below + 125°C.



5. MAXIMUM ALLOWABLE CASE TEMPERATURE (125°C Junction Temp.)



6. MAXIMUM ALLOWABLE AMBIENT TEMPERATURE (150°C Junction Temp.)