2N5190G, 2N5191G, 2N5192G

Silicon NPN Power Transistors

Silicon NPN power transistors are for use in power amplifier and switching circuits − excellent safe area limits. Complement to PNP 2N5194, 2N5195.

Features

- Epoxy Meets UL 94 V−0 @ 0.125 in.
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N5190G 2N5191G 2N5192G	V_{CEO}	 40 60 80	Vdc
Collector−Base Voltage 2N5190G 2N5191G 2N5192G	V_{CBO}	 40 60 80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	4.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 320	 W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C
ESD − Human Body Model	HBM	3B	V
ESD − Machine Model	MM	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.12	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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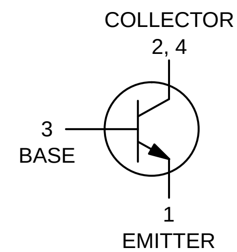
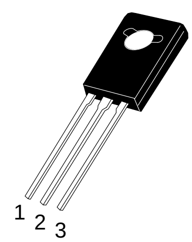
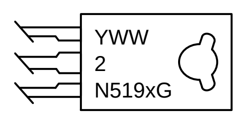
4.0 AMPERES
NPN SILICON
POWER TRANSISTORS
40, 60, 80 VOLTS − 40 WATTS





TO−225
CASE 77−09
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week
2N519x = Device Code
x = 0, 1, or 2
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
2N5190G	TO−225 (Pb−Free)	500 Units/Box
2N5191G	TO−225 (Pb−Free)	500 Units/Box
2N5192G	TO−225 (Pb−Free)	500 Units/Box

ELECTRICAL CHARACTERISTICS* (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 0.1 Adc, I_B = 0)	$V_{CEO(sus)}$			Vdc
2N5190G		40	−	
2N5191G		60	−	
2N5192G		80	−	
Collector Cutoff Current	I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0) 2N5190G		−	1.0	
(V_{CE} = 60 Vdc, I_B = 0) 2N5191G		−	1.0	
(V_{CE} = 80 Vdc, I_B = 0) 2N5192G		−	1.0	
Collector Cutoff Current	I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N5190G		−	0.1	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N5191G		−	0.1	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N5192G		−	0.1	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5190G		−	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5191G		−	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N5192G		−	2.0	
Collector Cutoff Current	I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0) 2N5190G		−	0.1	
(V_{CB} = 60 Vdc, I_E = 0) 2N5191G		−	0.1	
(V_{CB} = 80 Vdc, I_E = 0) 2N5192G		−	0.1	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	1.0	mAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain	h_{FE}			−
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc) 2N5190G/2N5191G		25	100	
2N5192G		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) 2N5190G/2N5191G		10	−	
2N5192G		7.0	−	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)		−	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)		−	1.4	
Base−Emitter On Voltage (I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	−	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	−	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*JEDEC Registered Data.
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

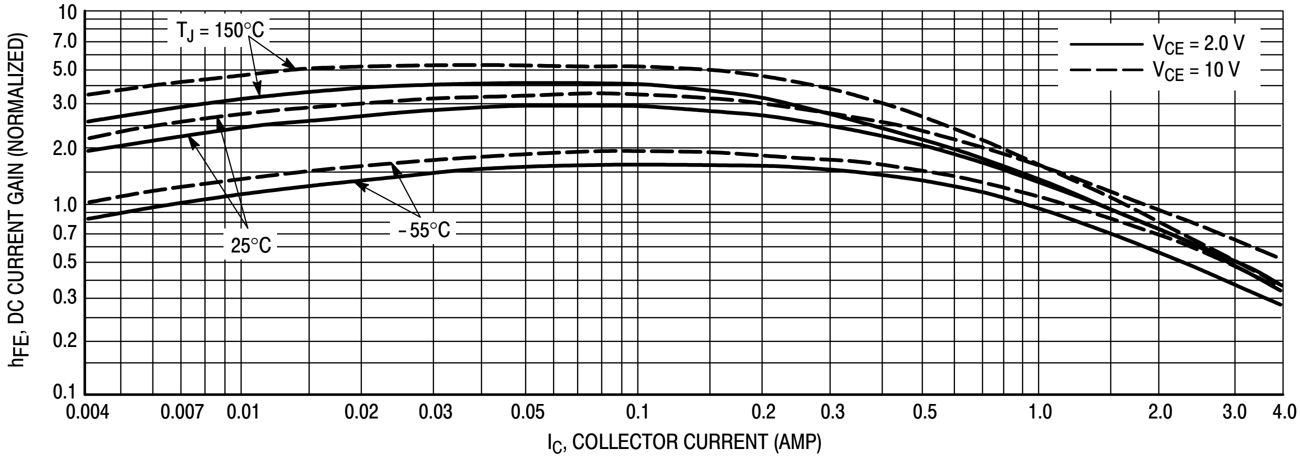


Figure 1. DC Current Gain

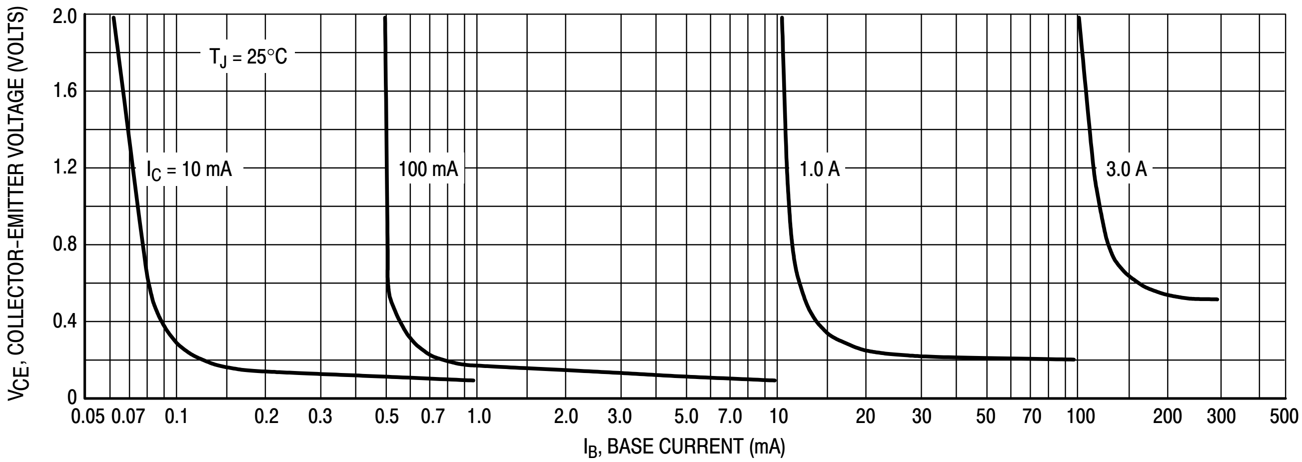


Figure 2. Collector Saturation Region

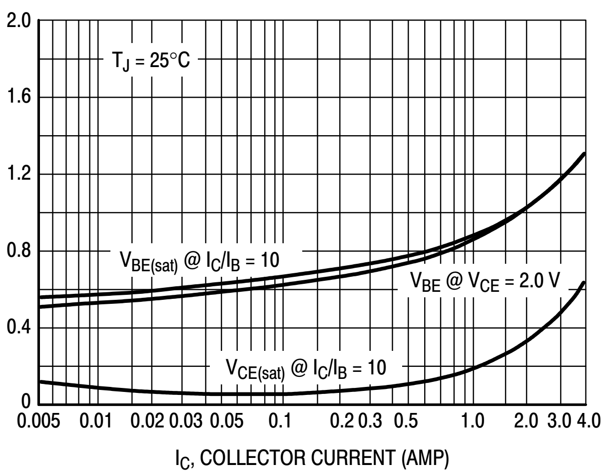


Figure 3. "On" Voltages

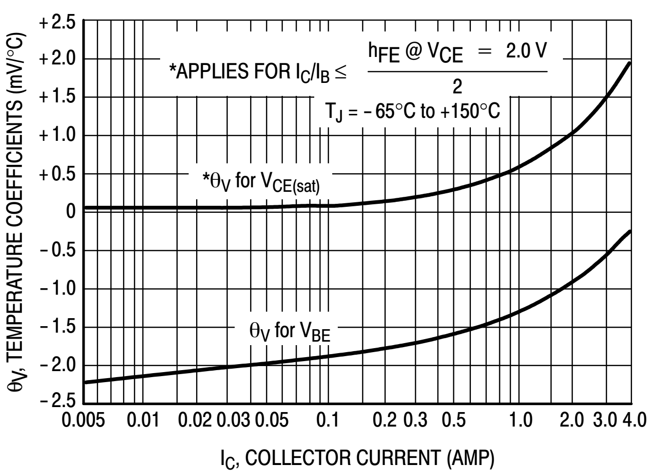


Figure 4. Temperature Coefficients

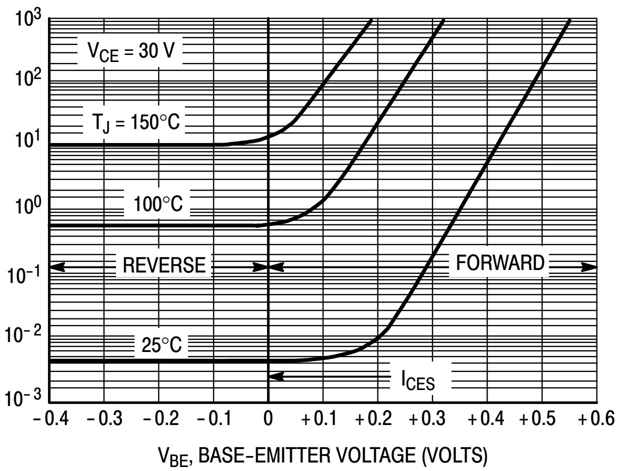


Figure 5. Collector Cut−Off Region

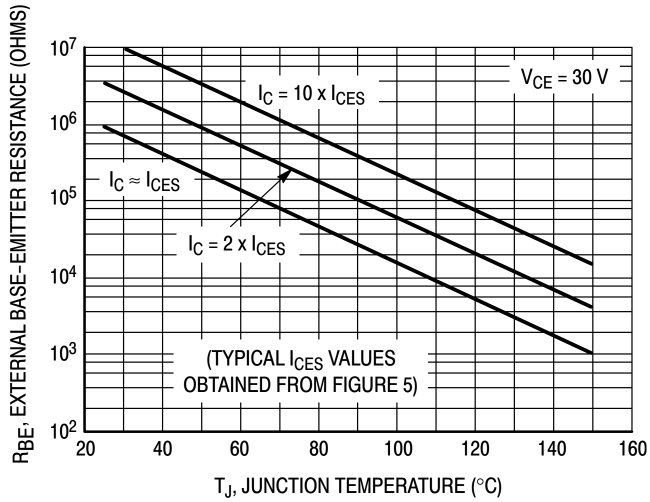


Figure 6. Effects of Base−Emitter Resistance

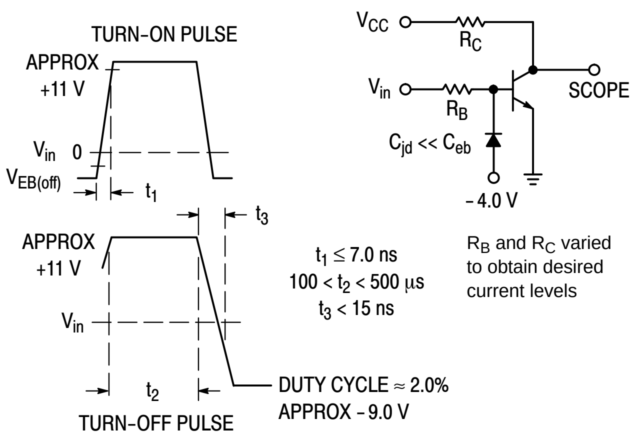


Figure 7. Switching Time Equivalent Test Circuit

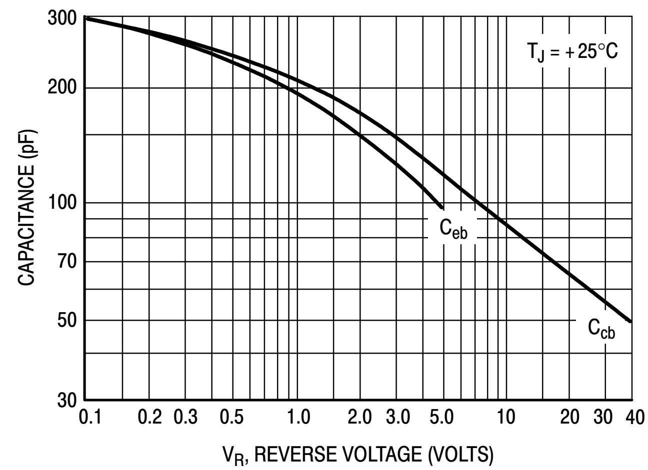


Figure 8. Capacitance

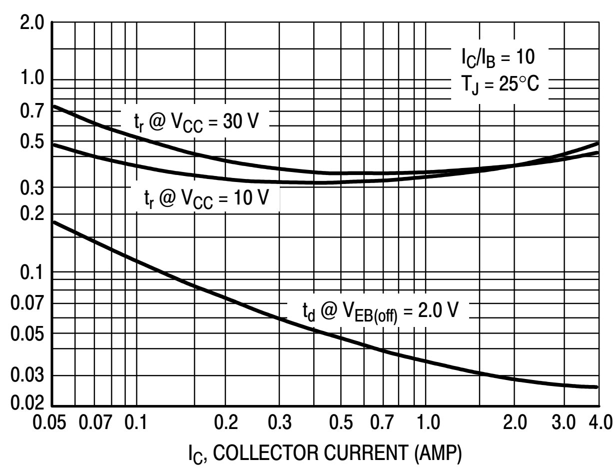


Figure 9. Turn−On Time

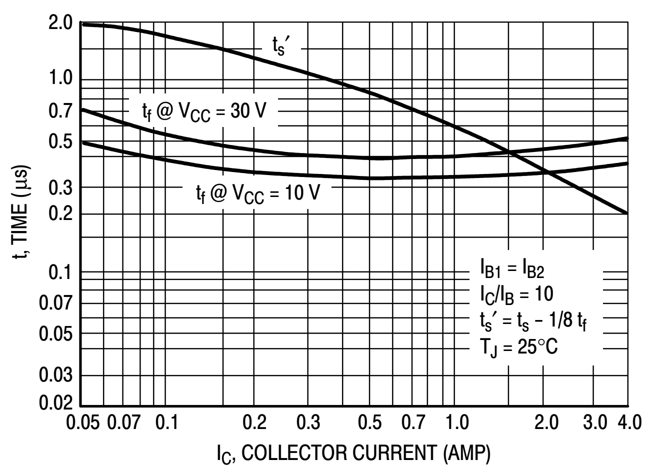


Figure 10. Turn−Off Time

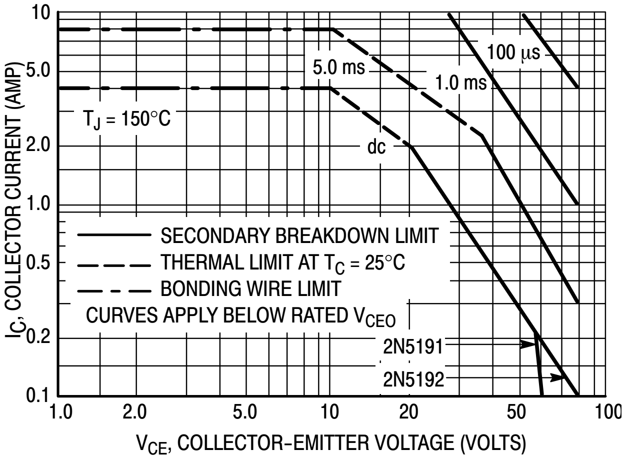


Figure 11. Rating and Thermal Data Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

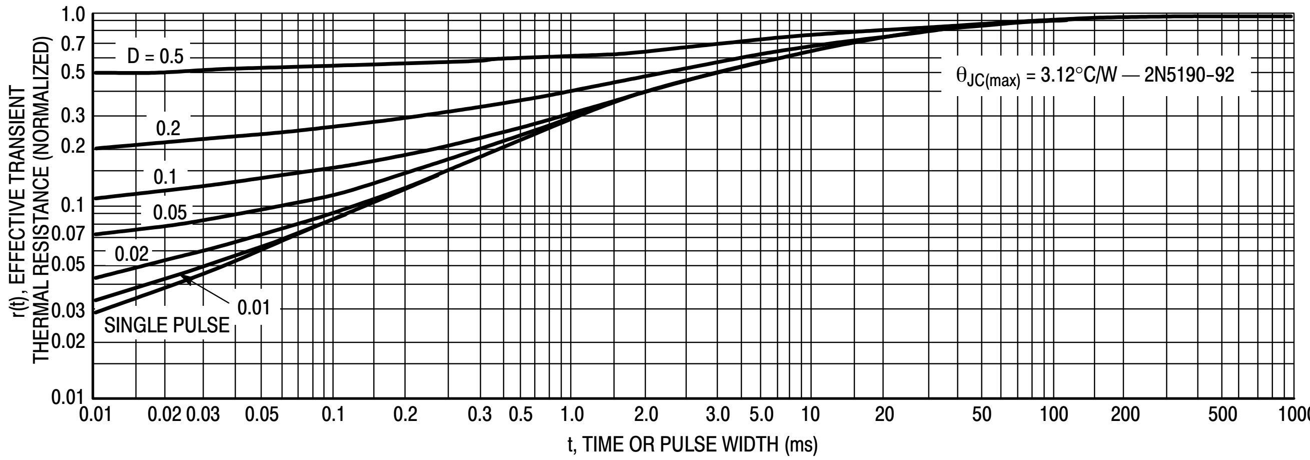


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

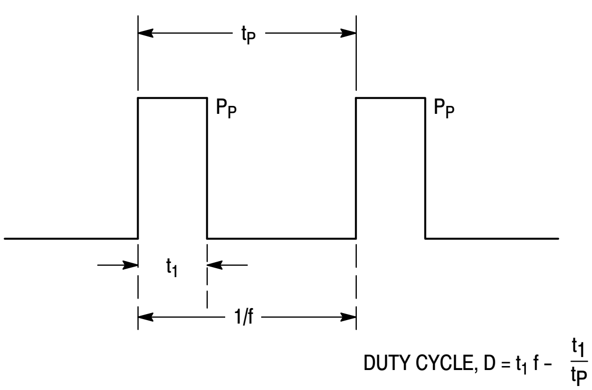


Figure A

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

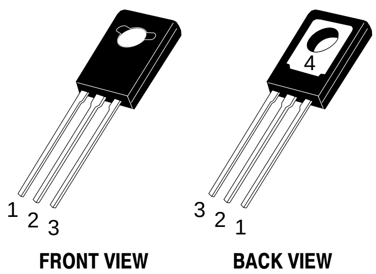
The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

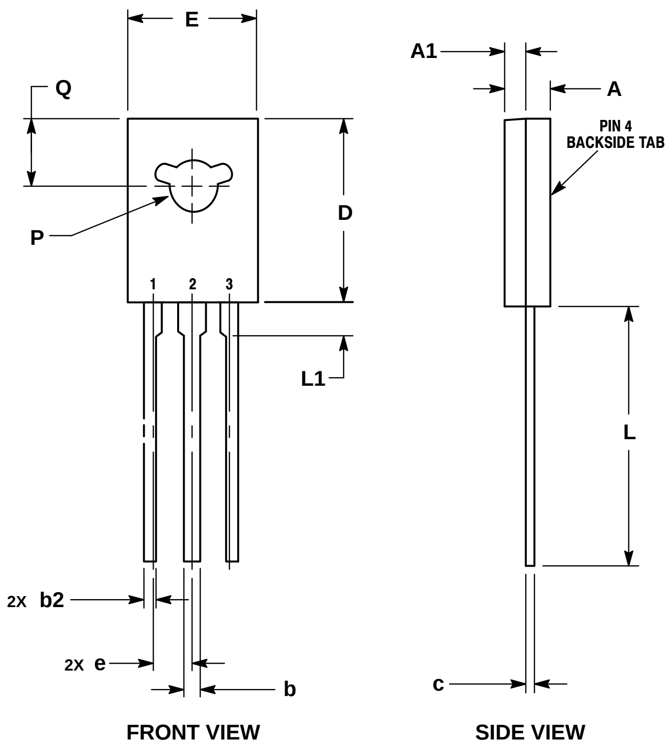
The peak rise in function temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

PACKAGE DIMENSIONS



TO−225
CASE 77−09
ISSUE AC



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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