

# 2N6284 (NPN); 2N6286, 2N6287 (PNP)

Preferred Device

## Darlington Complementary Silicon Power Transistors

These packages are designed for general-purpose amplifier and low-frequency switching applications.

### Features

- High DC Current Gain @  $I_C = 10 \text{ Adc}$  –  
 $h_{FE} = 2400 \text{ (Typ)} - 2N6284$   
 $= 4000 \text{ (Typ)} - 2N6287$
- Collector–Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)}$
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- Pb–Free Packages are Available\*

### MAXIMUM RATINGS (Note 1)

| Rating  | Symbol         | Value        | Unit      |
|---|----------------|--------------|-----------|
| Collector–Emitter Voltage   | $V_{CEO}$      | 80<br>100    | Vdc       |
| Collector–Base Voltage  | $V_{CB}$       | 80<br>100    | Vdc       |
| Emitter–Base Voltage  | $V_{EB}$       | 5.0          | Vdc       |
| Collector Current – Continuous<br>Peak  | $I_C$          | 20<br>40     | Adc       |
| Base Current  | $I_B$          | 0.5          | Adc       |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 160<br>0.915 | W<br>W/°C |
| Operating and Storage Temperature<br>Range  | $T_J, T_{stg}$ | –65 to +200  | °C        |

### THERMAL CHARACTERISTICS (Note 1)

| Characteristic                       | Symbol          | Max  | Unit |
|--------------------------------------|-----------------|------|------|
| Thermal Resistance, Junction–to–Case | $R_{\theta JC}$ | 1.09 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

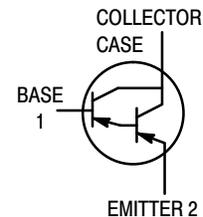
\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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## 20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 100 VOLTS, 160 WATTS



TO–204AA (TO–3)  
CASE 1–07  
STYLE 1

### MARKING DIAGRAM

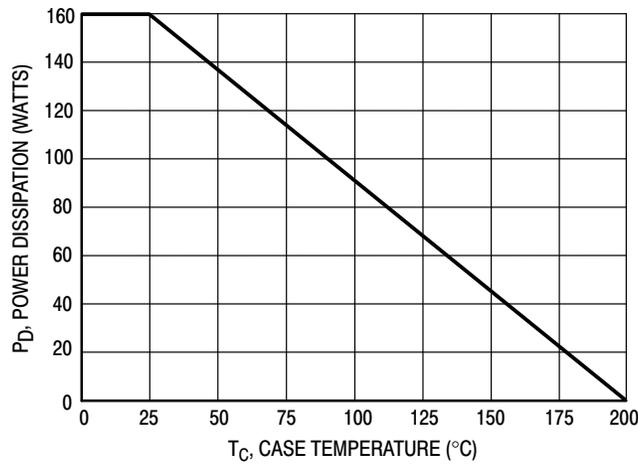


2N628x = Device Code  
x = 4, 6 or 7  
G = Pb–Free Package  
A = Location Code  
YY = Year  
WW = Work Week  
MEX = Country of Origin

### ORDERING INFORMATION

| Device  | Package           | Shipping       |
|---------|-------------------|----------------|
| 2N6284  | TO–3              | 100 Units/Tray |
| 2N6284G | TO–3<br>(Pb–Free) | 100 Units/Tray |
| 2N6286  | TO–3              | 100 Units/Tray |
| 2N6286G | TO–3<br>(Pb–Free) | 100 Units/Tray |
| 2N6287  | TO–3              | 100 Units/Tray |
| 2N6287G | TO–3<br>(Pb–Free) | 100 Units/Tray |

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**Figure 1. Power Derating**

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted) (Note 2)

| Characteristic   | Symbol                | Min | Max | Unit |
|--|-----------------------|-----|-----|------|
| <b>OFF CHARACTERISTICS</b>   |                       |     |     |      |
| Collector–Emitter Sustaining Voltage<br>(I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)   | V <sub>CEO(sus)</sub> | 80  | –   | Vdc  |
| 2N6286<br>2N6284, 2N6287   |                       | 100 | –   |      |
| Collector Cutoff Current<br>(V <sub>CE</sub> = 40 Vdc, I <sub>B</sub> = 0)<br>(V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0)   | I <sub>CEO</sub>      | –   | 1.0 | mAdc |
|  |                       | –   | 1.0 |      |
| Collector Cutoff Current<br>(V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc)<br>(V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C) | I <sub>CEX</sub>      | –   | 0.5 | mAdc |
|  |                       | –   | 5.0 |      |
| Emitter Cutoff Current<br>(V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)  | I <sub>EBO</sub>      | –   | 2.0 | mAdc |

### ON CHARACTERISTICS (Note 3)

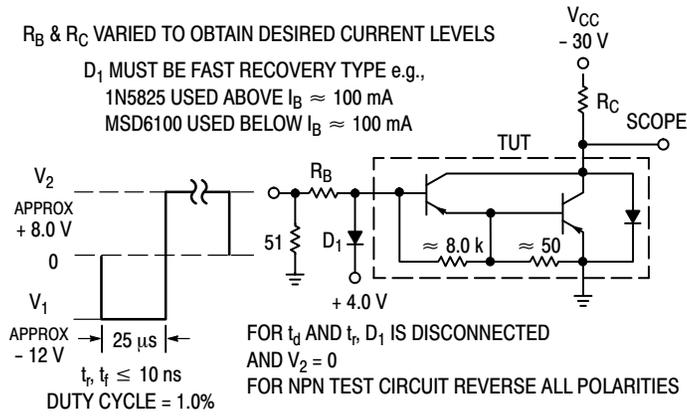
|   |                      |     |        |     |
|---|----------------------|-----|--------|-----|
| DC Current Gain<br>(I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc)<br>(I <sub>C</sub> = 20 Adc, V <sub>CE</sub> = 3.0 Vdc)                     | h <sub>FE</sub>      | 750 | 18,000 | –   |
|   |                      | 100 | –      |     |
| Collector–Emitter Saturation Voltage<br>(I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 40 mAdc)<br>(I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 200 mAdc) | V <sub>CE(sat)</sub> | –   | 2.0    | Vdc |
|   |                      | –   | 3.0    |     |
| Base–Emitter On Voltage<br>(I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc)   | V <sub>BE(on)</sub>  | –   | 2.8    | Vdc |
| Base–Emitter Saturation Voltage<br>(I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 200 mAdc)   | V <sub>BE(sat)</sub> | –   | 4.0    | Vdc |

### DYNAMIC CHARACTERISTICS

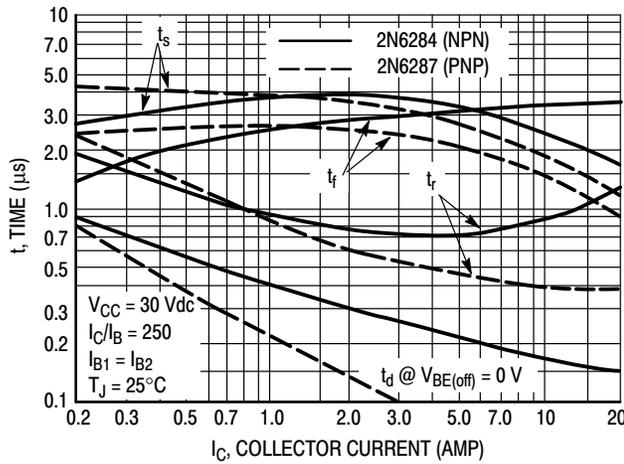
|  |                 |     |     |     |
|--|-----------------|-----|-----|-----|
| Magnitude of Common Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio<br>(I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz) | h <sub>fe</sub> | 4.0 | –   | MHz |
| Output Capacitance<br>(V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)  | C <sub>ob</sub> | –   | 400 | pF  |
|  |                 | –   | 600 |     |
| Small–Signal Current Gain<br>(I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)   | h <sub>fe</sub> | 300 | –   | –   |

2. Indicates JEDEC Registered Data.  
 3. Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

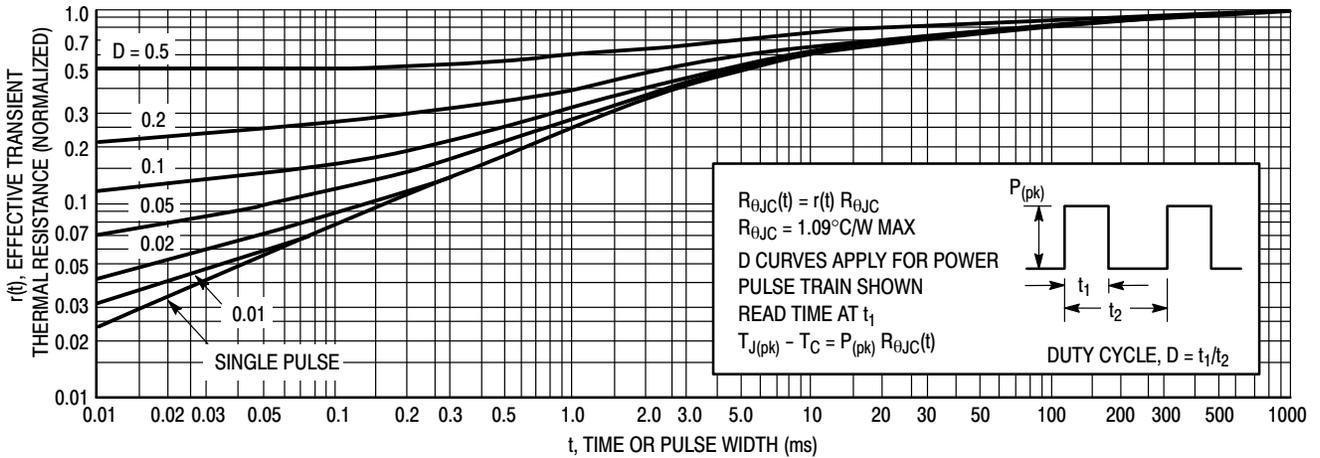
## 2N6284 (NPN); 2N6286, 2N6287 (PNP)



**Figure 2. Switching Times Test Circuit**



**Figure 3. Switching Times**



**Figure 4. Thermal Response**

## 2N6284 (NPN); 2N6286, 2N6287 (PNP)

### ACTIVE-REGION SAFE OPERATING AREA

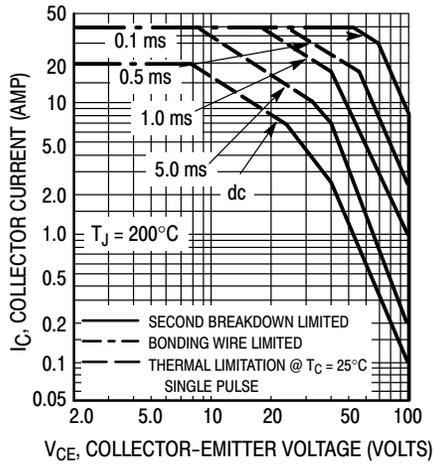


Figure 5. 2N6284, 2N6287

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

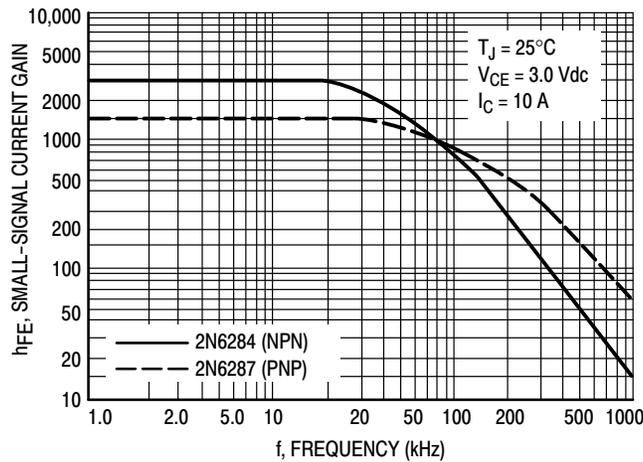


Figure 6. Small-Signal Current Gain

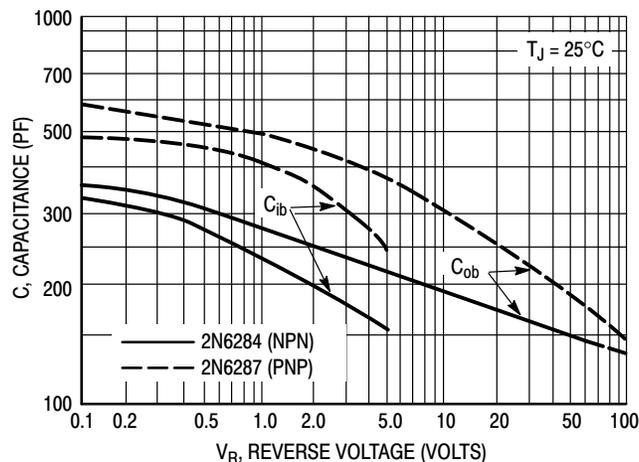


Figure 7. Capacitance

# 2N6284 (NPN); 2N6286, 2N6287 (PNP)

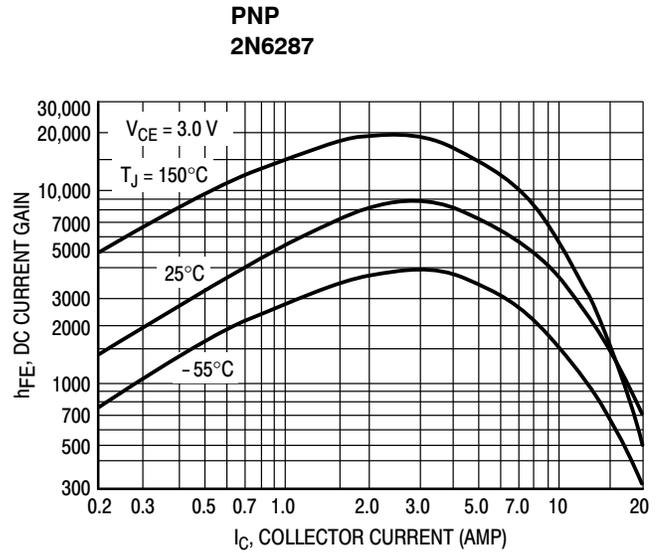
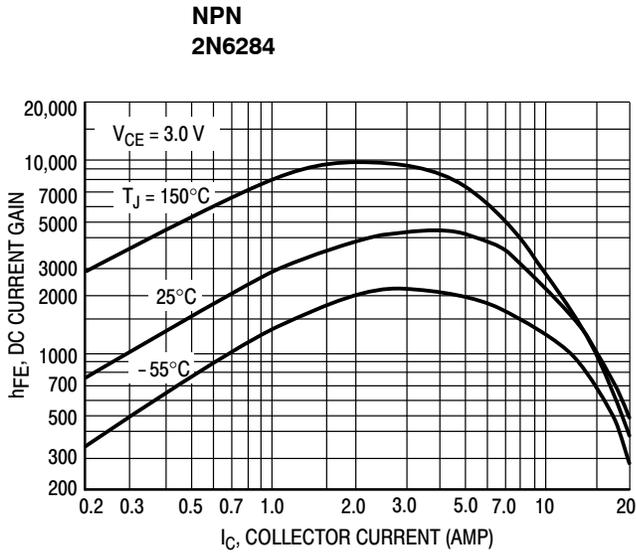


Figure 8. DC Current Gain

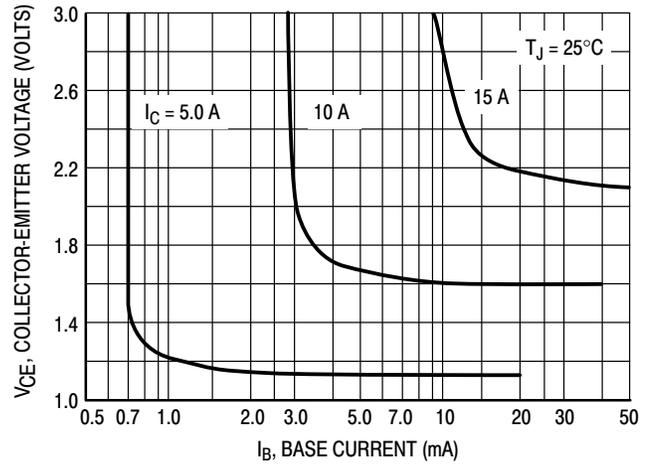
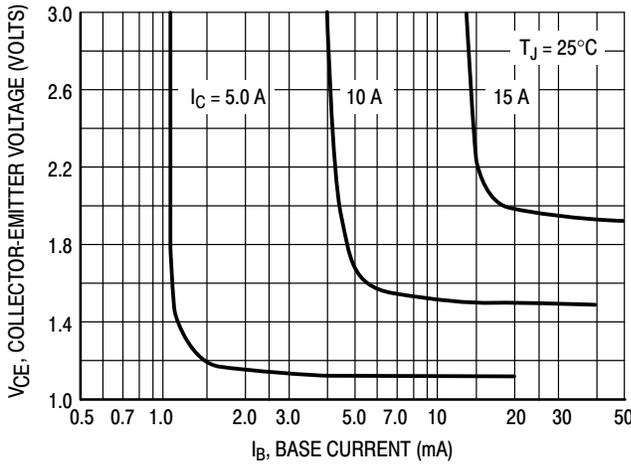


Figure 9. Collector Saturation Region

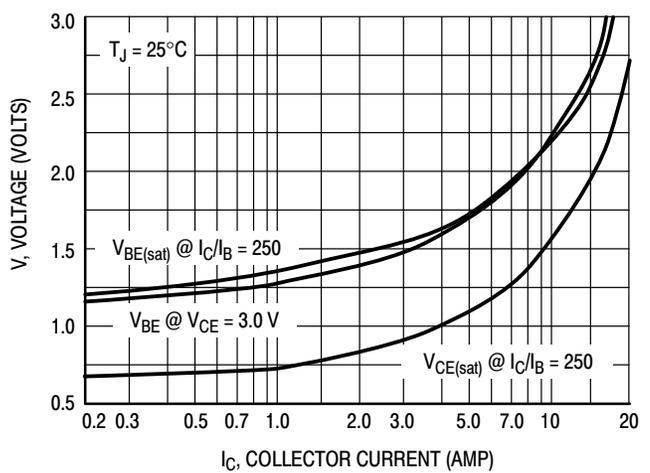
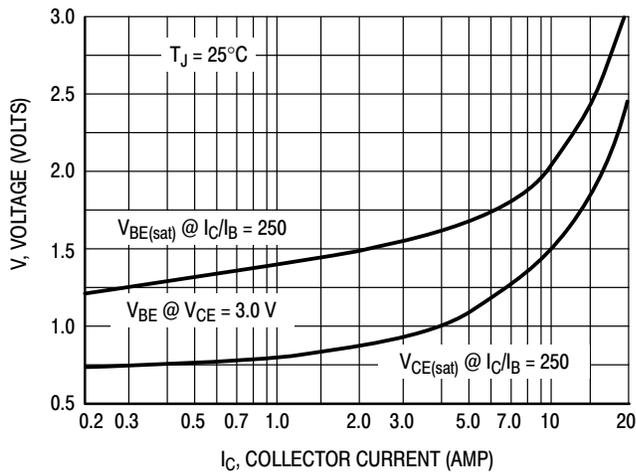
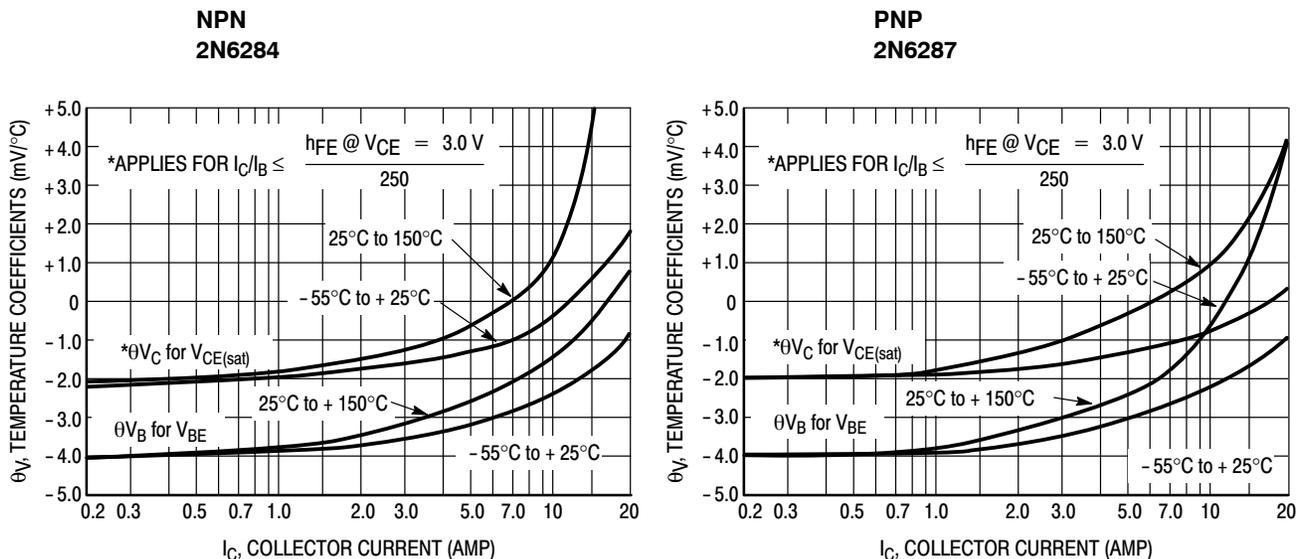
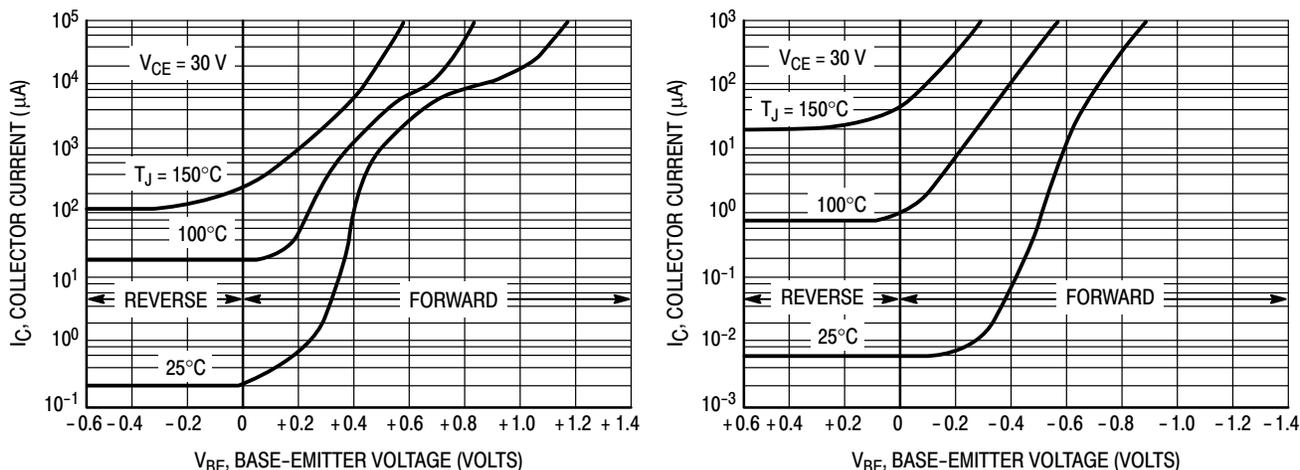


Figure 10. "On" Voltages

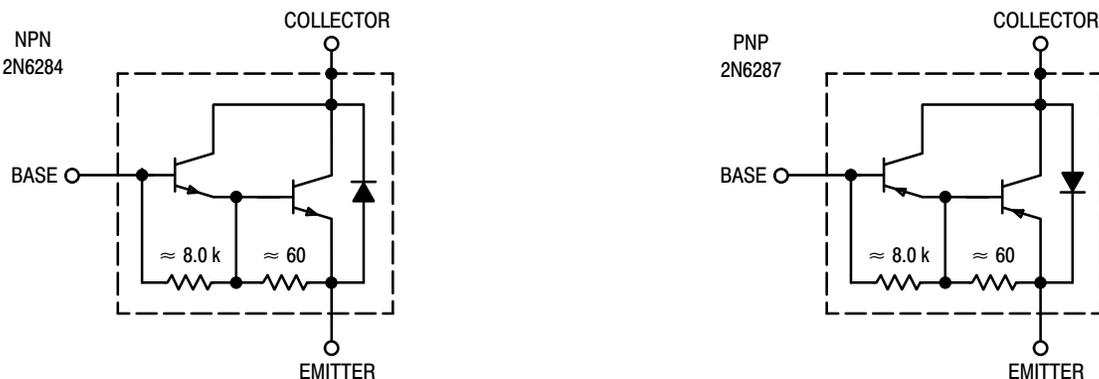
## 2N6284 (NPN); 2N6286, 2N6287 (PNP)



**Figure 11. Temperature Coefficients**



**Figure 12. Collector Cut-Off Region**



**Figure 13. Darlington Schematic**

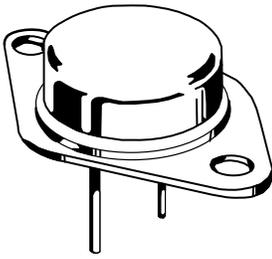
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor

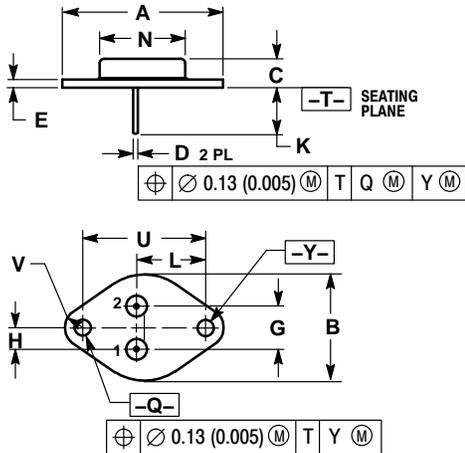


TO-204 (TO-3)  
CASE 1-07  
ISSUE Z

DATE 05/18/1988



SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.550 REF | ---   | 39.37 REF   | ---   |
| B   | ---       | 1.050 | ---         | 26.67 |
| C   | 0.250     | 0.335 | 6.35        | 8.51  |
| D   | 0.038     | 0.043 | 0.97        | 1.09  |
| E   | 0.055     | 0.070 | 1.40        | 1.77  |
| G   | 0.430 BSC | ---   | 10.92 BSC   | ---   |
| H   | 0.215 BSC | ---   | 5.46 BSC    | ---   |
| K   | 0.440     | 0.480 | 11.18       | 12.19 |
| L   | 0.665 BSC | ---   | 16.89 BSC   | ---   |
| N   | ---       | 0.830 | ---         | 21.08 |
| Q   | 0.151     | 0.165 | 3.84        | 4.19  |
| U   | 1.187 BSC | ---   | 30.15 BSC   | ---   |
| V   | 0.131     | 0.188 | 3.33        | 4.77  |

- |  |  |   |   |   |
|--|--|---|---|---|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. EMITTER<br/>CASE: COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>CASE: EMITTER</p> | <p>STYLE 3:<br/>PIN 1. GATE<br/>2. SOURCE<br/>CASE: DRAIN</p>           | <p>STYLE 4:<br/>PIN 1. GROUND<br/>2. INPUT<br/>CASE: OUTPUT</p>       | <p>STYLE 5:<br/>PIN 1. CATHODE<br/>2. EXTERNAL TRIP/DELAY<br/>CASE: ANODE</p> |
| <p>STYLE 6:<br/>PIN 1. GATE<br/>2. EMITTER<br/>CASE: COLLECTOR</p> | <p>STYLE 7:<br/>PIN 1. ANODE<br/>2. OPEN<br/>CASE: CATHODE</p>     | <p>STYLE 8:<br/>PIN 1. CATHODE #1<br/>2. CATHODE #2<br/>CASE: ANODE</p> | <p>STYLE 9:<br/>PIN 1. ANODE #1<br/>2. ANODE #2<br/>CASE: CATHODE</p> |   |

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