Silicon NPN Power Transistors 2SD1765

DESCRIPTION

·With TO-220Fa package
·DARLINGTON
·High DC current gain

APPLICATIONS

·For low frequency power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

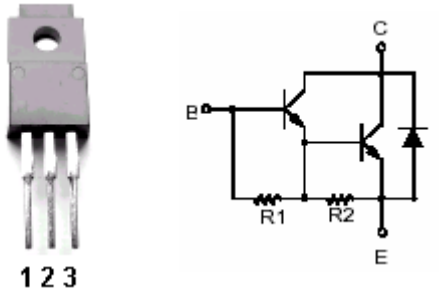

Fig.1 simplified outline (TO-220Fa) and symbol

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	100	V
V_{CEO}	Collector -emitter voltage	Open base	100	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		2	A
I_{CM}	Collector current-peak		3	A
P_C	Collector power dissipation	T_C=25□	20	W
		T_a=25□	2	
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C=50μA; I_C=0	100			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=5mA;I_B=0	100			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=1A ;I_B=1mA			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=100V; I_E=0			10	μA
I_{EBO}	Emitter cut-off current	V_{EB}=5V; I_C=0			3.0	mA
h_{FE}	DC current gain	I_C=1A ; V_{CE}=2V	1000		10000	
C_{OB}	Output capacitance	I_E=0 ; V_{CB}=10V;f=1MHz		25		pF

PACKAGE OUTLINE

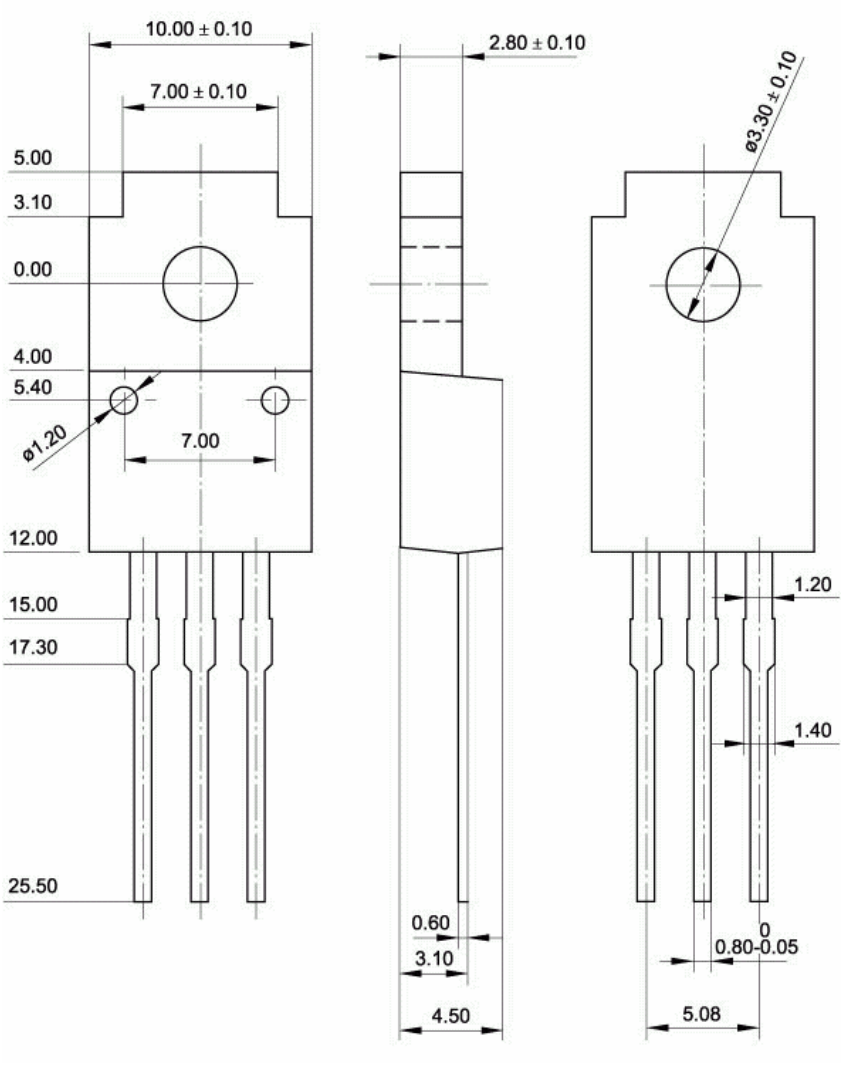

Fig.2 Outline dimensions (unindicated tolerance: ±0.15 mm)