

# MOS FIELD EFFECT TRANSISTOR 2SK3057

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### **DESCRIPTION**

This product is N-Channel MOS Field Effect Transistor designed for high current switching application.

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SK3057	Isolated TO-220

#### **FEATURES**

· Low on-state resistance

 $R_{DS(on)1} = 17 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, ID} = 23 \text{ A)}$ 

 $R_{DS(on)2} = 27 \text{ m}\Omega \text{ MAX.}$  (Vgs = 4 V, ID = 23 A)

- Low Ciss: Ciss = 2100 pF TYP.
- · Built-in gate protection diode
- Isolated TO-220 package

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	VDSS	60	V
Gate to Source Voltage	VGSS(AC)	±20	V
Gate to Source Voltage	VGSS(DC)	+20, -10	V
Drain Current (DC)	ID(DC)	±45	Α
Drain Current (pulse) Note1	D(pulse)	±150	Α
Total Power Dissipation (Tc = 25°C)	Рт	30	W
Total Power Dissipation (T <sub>a</sub> = 25°C)	PT	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	IAS	22.5	Α
Single Avalanche Energy Note2	Eas	50.6	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %

2. Starting Tch = 25 °C, RG = 25  $\Omega$ , VGS = 20 V $\rightarrow$ 0

#### THERMAL RESISTANCE

Channel to Case	Rth(ch-c)	4.17	°C/W	
Channel to Ambient	Rth(ch-a)	62.5	°C/W	

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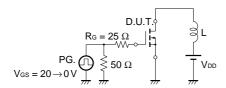
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

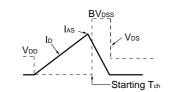


### **ELECTRICAL CHARACTERISTICS (TA = 25 °C)**

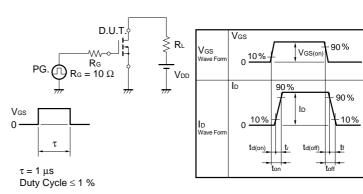
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Ip = 23 A		12	17	mΩ
	RDS(on)2	Vgs = 4 V, ID = 23 A		17	27	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 23 A	13	42		S
Drain Leakage Current	IDSS	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	$V_{GS} = \pm 20  \text{V},  V_{DS} = 0  \text{V}$			±10	μΑ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		2100		pF
Output Capacitance	Coss	Vgs = 0 V		550		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		220		pF
Turn-on Delay Time	t <sub>d(on)</sub>	ID = 23 A		35		ns
Rise Time	tr	V <sub>GS(on)</sub> = 10 V		410		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 30 V		120		ns
Fall Time	<b>t</b> f	R <sub>G</sub> = 10 Ω		200		ns
Total Gate Charge	Q <sub>G</sub>	ID = 45 A		45		nC
Gate to Source Charge	Qgs	V <sub>DD</sub> = 48 V		7.0		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS(on)</sub> = 10 V		13		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 45 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 45 A, VGS = 0 V		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs	_	100		nC

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**





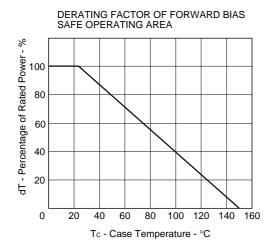
#### **TEST CIRCUIT 2 SWITCHING TIME**

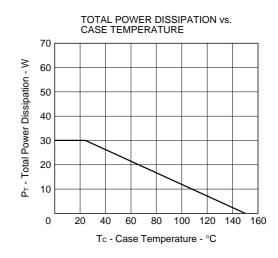


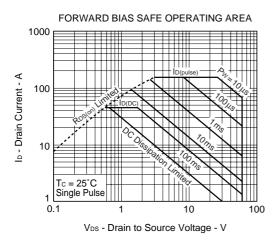
#### **TEST CIRCUIT 3 GATE CHARGE**

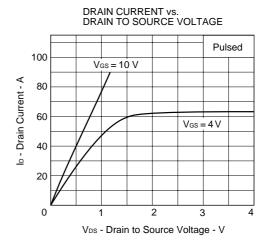


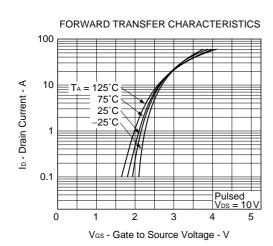
### TYPICAL CHARACTERISTICS (TA = 25 °C)





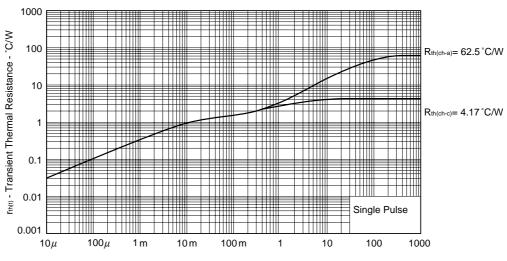






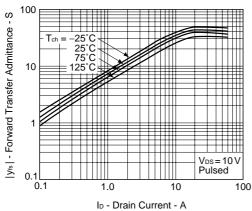
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#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

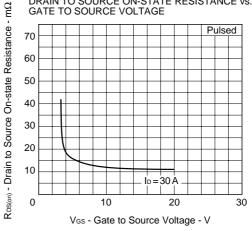


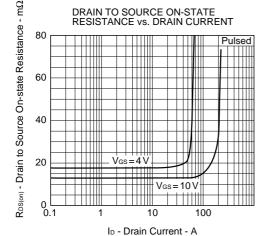
PW - Pulse Width - s

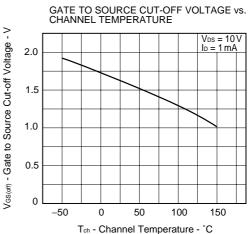




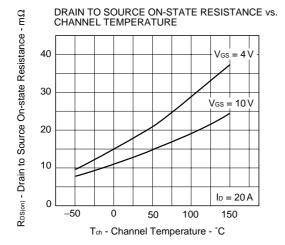
### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

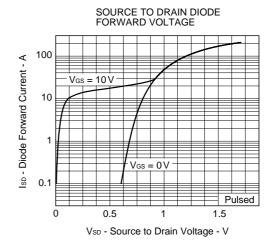


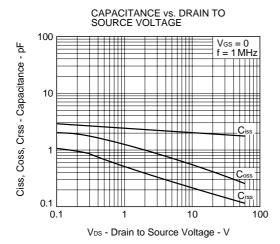


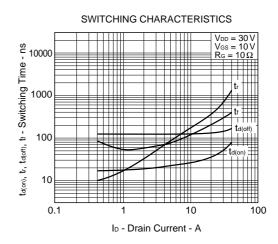


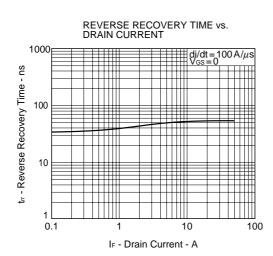


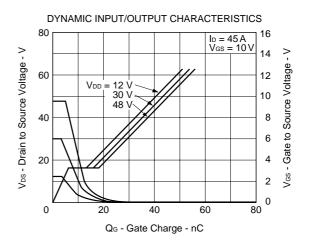




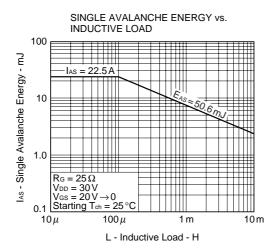


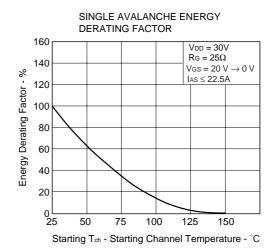






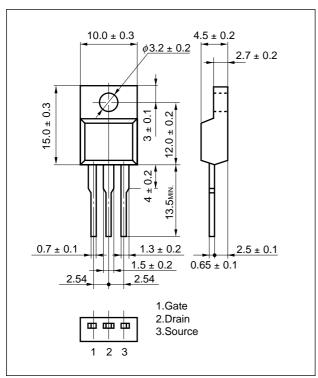




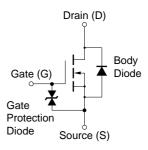


#### PACKAGE DRAWING (Unit: mm)

#### Isolated TO-220 (MP-45F)



#### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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