

DATA SHEET

NEC**MOS FIELD EFFECT TRANSISTOR
2SK3298****SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE****DESCRIPTION**

The 2SK3298 is N-channel MOS FET device that features a low gate charge and excellent switching characteristics, designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3298	Isolated TO-220

FEATURES

- Low gate charge
 $Q_G = 34 \text{ nC TYP. (} V_{DD} = 450 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 7.5 \text{ A)}$
- Gate voltage rating $\pm 30 \text{ V}$
- Low on-state resistance
 $R_{DS(on)} = 0.75 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
- Avalanche capability ratings
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	600	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±30	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±7.5	A
Drain Current (Pulse) ^{Note1}	I _{D(pulse)}	±30	A
Total Power Dissipation (T _A = 25°C)	P _{T1}	2.0	W
Total Power Dissipation (T _C = 25°C)	P _{T2}	40	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current ^{Note2}	I _{AS}	7.5	A
Single Avalanche Energy ^{Note2}	E _{AS}	37.5	mJ

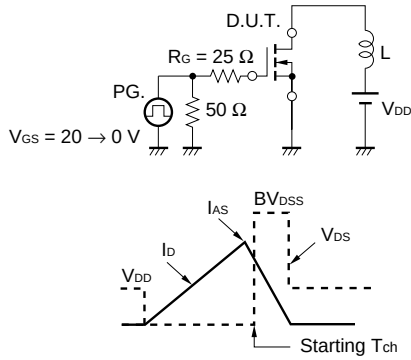
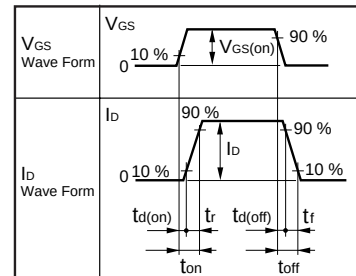
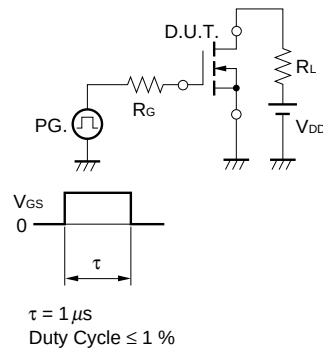
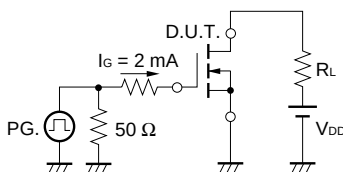
Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

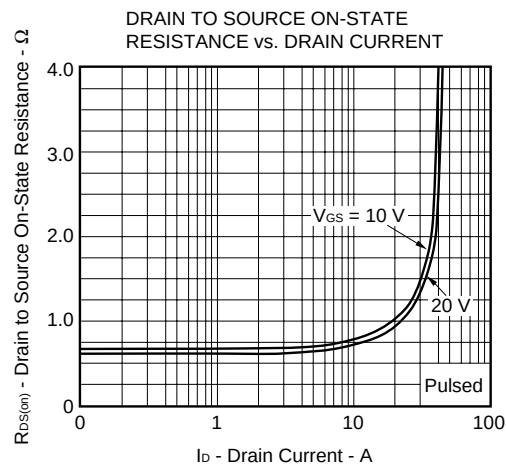
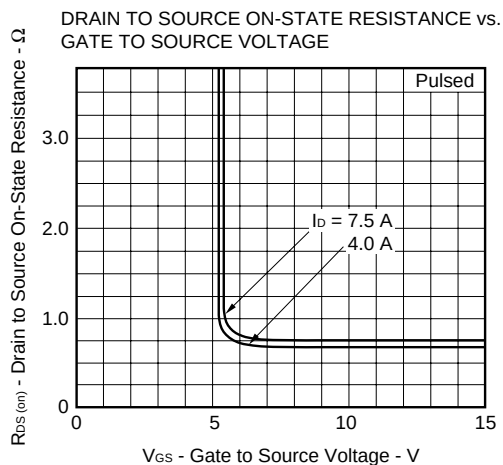
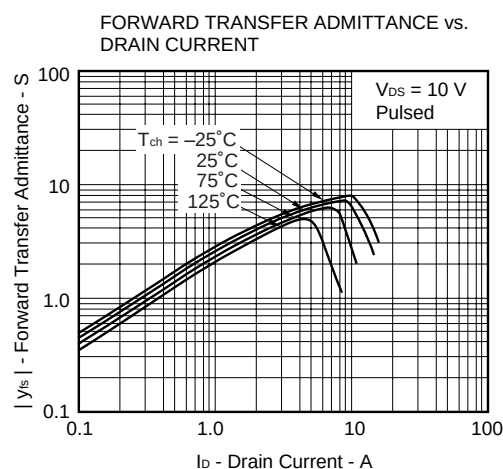
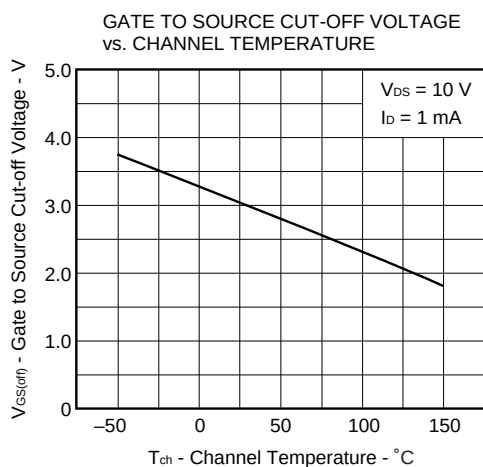
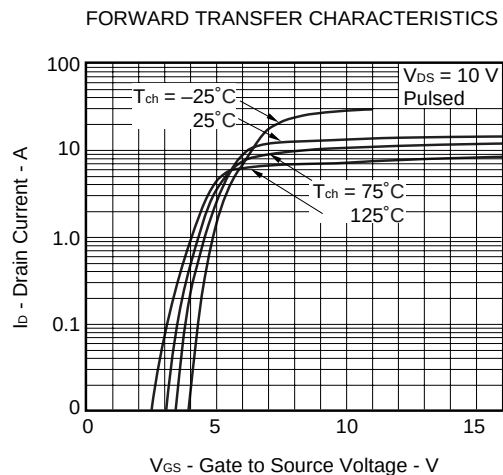
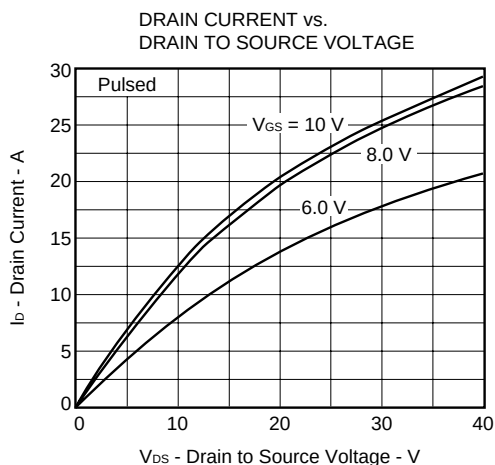
2. Starting T_{ch} = 25 °C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 V → 0 V

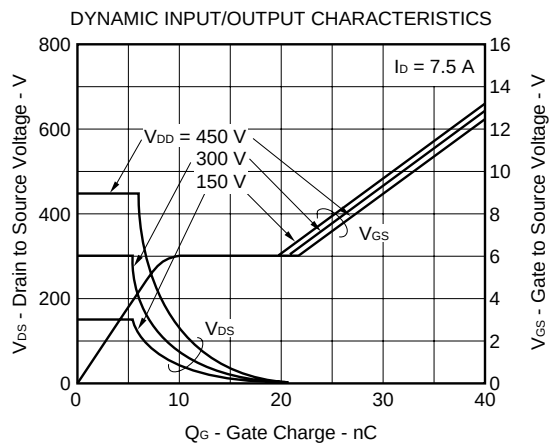
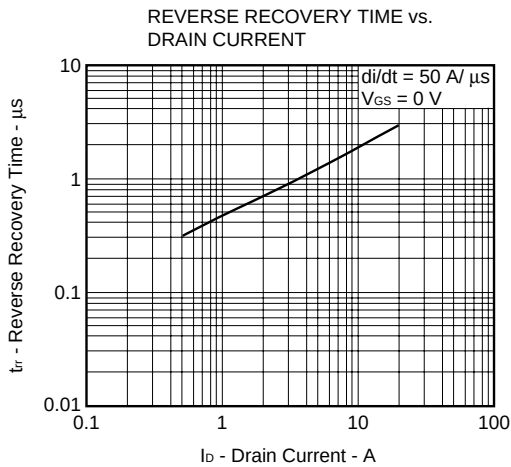
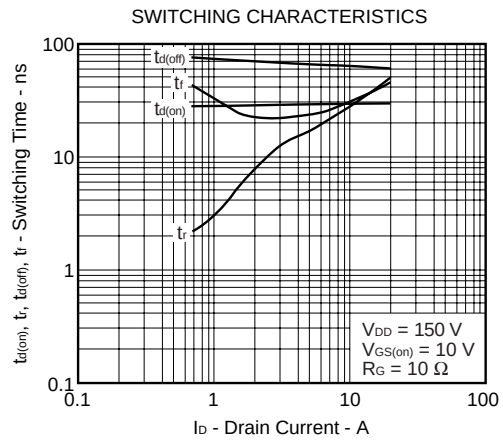
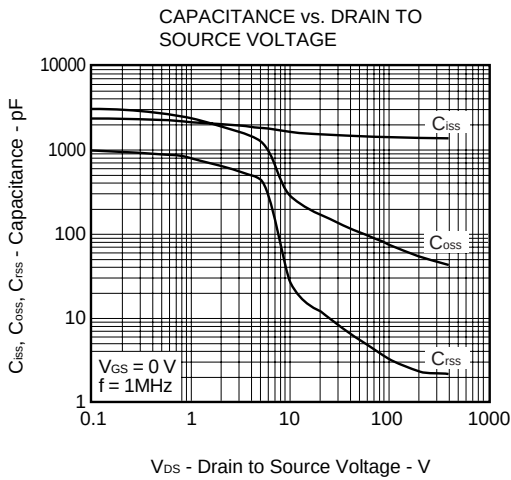
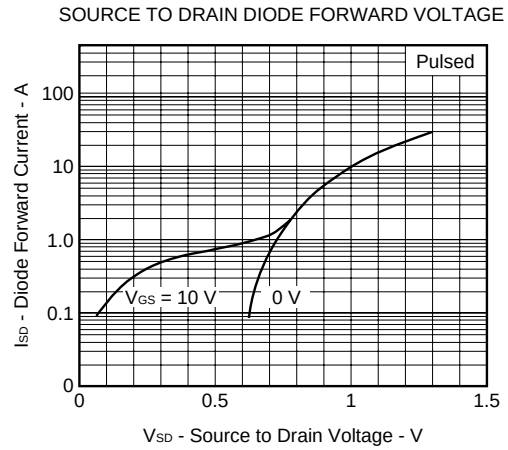
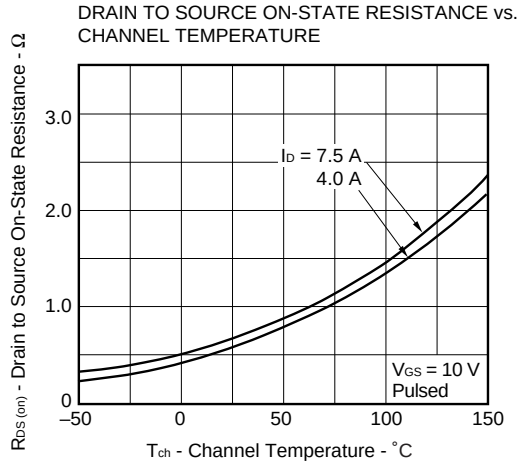
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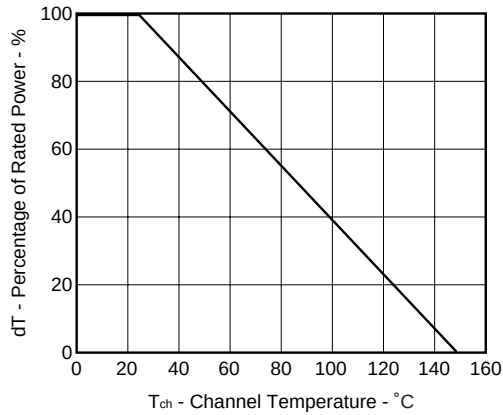
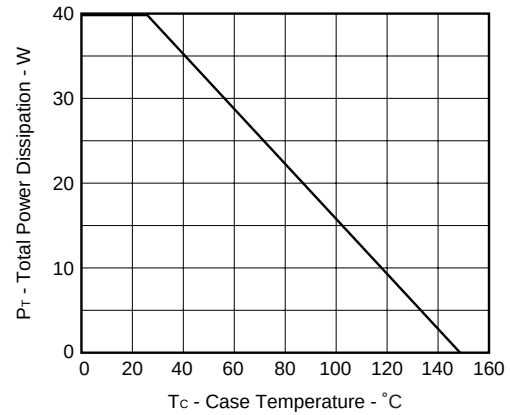
ELECTRICAL CHARACTERISTICS(T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	3.2			S
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.0 A		0.67	0.75	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		1580		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		280		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		25		pF
Turn-on Delay Time	t _{d(on)}	I _D = 4.0 A		27		ns
Rise Time	t _r	V _{GS(on)} = 10 V		14		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 150 V		66		ns
Fall Time	t _f	R _G = 10 Ω		24		ns
Total Gate Charge	Q _G	I _D = 7.5 A		34		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 450 V		8.2		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		12.3		nC
Diode Forward Voltage	V _{F(S-D)}	I _F = 7.5 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 7.5 A, V _{GS} = 0 V		1.6		μs
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		9.0		μC

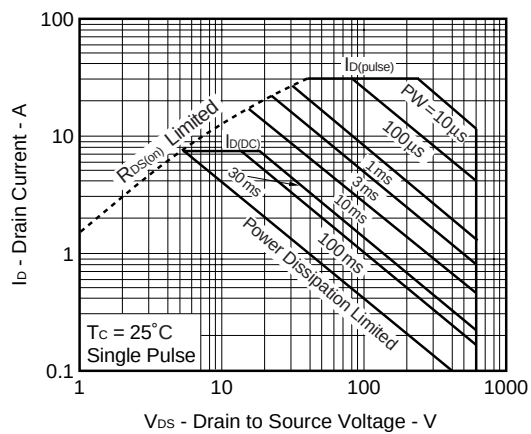
★ **TEST CIRCUIT 1 AVALANCHE CAPABILITY****TEST CIRCUIT 2 SWITCHING TIME****TEST CIRCUIT 3 GATE CHARGE**

★ TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

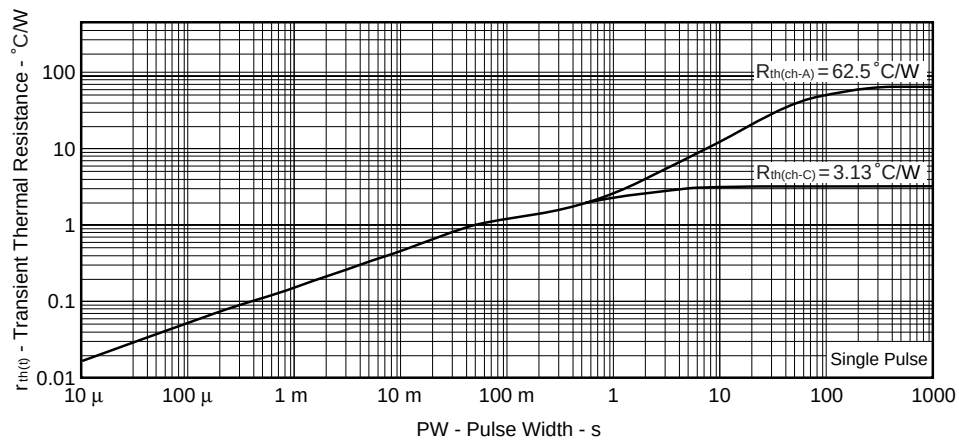


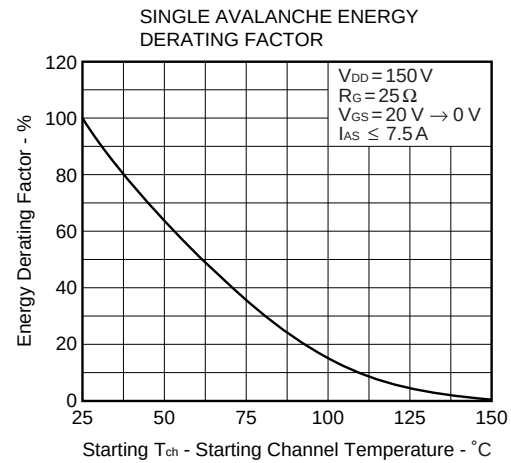
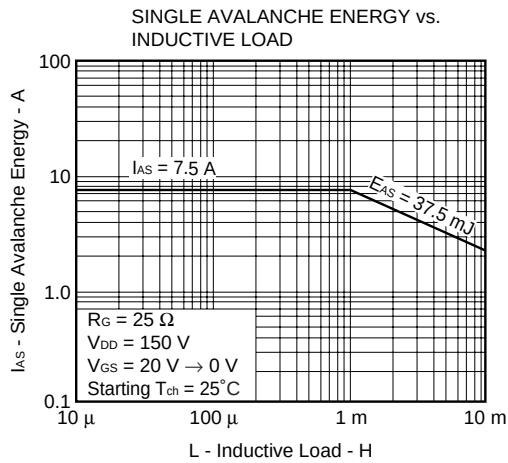
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREATOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

FORWARD BIAS SAFE OPERATING AREA



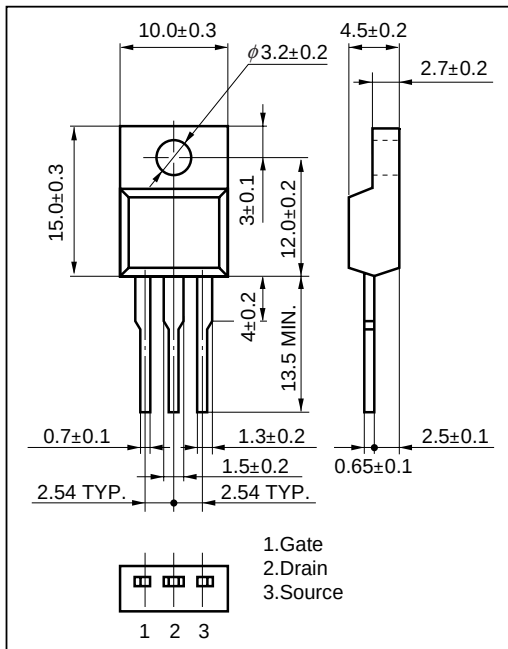
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



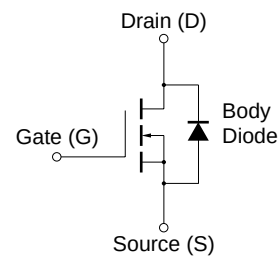


PACKAGE DRAWING (Unit : mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

[MEMO]

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