Ordering number: EN 3454

SANYO No.3454

2SK1451

N-Channel MOS Silicon FET

Very High-Speed Switching Applications

Features

- Low ON-state resistance.
- Very high-speed switching.
- Converters.
- Micaless package facilitating mounting.

Absolute Maximum Ratings at Ta = 25°C

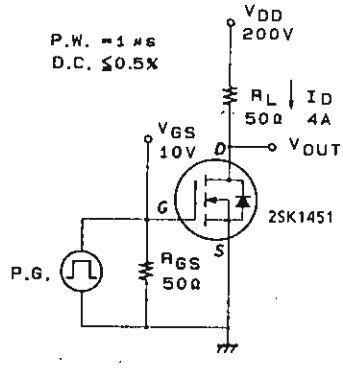
				unit
Drain to Source Voltage	V_{DSS}		450	V
Gate to Source Voltage	V_{GSS}		±30	V
Drain Current(DC)	I_D		8	A
Drain Current(Pulse)	I_{DP}	PW≦10μs, duty cycle≦1%	32	A
Allowable Power Dissipation	P_D	Tc=25°C	50	W
			3.0	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Electrical Characteristics at Ta = 25°C

			min	typ	max	unit
D-S Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	450			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=450V, V_{GS}=0			1.0	mA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0			±100	nA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	2.0		3.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS}=10V, I_D=4A	3.0	6.0		S
Static Drain to Source on State Resistance	$R_{DS(on)}$	I_D=4A, V_{GS}=10V		0.6	0.8	Ω
Input Capacitance	Ciss	V_{DS}=20V, f=1MHz		1200		pF
Output Capacitance	Coss	V_{DS}=20V, f=1MHz		180		pF
Reverse Transfer Capacitance	Crss	V_{DS}=20V, f=1MHz		70		pF
Turn-ON Delay Time	$t_{d(on)}$	I_D=4A, V_{GS}=10V V_{DD}=200V, R_{GS}=50Ω		20		ns
Rise Time	t_r			40		ns
Turn-OFF Delay Time	$t_{d(off)}$			160		ns
Fall Time	t_f			60		ns
Diode Forward Voltage	V_{SD}	I_S=8A, V_{GS}=0			1.8	V

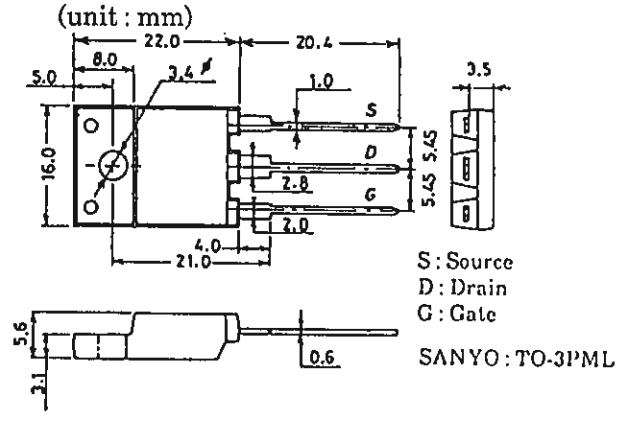
(Note) Be careful in handling the 2SK1451 because it has no protection diode between gate and source.

Switching Time Test Circuit



Package Dimensions 2076

(unit : mm)



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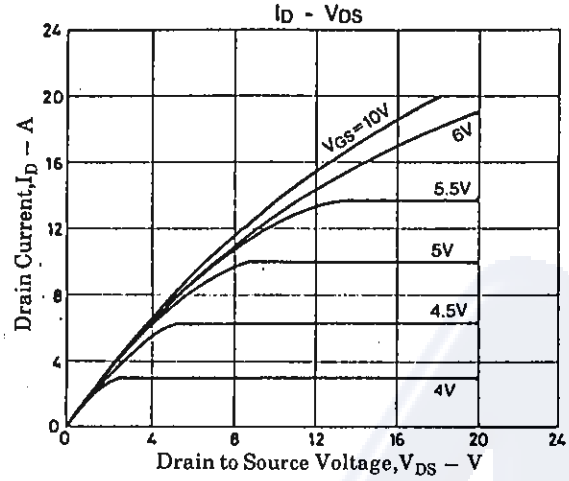
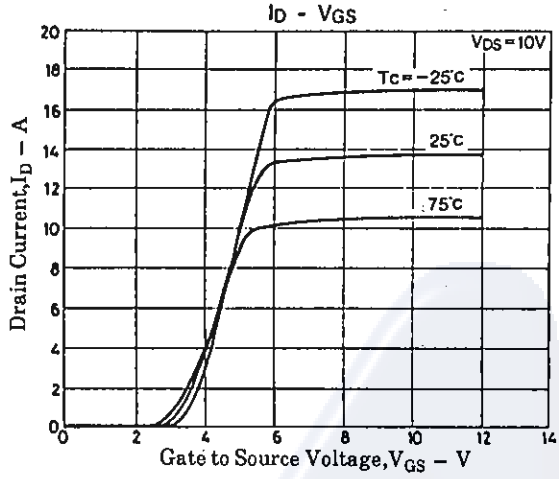
TOKYO OFFICE Tokyo Bldg.,1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

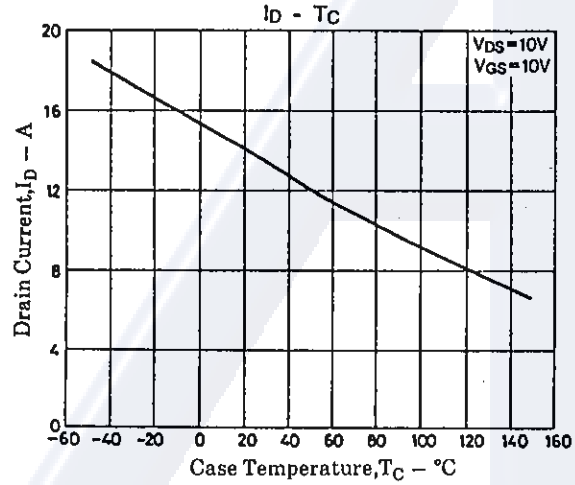
I_D - V_{DS}



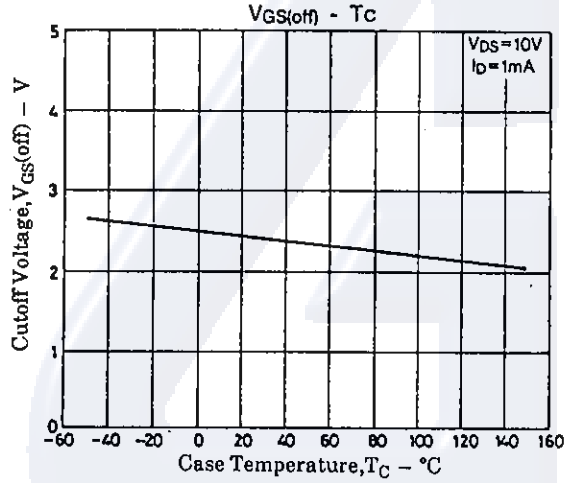
I_D - V_{GS}



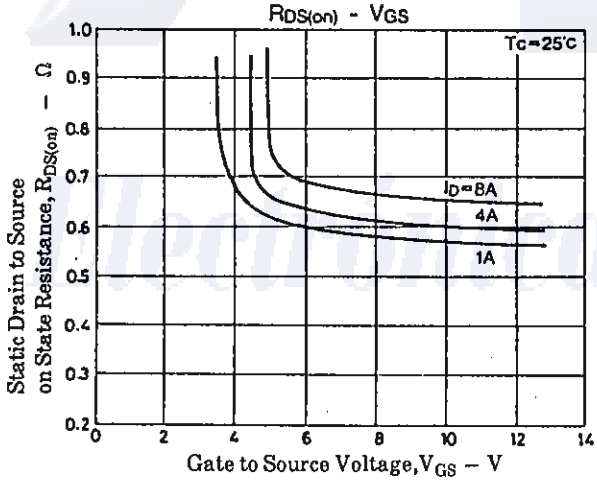
I_D - Tc



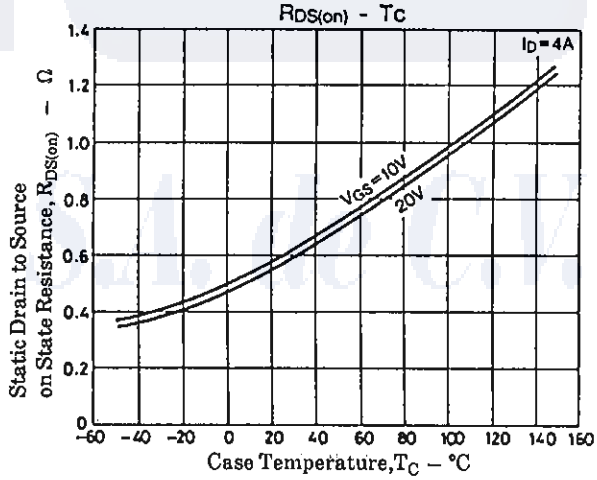
$V_{GS(off)}$ - Tc



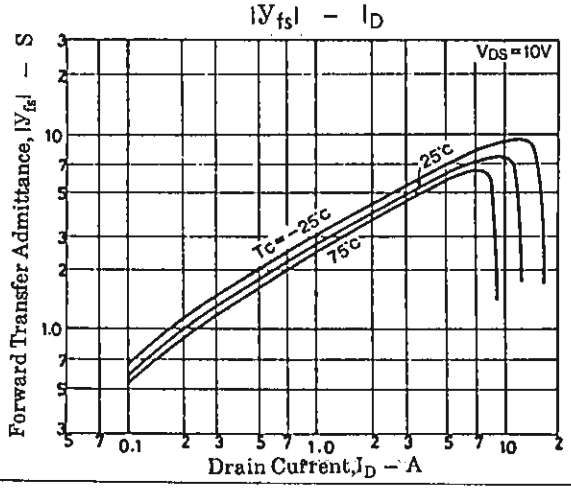
$R_{DS(on)}$ - V_{GS}



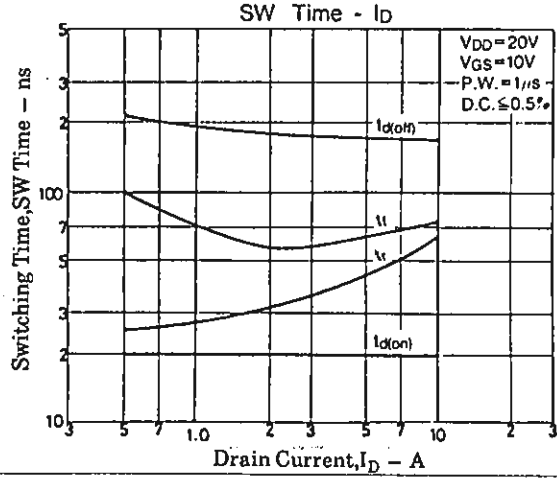
$R_{DS(on)}$ - Tc



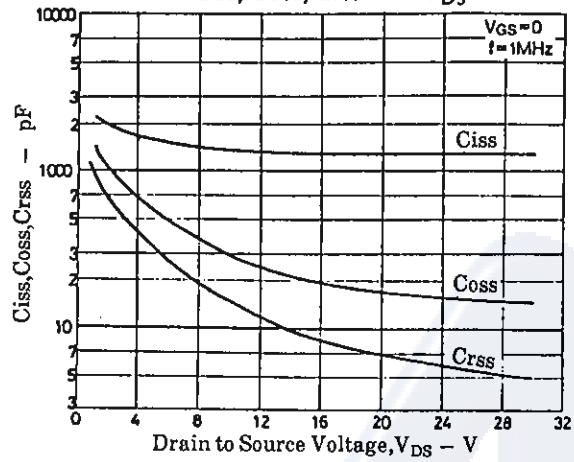
$|y_{fs}|$ - I_D



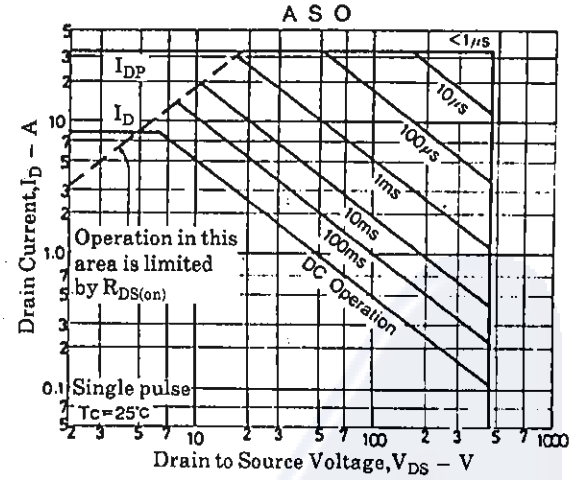
SW Time - I_D



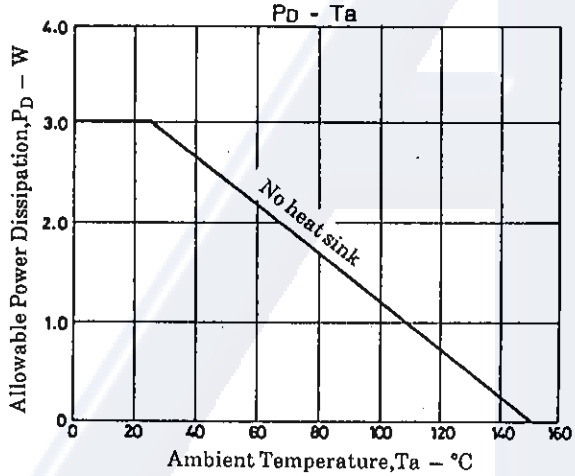
Ciss, Coss, Crss – V_{DS}



A S O



P_D - Ta



P_D – Tc