



October 1987
Revised January 1999

CD4007C Dual Complementary Pair Plus Inverter

General Description

The CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS} .

For proper operation the voltages at all pins must be constrained to be between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$ at all times.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{CC} (typ.)

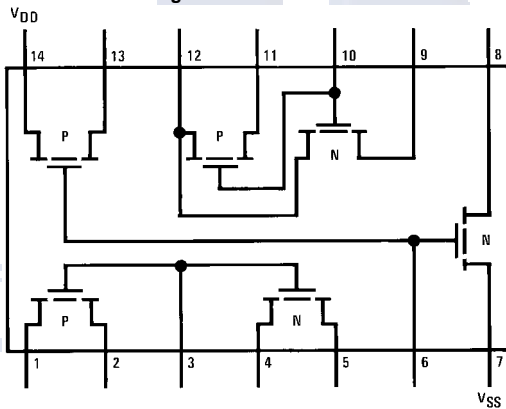
Ordering Code:

Order Number	Package Number	Package Description
CD4007CM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
CD4007CN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP and SOIC



Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS} .

Top View

CD4007C Dual Complementary Pair Plus Inverter

CD4007C

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$	Operating V_{DD} Range	$V_{SS} + 3.0V$ to $V_{SS} + 15V$
Operating Temperature Range	$-40^{\circ}C$ to $+85^{\circ}C$	Lead Temperature	
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$	(Soldering, 10 seconds)	$260^{\circ}C$
Power Dissipation (P_D)			
Dual-In-Line	700 mW		
Small Outline	500 mW		

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Limits									Units
			−40°C			+25°C			+85°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _L	Quiescent Device Current	V _{DD} = 5.0V			0.5		0.005	0.05			15	μA
		V _{DD} = 10V			1.0		0.005	1.0			30	μA
P _D	Quiescent Device Dissipation Package	V _{DD} = 5.0V			2.5		0.025	2.5			75	μW
		V _{DD} = 10V			10		0.05	10			300	μW
V _{OL}	Output Voltage LOW Level	V _{DD} = 5.0V			0.05		0	0.01			0.05	V
		V _{DD} = 10V			0.05		0	0.01			0.05	V
V _{OH}	Output Voltage HIGH Level	V _{DD} = 5.0V	4.95			4.95	5.0		4.95			V
		V _{DD} = 10V	9.95			9.95	10		9.95			V
V _{NL}	Noise Immunity (All inputs)	V _{DD} = 5.0V, V _O = 3.6V			1.5		2.25	1.5			1.4	V
		V _{DD} = 10V, V _O = 7.2V			3.0		4.5	3.0			2.9	V
V _{NH}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O = 0.95V	3.6			3.5	2.25		3.5			V
		V _{DD} = 10V, V _O = 2.9V	7.1			7.0	4.5		7.0			V
I _{DN}	Output Drive Current N-Channel	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD}	0.35			0.3	1.0		0.24			mA
		V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	1.2			1.0	2.5		0.8			mA
I _{DP}	Output Drive Current P-Channel	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS}	−1.3			−1.1	−4.0		−0.9			mA
		V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.65			−0.55	−2.5		−0.45			mA
I _I	Input Current						10					pA

AC Electrical Characteristics (Note 2)

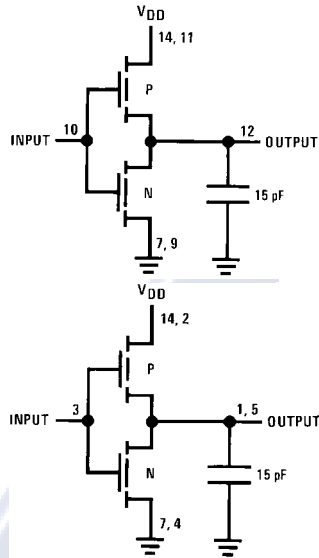
$T_A = 25^{\circ}C$ and $C_L = 15$ pF and rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$		35	75	ns
		$V_{DD} = 10V$		20	50	ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5.0V$		50	100	ns
		$V_{DD} = 10V$		30	50	ns
C_I	Input Capacitance	Any Input		5		pF

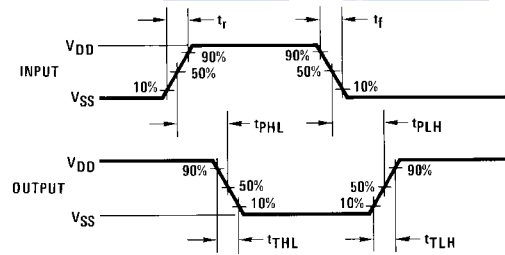
Note 2: AC Parameters are guaranteed by DC correlated testing.

CD4007C

AC Test Circuits

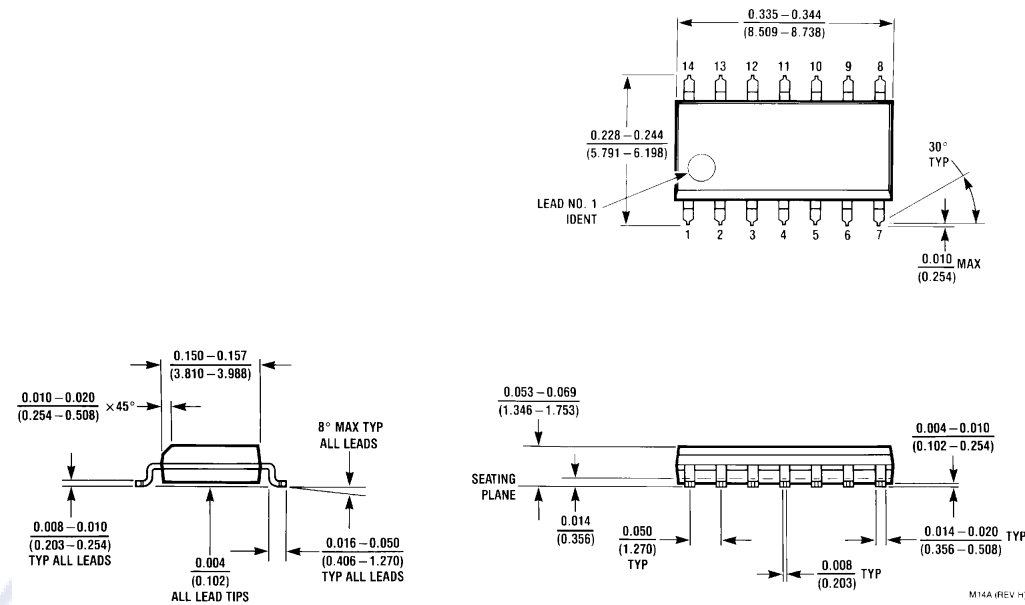


Switching Time Waveforms

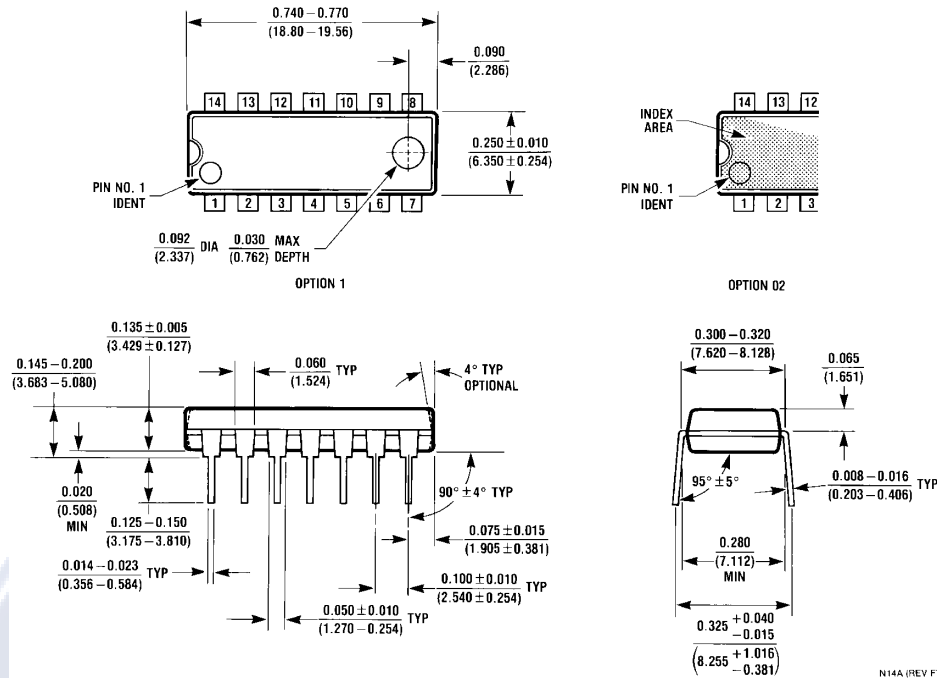


Electrónica S.A. de C.V.

CD4007C

Physical Dimensions inches (millimeters) unless otherwise noted

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

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