



October 1987
Revised July 1999

CD40174BC • CD40175BC

Hex D-Type Flip-Flop • Quad D-Type Flip-Flop

General Description

The CD40174BC consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. The CD40175BC consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available. All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and $\bar{Q}$ s (CD40175BC only) to logical "1". All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS} .

Features

- Wide supply voltage range: 3V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility:
fan out of 2 driving 74L or 1 driving 74 LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

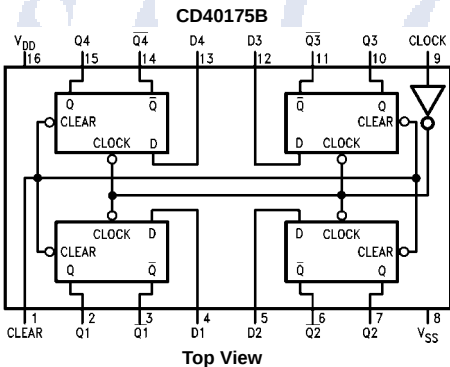
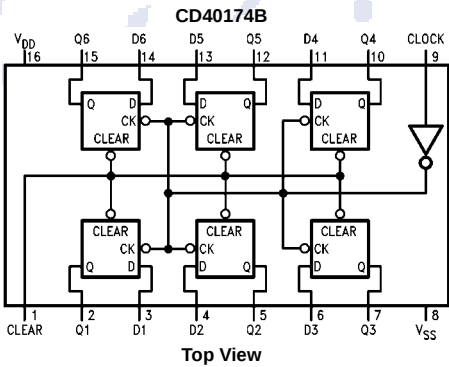
Ordering Code:

Order Number	Package Number	Package Description
CD40174BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD40174BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD40175BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD40175BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for DIP and SOIC



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Truth Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$ (Note 1)
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = HIGH Level
L = LOW Level
X = Irrelevant
↑ = Transition from LOW-to-HIGH level
NC = No change
Note 1: $\overline{Q}$ for CD40175B only

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Absolute Maximum Ratings(Note 2)

(Note 3)

DC Supply Voltage (V_{DD})	-0.5V to +18V
Input Voltage (V_{IN})	-0.5V to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	-40°C to +85°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

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Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		4			4		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		8			8		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		16			16		120	μA
V_{OL}	LOW Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.30		-10 ⁻⁵	-0.30		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.30		10 ⁻⁵	0.30		1.0	μA

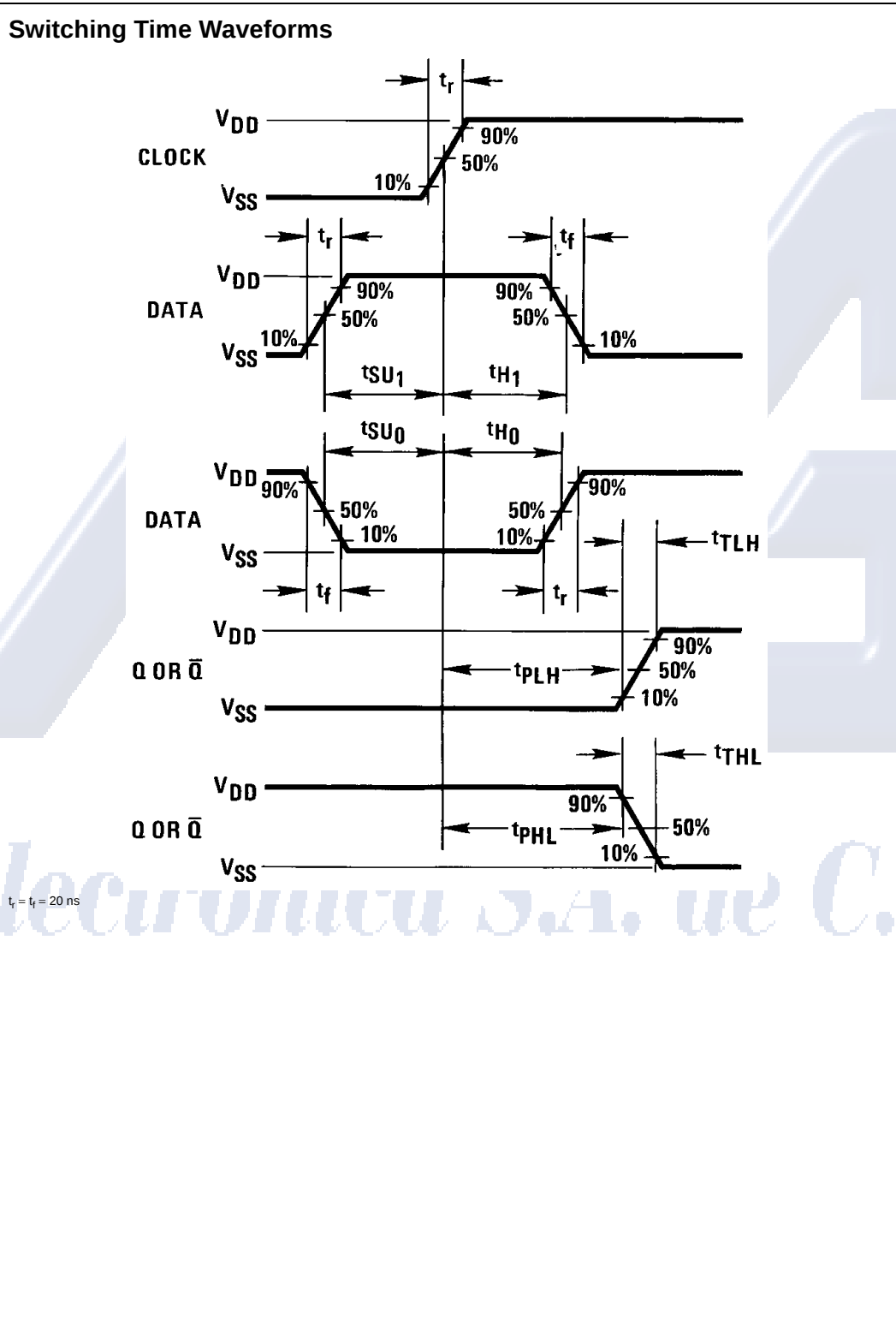
Note 4: I_{OH} and I_{OL} are tested one output at a time.

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AC Electrical Characteristics (Note 5) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$ and $t_r = t_f = 20\text{ ns}$, unless otherwise specified

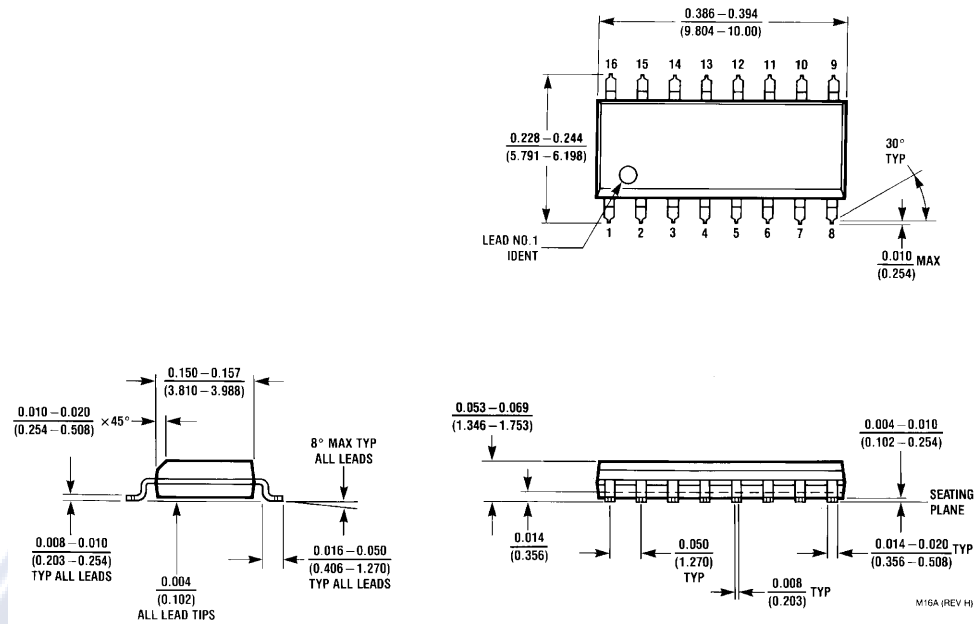
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\bar{Q}$ (CD40175 Only)	$V_{DD} = 5\text{V}$		190	300	ns
		$V_{DD} = 10\text{V}$		75	110	ns
		$V_{DD} = 15\text{V}$		60	90	ns
t_{PHL}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{DD} = 5\text{V}$		180	300	ns
		$V_{DD} = 10\text{V}$		70	110	ns
		$V_{DD} = 15\text{V}$		60	90	ns
t_{PLH}	Propagation Delay Time to a Logical "1" from Clear to $\bar{Q}$ (CD40175 Only)	$V_{DD} = 5\text{V}$		230	400	ns
		$V_{DD} = 10\text{V}$		90	150	ns
		$V_{DD} = 15\text{V}$		75	120	ns
t_{SU}	Time Prior to Clock Pulse that Data must be Present	$V_{DD} = 5\text{V}$		45	100	ns
		$V_{DD} = 10\text{V}$		15	40	ns
		$V_{DD} = 15\text{V}$		13	35	ns
t_H	Time after Clock Pulse that Data Must be Held	$V_{DD} = 5\text{V}$		-11	0	ns
		$V_{DD} = 10\text{V}$		-4	0	ns
		$V_{DD} = 15\text{V}$		-3	0	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$		100	200	ns
		$V_{DD} = 10\text{V}$		50	100	ns
		$V_{DD} = 15\text{V}$		40	80	ns
t_{WH}, t_{WL}	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$		130	250	ns
		$V_{DD} = 10\text{V}$		45	100	ns
		$V_{DD} = 15\text{V}$		40	80	ns
t_{WL}	Minimum Clear Pulse Width	$V_{DD} = 5\text{V}$		120	250	ns
		$V_{DD} = 10\text{V}$		45	100	ns
		$V_{DD} = 15\text{V}$		40	80	ns
t_{RCL}	Maximum Clock Rise Time	$V_{DD} = 5\text{V}$	15			μs
		$V_{DD} = 10\text{V}$	5.0			μs
		$V_{DD} = 15\text{V}$	5.0			μs
t_{FCL}	Maximum Clock Fall Time	$V_{DD} = 5\text{V}$	15	50		μs
		$V_{DD} = 10\text{V}$	5.0	50		μs
		$V_{DD} = 15\text{V}$	5.0	50		μs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5\text{V}$	2.0	3.5		MHz
		$V_{DD} = 10\text{V}$	5.0	10		MHz
		$V_{DD} = 15\text{V}$	6.0	12		MHz
C_{IN}	Input Capacitance	Clear Input		10	15	pF
		Other Input		5.0	7.5	pF
C_{PD}	Power Dissipation	Per Package (Note 6)		130		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.**Note 6:** C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.



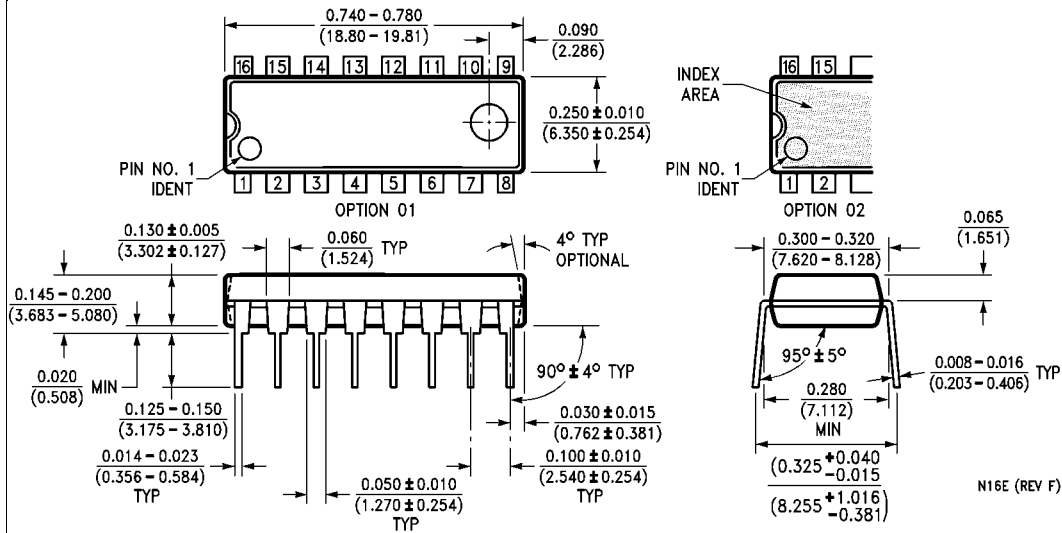
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Physical Dimensions inches (millimeters) unless otherwise noted

**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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