

INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4072B **gates** Dual 4-input OR gate

Product specification
File under Integrated Circuits, IC04

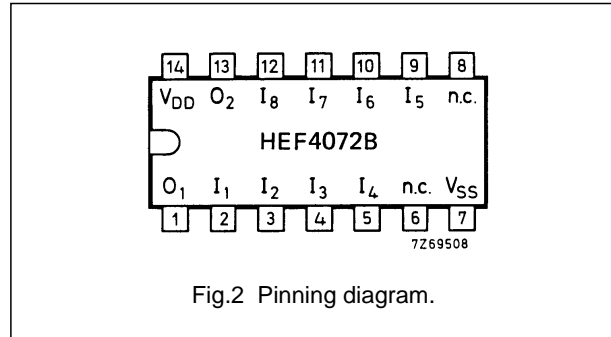
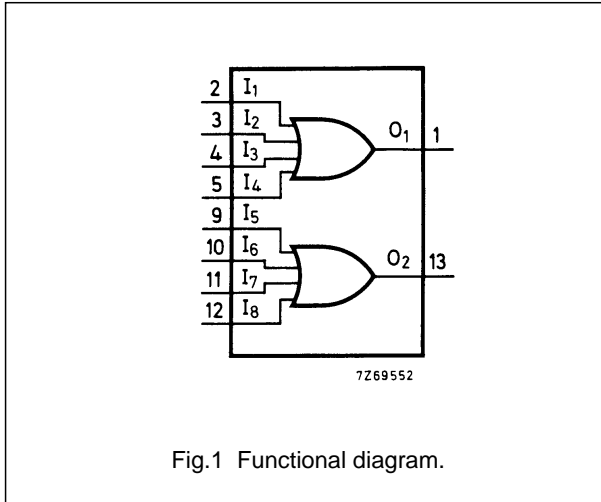
January 1995

Dual 4-input OR gate

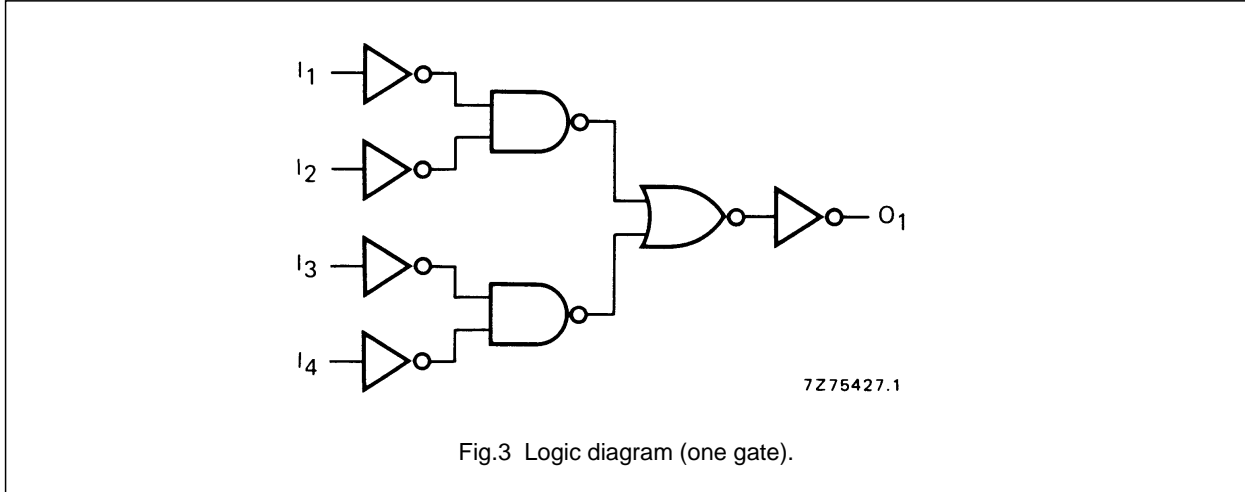
HEF4072B gates

DESCRIPTION

The HEF4072B provides the positive dual 4-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4072BP(N): 14-lead DIL; plastic (SOT27-1)
 - HEF4072BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
 - HEF4072BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America



FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

Dual 4-input OR gate

HEF4072B
gates**AC CHARACTERISTICS**V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays I _n → O _n HIGH to LOW	5	t _{PHL}	80	155	ns	53 ns + (0,55 ns/pF) C _L	
	10		35	70	ns	24 ns + (0,23 ns/pF) C _L	
	15		25	55	ns	17 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	75	145	ns	48 ns + (0,55 ns/pF) C _L
		10		35	70	ns	24 ns + (0,23 ns/pF) C _L
		15		25	55	ns	17 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L	
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
	LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
		10		30	60	ns	9 ns + (0,42 ns/pF) C _L
		15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	950 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	4500 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	13 700 f _i + ∑ (f _o C _L) × V _{DD} ²	