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DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4085B gates

Dual 2-wide 2-input AND-OR-invert gate

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

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Dual 2-wide 2-input AND-OR-invert gate

HEF4085B gates

DESCRIPTION

The HEF4085B is a dual 2-wide 2-input AND-OR-invert gate, each with an additional input (A_4 or B_4) which can be used as either an expander input or an inhibit input. A HIGH on A_4 or B_4 forces the output (O_A or O_B) LOW independent of the other inputs (A_0 to A_3 or B_0 to B_3). The outputs O_A and O_B are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

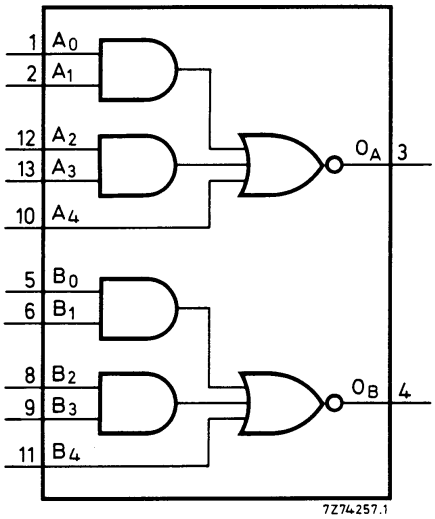

Fig.1 Functional diagram.

Fig.2 Pinning diagram.

HEF4085BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4085BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF4085BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America

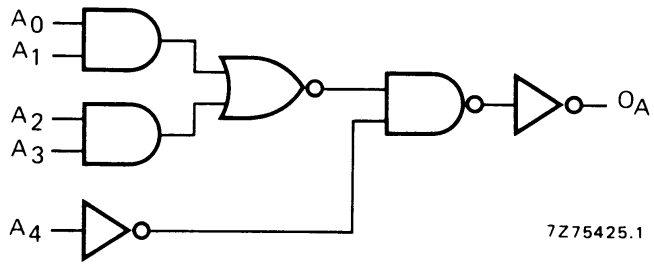

Fig.3 Logic diagram (one gate).

LOGIC FUNCTION

$$O_A = \overline{A_0 \cdot A_1 + A_2 \cdot A_3 + A_4}$$

$$O_B = \overline{B_0 \cdot B_1 + B_2 \cdot B_3 + B_4}$$

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
A_n, $B_n \rightarrow O_n$	5		75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		65	135	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	55	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$750\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$3200\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$9200\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

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