SDLS042

SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

MAY 1983 - REVISED MARCH 1988

- Programmable Output Pulse Width
 With R_{int}...35 ns Typ
 With R_{ext}/C_{ext}...40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

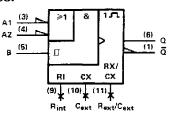
SN54121 J OR W PACKAGE SN74121 N PACKAGE (TOP VIEW)							
Q 1	14 VCC						
NC 2	13 NC						
A1 3	12 NC						
A2 4	11 Rext/Cext						
B 5	10 Cext						
Q 6	9 Rint						
GND 7	8 NC						

NC - No internal connection.

FUNCTION TABLE

INPUTS			OUTPUTS
A1	A2	В	<u>a</u> <u>ā</u>
L	Х	H	L H
x	L	H	Lt Ht
х	х	L	Lt Ht
н	Н	X	Lt Ht]
Н	1	н	17 17
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L x	L	1	17 77





[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

For explanation of function table symbols, see page

† These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to VCC noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC} , C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

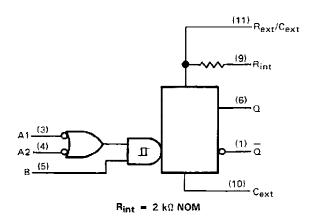
Jitter-free operation is maintained over the full temperature and VCC ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54121 and 2 k Ω to 40 k Ω for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{W(out)} = C_{ext}RT_{10} \approx 0.7 C_{ext}R_{10}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if VCC is held to 5 volts and free-air temperature is 25 °C. Duty cycles as high as 90% are achieved when using maximum recommended RT'. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

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logic diagram (positive logic)



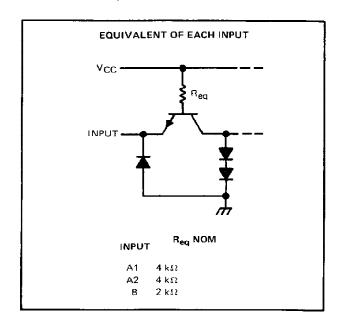
Pin numbers shown on logic notation are for J or N packages.

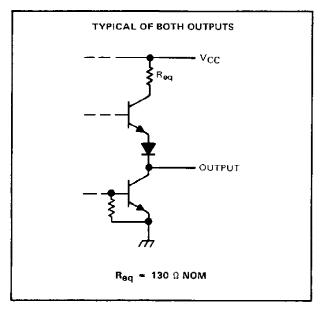
NOTES: 1. An external capacitor may be connected between $C_{\rm ext}$ (positive) and $H_{\rm ext}/C_{\rm ext}$.

2. To use the internal timing resistor, connect $H_{\rm int}$ to $V_{\rm CC}$. For improved pulse width accuracy and repeatability, connect an external resistor between $H_{\rm ext}/C_{\rm ext}$ and $V_{\rm CC}$

with Rint open-circuited.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 3)	. 7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54121 55 °C to 1	25°C
SN74121 0°C to	
Storage temperature range65°C to 1	50°C

NOTE 3: Voltage values are with respect to network ground terminal.

recommended operating conditions

				MIN	NOM	MAX	UNIT
VCC	Supply voltage	-	54 Family	4.5	5	5.5	,,
*	Outply voitage		74 Family	4.75	5	5.25	٧
Іон	High-level output current			i i		-0.4	mA
JOL	Low-level output current					16	mA
dv/dt	Rate of rise or fall of input pulse	Schmitt input, B		1			V/s
		Logic inputs, A1, A2		1			V/μs
tw(in)	input pulse width	ridth		50			ns
Rext	External timing capacitance		54 Family	1.4		30	
''ext	External timing capacitance		74 Family	1.4		40	kΩ
C _{ext}	External timing capacitance			0		1000	μF
	Duty cycle	$R_T = 2 k\Omega$	$i_T = 2 k\Omega$			67	%
	Daty Cycle	R _T = MAX R _{ext}				90	
T _A	Operating free-air temperature		54 Family	- 55		125	
'A	Operating nee-on temperature		74 Family	0		70	۵C



electrical characteristics over recommended operating free-air temperature range (unless otherwise

PARAMETER		TEST CONDITONS [†]		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage at B input	V _{CC} = MIN		2			V
VIL	Low-level input voltage at A input	VCC - MIN	<u> </u>			0.8	٧
V _{T+}	Positive-going threshold voltage at B input	VCC = MIN		1	1.55	2	٧
VT_	Negative-going threshold voltage at B input	V _{CC} = MIN		0.8	1.35		>
Vik	Input clamp voltage	V _{CC} = MIN,	I _f = -12 mA			- 1.5	V
ЮН	High-level output voltage	V _{CC} = MIN,	IOH = MAX	2.4	3.4		٧
VoL	Low-level output voltage	VCC = MIN,	IOL = MAX		0.2	0.4	V
l _l	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 5.5 V			1	mA
		V _{CC} = MAX,	A1 or A2			40	
ΊΗ	High-level input current	V ₁ - 2.4 V	В			80	μА
IţL	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	A1 or A2		-	- 1.6	^
			В			- 3.2	mA
1	Short-circuit output current [§]	V _{CC} = MAX	54 Family	- 20		- 55	^
los			74 Family	- 18		- 55	mA
	0 1	V _{CC} = MAX	Quiescent		13	25	^
ICC	Supply current		Triggered		23	40	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

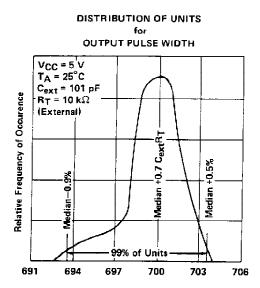
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
^t PLH	Propagation dalay time, low-to-high- level Q output from either A input				45	70	ns
tPLH	Propagation delay time, low-to-high- level Ω output from B input		C _{ext} = 80 pF,		35	55	ns
tpHL	Propagation delay time, high-to-low level Q output from either A input	C _I = 15 pF,	R _{int} to V _{CC}		50	80	пŝ
^t PHL	Propagation delay time, high-to-low level $\overline{\Omega}$ output from 8 input	$R_L = 400 \Omega$, See Note 4			40	65	ns
tw(out)	Pulse width obtained using internal timing resistor		C _{ext} = 80 ρF, R _{int} to V _{CC}	70	110	150	ns
^t w(out)	Pulse width obtained with zero timing capacitance		C _{ext} = 0, R _{int} to V _{CC}		30	50	ns
	Pulse width obtained using		$C_{ext} = 100 \text{ pF},$ $R_T = 10 \text{ k}\Omega$	600	700	800	ns
^t w(out)	external timing resistor		$C_{\text{ext}} = 1 \mu\text{F},$ $R_{\text{T}} = 10 \text{k}\Omega$	6	7	8	ms

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. † Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS[†]



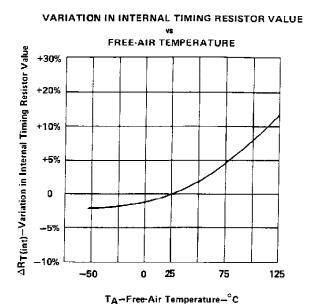


FIGURE 1

tw(out)-Output Pulse Width-ns

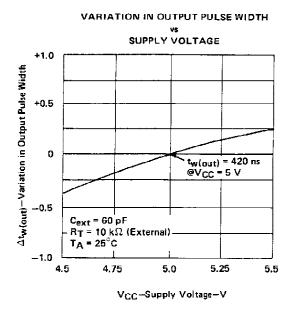


FIGURE 2

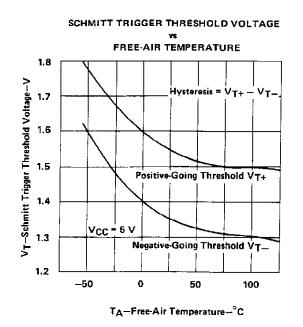


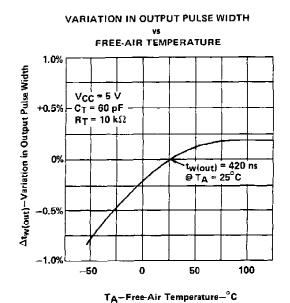
FIGURE 3

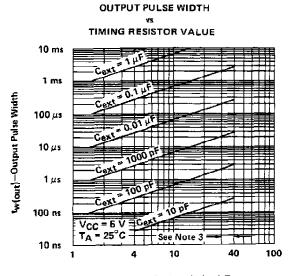
[†]Data for temperatures below 0°C and above 70°C are applicable for SN54121.

Figure 4

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TYPICAL CHARACTERISTICS[†] (continued)





R_T-Timing Resistor Value- $k\Omega$

FIGURE 5

FIGURE 6

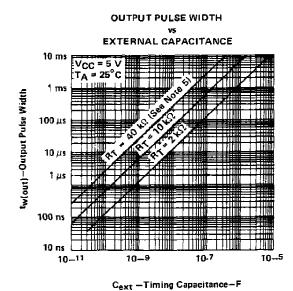


FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121. †Data for temperatures below 0 °C and above 70 °C are applicable for SN54121.



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