



September 1983
Revised February 1999

MM74HC32 Quad 2-Input OR Gate

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General Description

The MM74HC32 OR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

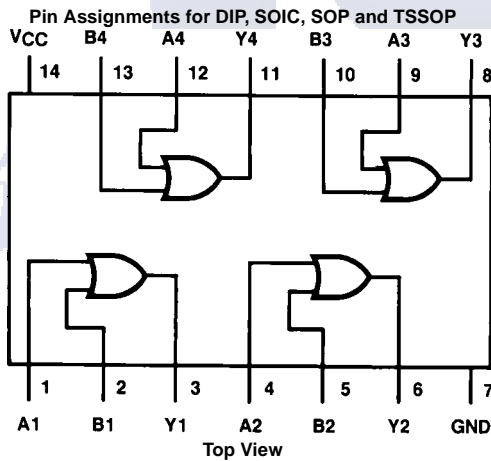
- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads

Ordering Code:

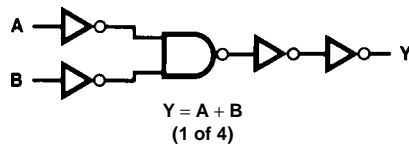
Order Number	Package Number	Package Description
MM74HC32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC32N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram



MM74HC32

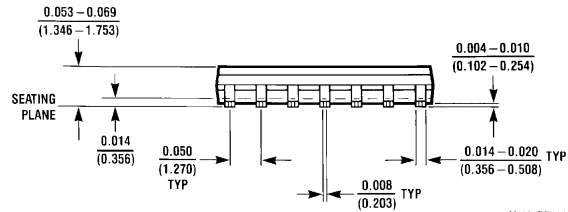
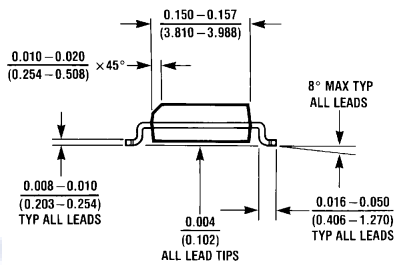
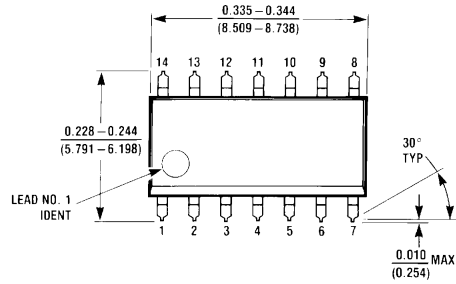
Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions						
(Note 2)			Min	Max	Units			
Supply Voltage (V _{CC})	-0.5 to +7.0V	Supply Voltage (V _{CC})	2	6	V			
DC Input Voltage (V _{IN})	-1.5 to V _{CC} + 1.5V	DC Input or Output Voltage (V _{IN} , V _{OUT})	0	V _{CC}	V			
DC Output Voltage (V _{OUT})	-0.5 to V _{CC} + 0.5V	Operating Temperature Range (T _A)	-40	+85	°C			
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA	Input Rise or Fall Times (t _r , t _f) V _{CC} = 2.0V		1000	ns			
DC Output Current, per pin (I _{OUT})	±25 mA	V _{CC} = 4.5V		500	ns			
DC V _{CC} or GND Current, per pin (I _{CC})	±50 mA	V _{CC} = 6.0V		400	ns			
Storage Temperature Range (T _{STG})	-65°C to +150°C	Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.						
Power Dissipation (P _D) (Note 3)	600 mW	Note 2: Unless otherwise specified all voltages are referenced to ground.						
S.O. Package only	500 mW	Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.						
Lead Temperature (T _L) (Soldering 10 seconds)	260°C							
DC Electrical Characteristics (Note 4)								
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C		Units
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V	
			4.5V		3.15	3.15	V	
			6.0V		4.2	4.2	V	
V _{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V	
			4.5V		1.35	1.35	V	
			6.0V		1.8	1.8	V	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.7	3.98	3.84	V	
			6.0V	5.2	5.48	5.34	V	
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
		V _{IN} = V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	V	
			6.0V	0.2	0.26	0.33	V	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	μA	
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		2.0	20	μA	
Note 4: For a power supply of 5V ±10% the worst case output voltages (V _{OH} and V _{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V _{IH} and V _{IL} occur at V _{CC} = 5.5V and 4.5V respectively. (The V _{IH} value at 5.5V is 3.85V.) The worst case leakage current (I _{IN} , I _{CC} , and I _{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.								

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AC Electrical Characteristics							
$V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$							
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units		
t_{PHL} , t_{PLH}	Maximum Propagation Delay		10	18	ns		
AC Electrical Characteristics							
$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)							
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		$T_A = -40 \text{ to } 85^\circ C$	Units
				Typ	Guaranteed Limits		
t_{PHL} , t_{PLH}	Maximum Propagation Delay		2.0V	30	100	125	ns
			4.5V	12	20	25	ns
			6.0V	9	17	21	ns
t_{TLH} , t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	ns
			4.5V	8	15	19	ns
			6.0V	7	13	16	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		50			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF
<p>Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.</p>							

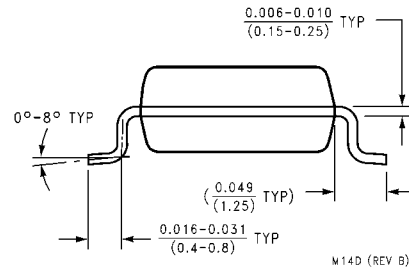
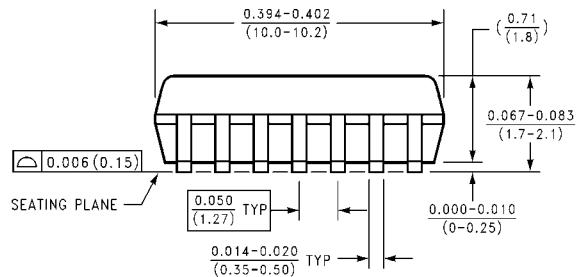
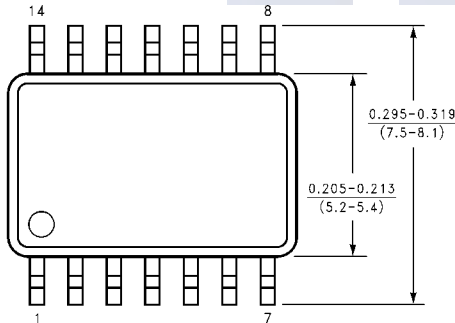
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Physical Dimensions inches (millimeters) unless otherwise noted



M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Package Number M14A



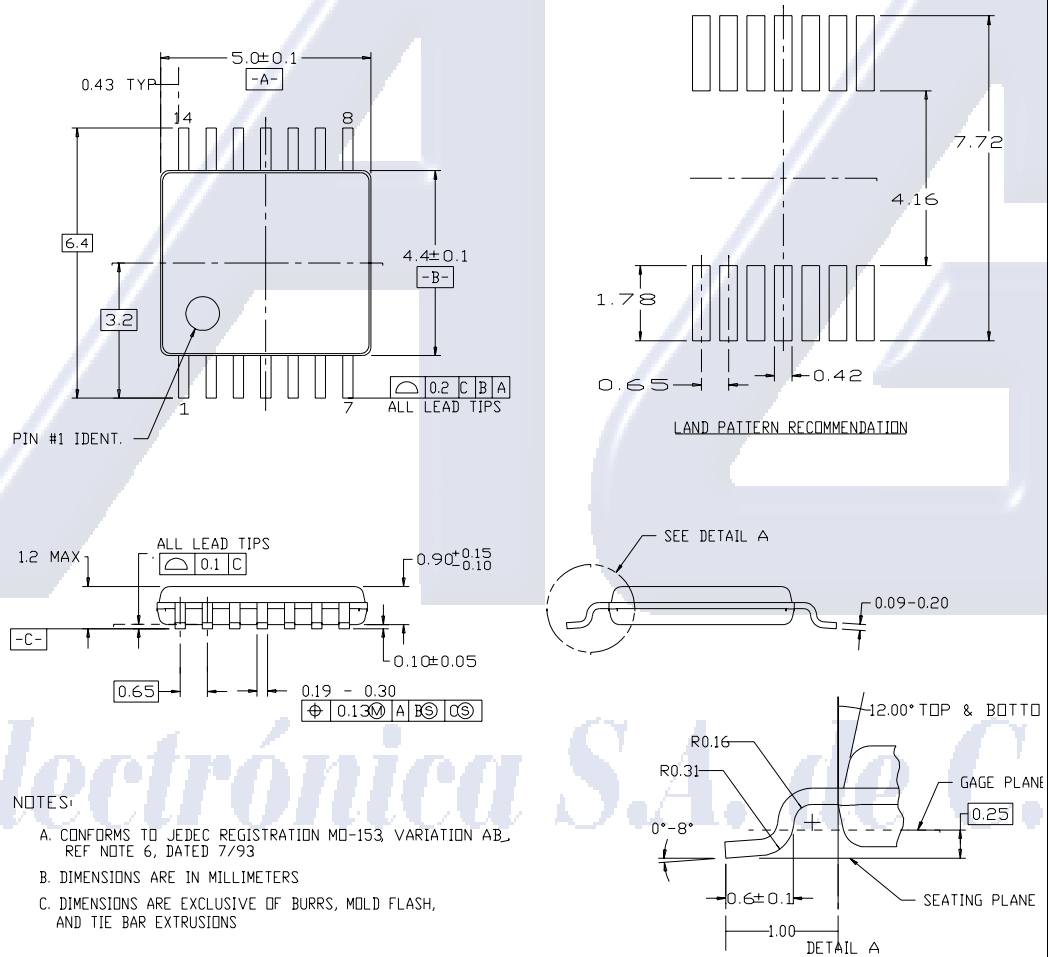
M14D (REV B)

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE



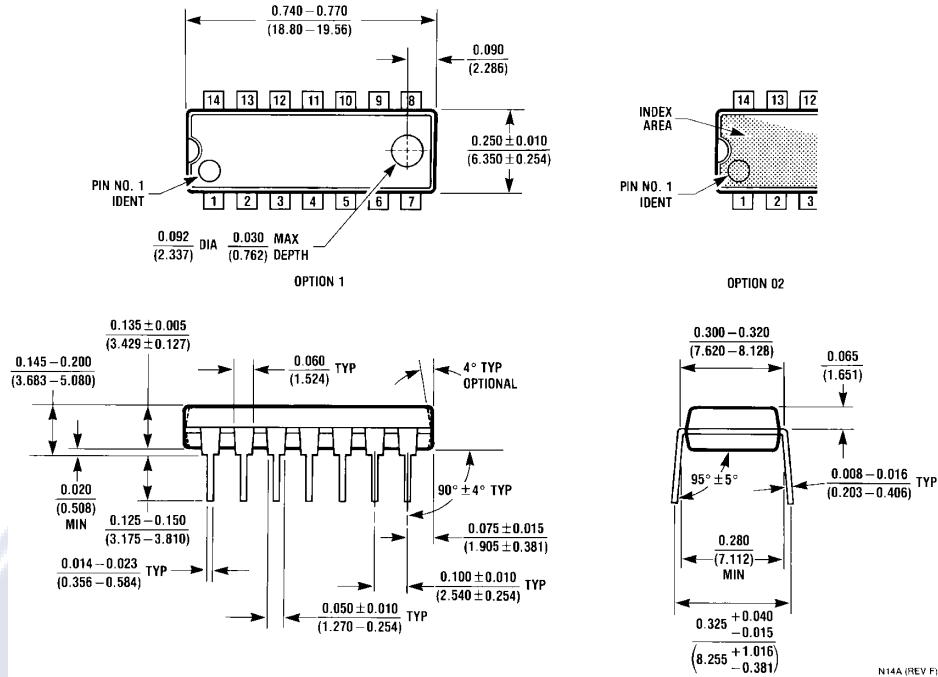
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

MM74HC32 Quad 2-Input OR Gate

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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