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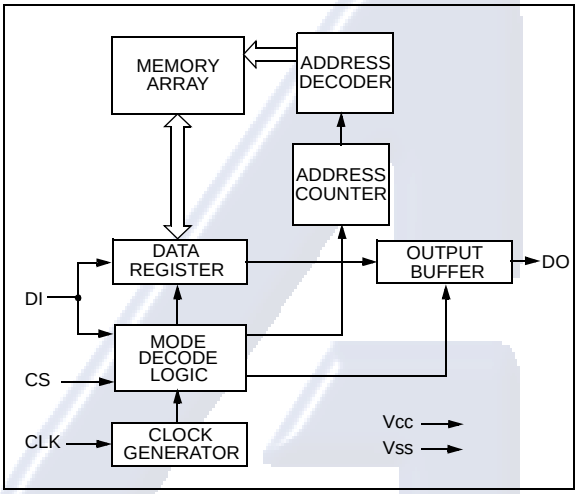
93LC66A/B

4K 2.5V Microwire® Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 512 x 8 bit organization (93LC66A)
- 256 x 16 bit organization (93LC66B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

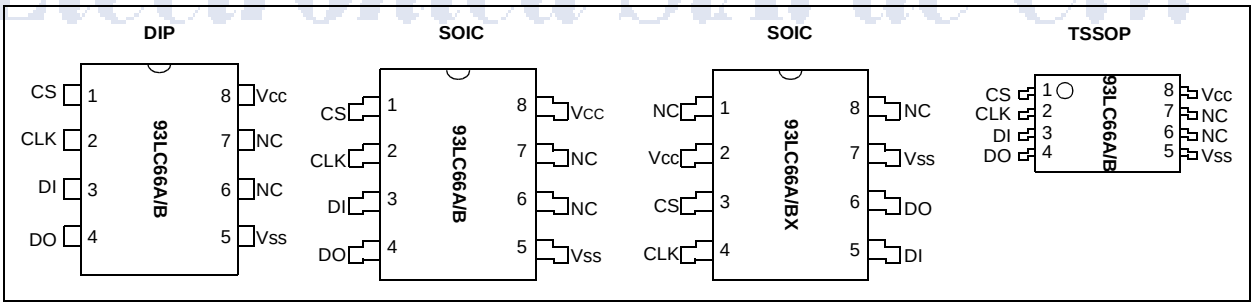
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93LC66A/B are 4K-bit, low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 (93LC66A) or x16 bits (93LC66B). Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. The 93LC66A/B is available in standard 8-pin DIP, surface mount SOIC, and TSSOP packages. The 93LC66AX/BX are only offered in a 150-mil SOIC package.

PACKAGE TYPE



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
NC	No Connect
VCC	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Commercial (C): Industrial (I):	VCC = +2.5V to +6.0V VCC = +2.5V to +6.0V	Tamb = 0°C to +70°C Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	Vcc +1	V	2.7V ≤ VCC ≤ 6.0V **(Note 2)**
	VIH2	0.7 VCC	Vcc +1	V	VCC < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	VCC > 2.7V **(Note 2)**
	VIL2	-0.3	0.2 Vcc	V	VCC < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 µA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	VCC-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = VSS to VCC
Output leakage current	ILO	-10	10	µA	VOUT = VSS to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V **(Notes 1 & 2)** Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC read	—	1 500	mA µA	FCLK = 2 MHz; Vcc = 6.0V FCLK = 1 MHz; Vcc = 3.0V
	ICC write	—	1.5	mA	
Standby current	ICCS	—	1	µA	CS = Vss; DI = VSS
Clock frequency	FCLK	—	2 1	MHz MHz	VCC > 4.5V VCC < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF **(Note 2)**
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	6	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode **(Note 3)**

Note 1: This parameter is tested at Tamb = 25°C and Fclk = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

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2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock (CLK) is used to synchronize the communication between a master device and the 93LC66A/B. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a “Don't Care” if CS is low (device deselected). If CS is high, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1 INSTRUCTION SET FOR 93LC66A

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20

TABLE 2-2 INSTRUCTION SET FOR 93LC66B

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27

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3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The READY/BUSY status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) Data Out (DO)

It is possible to connect the Data In (DI)and Data Out (DO)pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

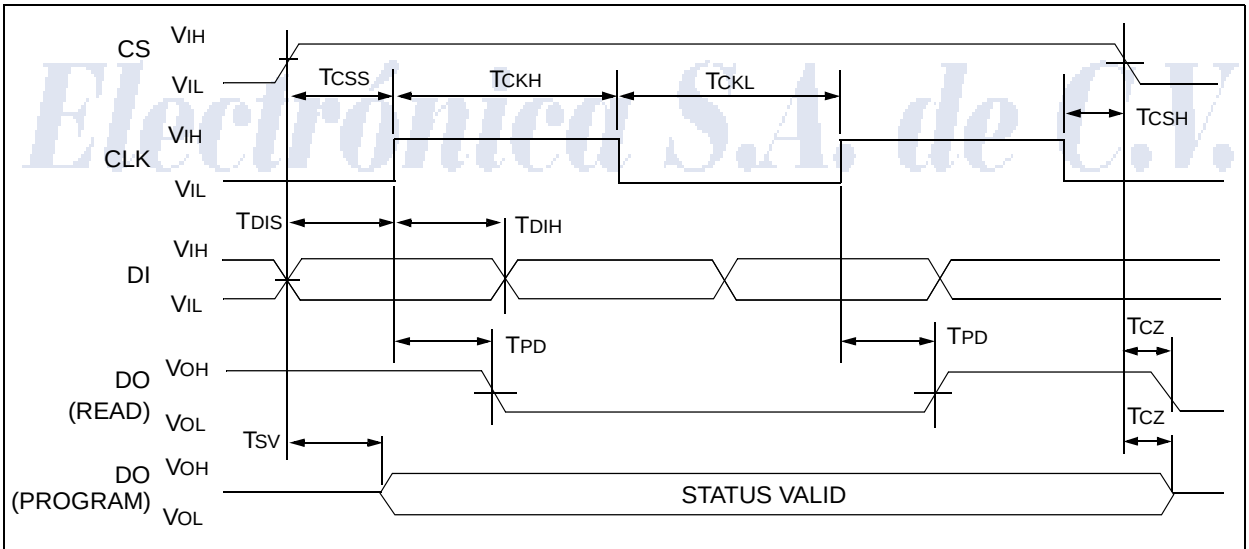
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until VCC has reached a level greater than 2.2V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 2.2V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE/WRITE Enable (EWEN) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC Test Conditions: VIL = 0.4V, VIH = 2.4V.

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3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical “0” indicates that programming is still in progress. DO at logical “1” indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical “1” state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

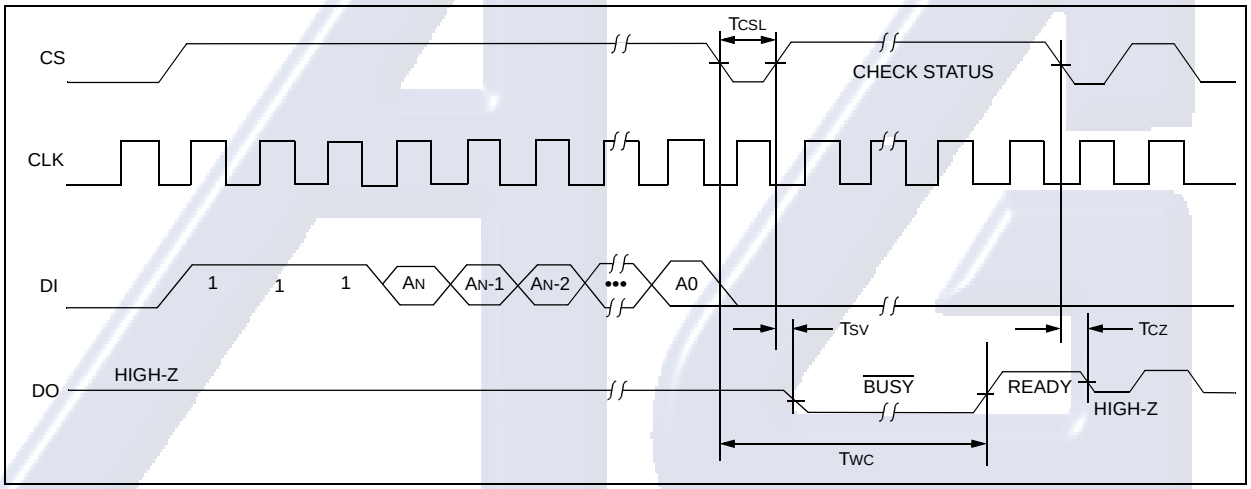
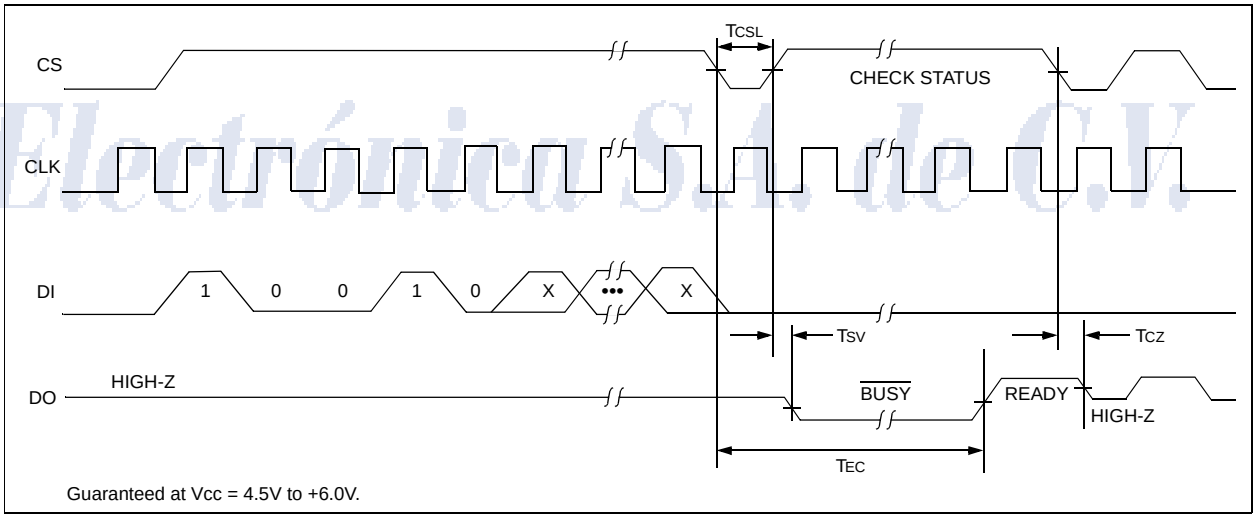


FIGURE 3-3: ERAL TIMING



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3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The 93LC66A/B powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWDS and EWEN instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93LC66A) or 16-bit (93LC66B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

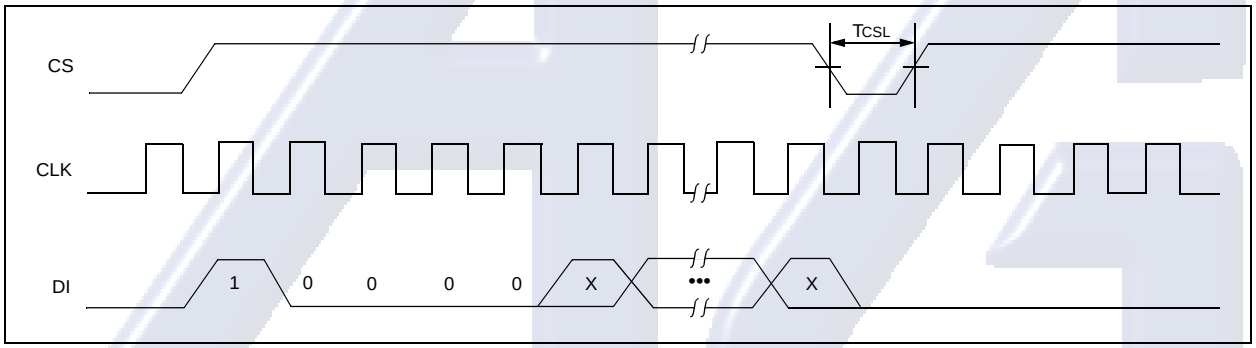


FIGURE 3-5: EWEN TIMING

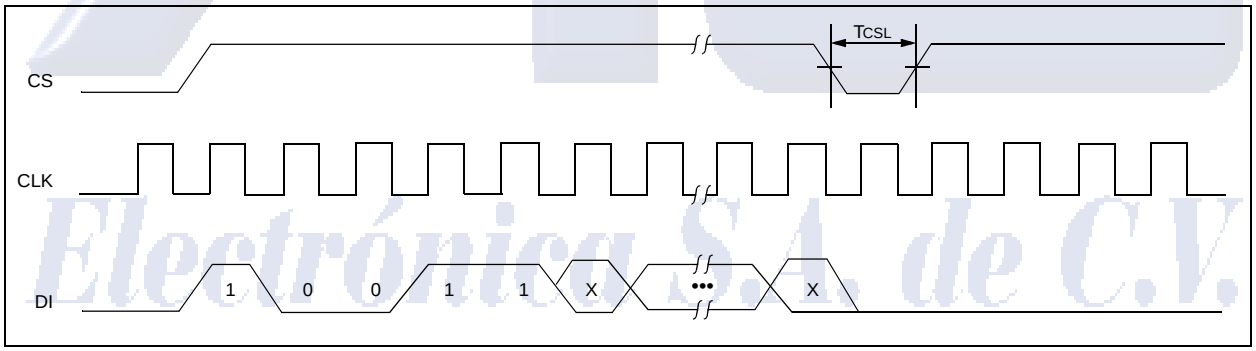
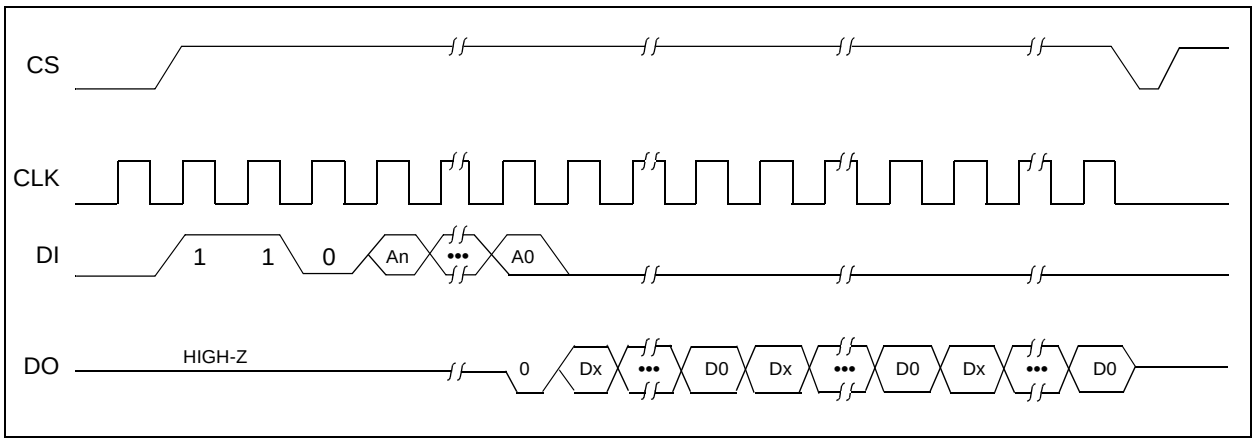


FIGURE 3-6: READ TIMING



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3.8 WRITE

The WRITE instruction is followed by 8 bits (93LC66A) or 16 bits (93LC66B) of data which are written into the specified address. After the last data bit is put on the DI pin, the falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

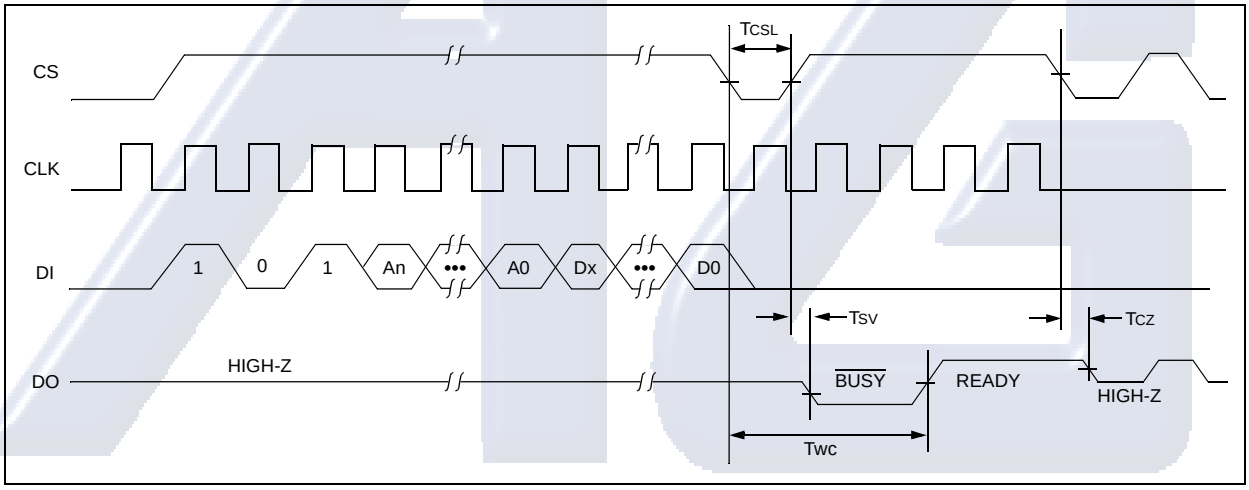
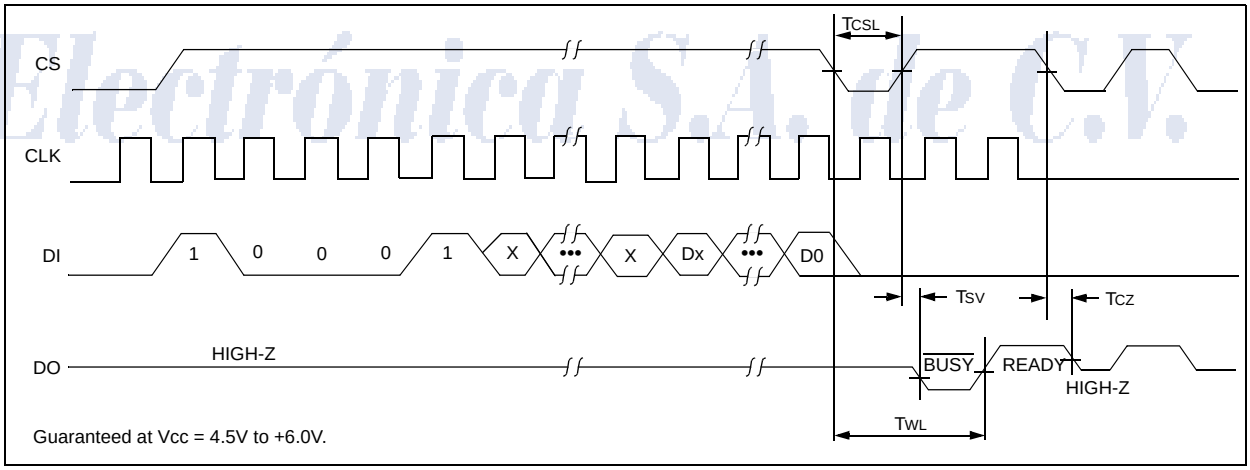


FIGURE 3-8: WRAL TIMING



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93LC66A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

93LC66A/B — /P

Package:

P	=	Plastic DIP (300 mil Body), 8-lead
SN	=	Plastic SOIC (150 mil Body), 8-lead
SM	=	Plastic SOIC (208 mil Body), 8-lead
ST	=	TSSOP, 8-lead

Temperature Range:

Blank	=	0°C to +70°C
I	=	-40°C to +85°C

Device:

93LC66A	4K Microwire Serial EEPROM (x8)
93LC66AT	4K Microwire Serial EEPROM (x8) Tape and Reel
93LC66AX	4K Microwire Serial EEPROM (x8) in alternate pinout (SN only)
93LC66AXT	4K Microwire Serial EEPROM (x8) in alternate pinout, Tape and Reel (SN only)
93LC66B	4K Microwire Serial EEPROM (x16)
93LC66BT	4K Microwire Serial EEPROM (x16) Tape and Reel
93LC66BX	4K Microwire Serial EEPROM (x16) in alternate pinout (SN only)
93LC66BXT	4K Microwire Serial EEPROM (x16) in alternate pinout, Tape and Reel (SN only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
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3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

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