

# Am27S02/27S03

64-Bit Inverting-Output Bipolar RAM

Am27S02/27S03

## DISTINCTIVE CHARACTERISTICS

- Fully decoded 16 word x 4-bit low-power Schottky RAMS
- Ultra-Fast "A" Version: Address access time 25ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open-collector outputs (Am27S02/02A) or with three-state outputs (Am27S03/03A)
- Pin-compatible replacements for 3101A, 74S289, (use Am27S02A/02); for 74S189, (use Am27S03A/03)

## GENERAL DESCRIPTION

The Am27S02/02A and Am27S03/03A are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select (CS) input and open collector OR tieable outputs (Am27S02/02A) or three-state outputs (Am27S03/03A). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

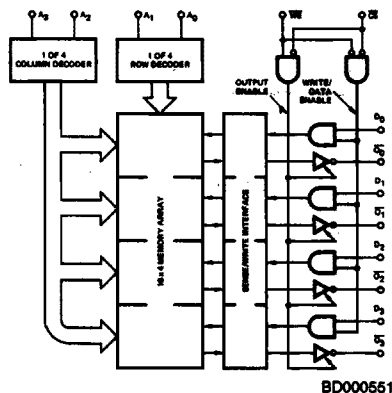
An active LOW Write line (WE) controls the writing/reading operation of the memory. When the chip select and write

lines are LOW the information on the four data inputs  $D_0$  to  $D_3$  is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs  $O_0$  to  $O_3$ .

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

## BLOCK DIAGRAM



## MODE SELECT TABLE

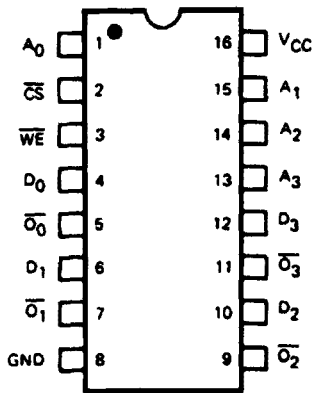
Input		Data Output Status $O_0 - O_3$	Mode
CS	WE		
L	L	Output Disabled	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

H = HIGH  
L = LOW  
X = Don't Care

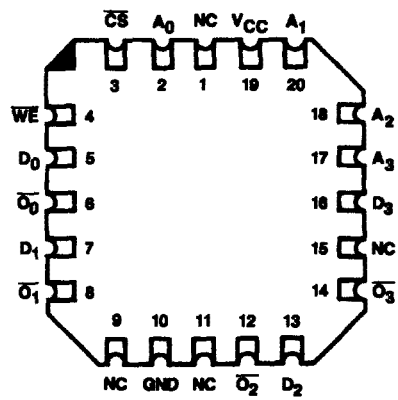
## PRODUCT SELECTOR GUIDE

Access Time	25 ns	30 ns	35 ns	50 ns
$I_{CC}$	100 mA	105 mA	100 mA	105 mA
Temperature Range	C	M	C	M
Open Collector	Am27S02A	Am27S02A	Am27S02	Am27S02
Three-State	Am27S03A	Am27S03A	Am27S03	Am27S03

# CONNECTION DIAGRAM Top View



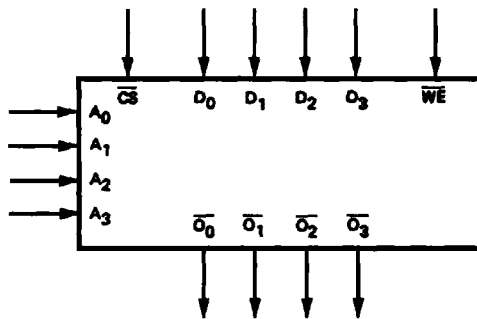
CD000831



CD000891

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



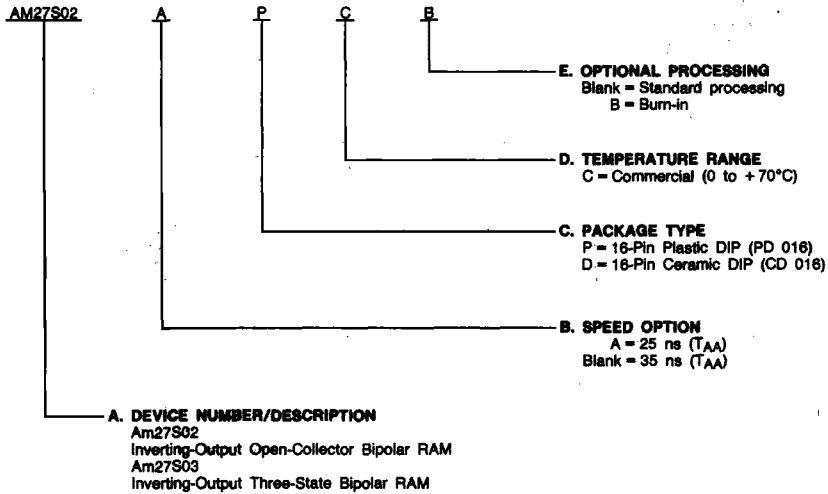
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## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number
- B. Speed Option (if applicable)
- C. Package Type
- D. Temperature Range
- E. Optional Processing



Valid Combinations	
AM27S02	PC, PCB, DC, DCB
AM27S02A	
AM27S03	
AM27S03A	

### Valid Combinations

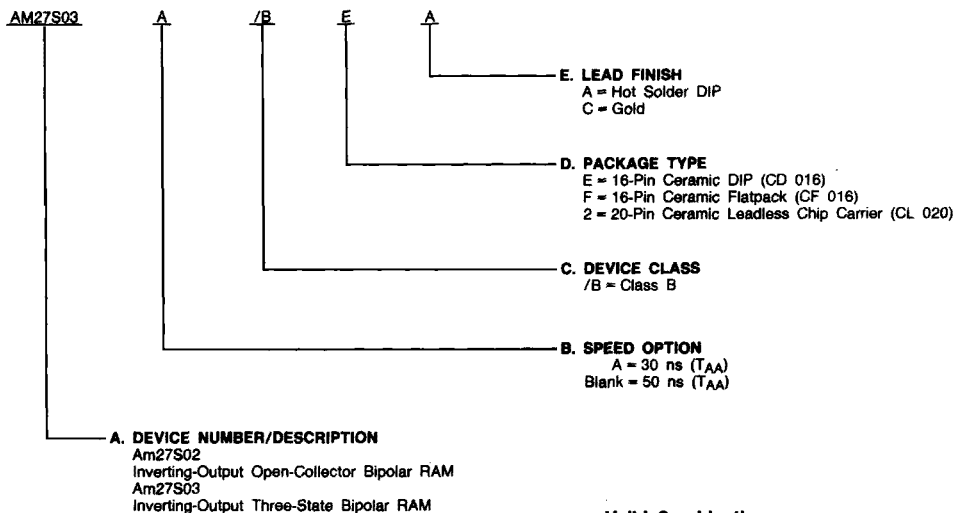
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



### Valid Combinations

Valid Combinations	
AM27S02	/BEA,
AM27S02A	/BFA,
AM27S03	/B2C
AM27S03A	

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55 to +125°C  
 Supply Voltage ..... -0.5 V to +7.0 V  
 DC Voltage Applied to Outputs ..... -0.5 V to +V<sub>CC</sub>Max.  
 DC Input Voltage ..... -0.5 V to +5.5 V  
 Output Current into Outputs ..... 20 mA  
 DC Input Current ..... -30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES (See Note 5)

Commercial (C) Devices

Temperature ..... 0 to +75°C  
 Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices

Temperature ..... -55 to +125°C  
 Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified\*

Parameter Symbol	Parameter Description	Test Conditions			27S02/3			Units
					Min.	Typ.	Max.	
V <sub>OH</sub> (Note 2)	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -5.2 mA I <sub>OH</sub> = -2.0 mA	COM'L MIL	2.4	3.2		Volts
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 20 mA			350 380	450 500	mV
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)		COM'L MIL	2.0 2.1			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 3)		COM'L MIL			0.8 0.8	
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.40 V	WE, D <sub>0</sub> -D <sub>3</sub> , A <sub>0</sub> -A <sub>3</sub> CS			-15 -30	-250 -250	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.7 V				0	10	μA
I <sub>SC</sub> (Note 2)	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0 V (Note 4)			-20	-45	-90	mA
I <sub>CC</sub>	Power Supply Current	All Inputs = GND V <sub>CC</sub> = Max.		COM'L MIL		75 75	100 105	
V <sub>CL</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA				-0.85	-1.2	Volts
I <sub>CEX</sub>	Output Leakage Current	V <sub>CS</sub> = V <sub>IH</sub> or V <sub>WE</sub> = V <sub>IL</sub> V <sub>OUT</sub> = 2.4 V, V <sub>CC</sub> = Max. V <sub>CS</sub> = V <sub>IH</sub> or V <sub>WE</sub> = V <sub>IL</sub> V <sub>OUT</sub> = 0.4 V, V <sub>CC</sub> = Max.		(Note 2)	-40	0		μA

Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.

2. This applies to three-state devices only.

3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

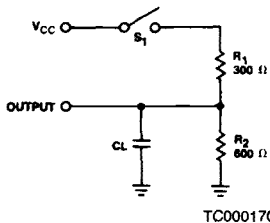
5. Operating specifications with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance Testing performance instantaneously where T<sub>A</sub> = T<sub>C</sub> = T<sub>J</sub>.

θ<sub>JA</sub> ≈ 50 °C/W (with moving air) for Ceramic DIP.

θ<sub>JA</sub> ≈ 10-17°C/W for flatpack and leadless chip carrier.

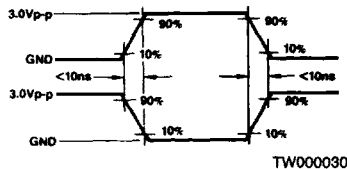
\*See the last page of this spec for Group A Subgroup Testing information.

# SWITCHING TEST CIRCUIT



TC000170

# SWITCHING TEST WAVEFORM



# KEY TO THE SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

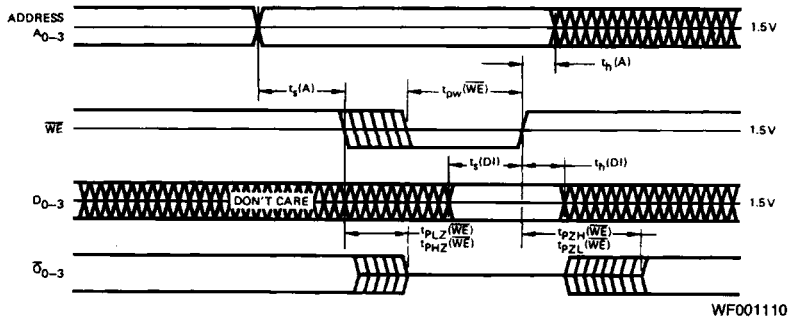
# SWITCHING CHARACTERISTICS over operating range unless otherwise specified\*

No.	Parameter Symbol	Parameter Description	Am27S02A/3A				Am27S02/3				Units
			A C Devices		A M Devices		STD C Devices		STD M Devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>PLH</sub> (A)	Delay from Address to Output		25		30		35		50	ns
2	t <sub>PHL</sub> (A)										
3	t <sub>PZH</sub> (CS)	Delay from Chip Select (LOW) to Active Output and Correct Data		15		20		17		25	ns
4	t <sub>PZL</sub> (CS)										
5	t <sub>PZH</sub> (WE)	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery- See Note 1)		20		25		35		40	ns
6	t <sub>PZL</sub> (WE)										
7	t <sub>s</sub> (A)	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
8	t <sub>h</sub> (A)	Hold Time Address (After Termination of Write)	0		0		0		0		ns
9	t <sub>s</sub> (DI)	Setup Time Data Input (Prior to Termination of Write)	20		25		25		25		ns
10	t <sub>h</sub> (DI)	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
11	t <sub>pw</sub> (WE)	MIN Write Enable Pulse Width to Insure Write	20		25		25		25		ns
12	t <sub>PHZ</sub> (CS)	Delay from Chip Select (HIGH) to inactive Output (HI-Z)		15		20		17		25	ns
13	t <sub>PLZ</sub> (CS)										
14	t <sub>PLZ</sub> (WE)	Delay from Write Enable (LOW) to inactive Output (HI-Z)		20		25		25		35	ns
15	t <sub>PHZ</sub> (WE)										

- Notes: 1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2.  $t_{PLH}(A)$  and  $t_{PHL}(A)$  are tested with  $S_1$  closed and  $C_L = 30$  pF with both input and output timing referenced to 1.5 V.
3. For open collector, all delays from Write Enable ( $\overline{WE}$ ) or Chip Select ( $\overline{CS}$ ) inputs to the Data Output ( $D_{OUT}$ ),  $t_{PLZ}(\overline{WE})$ ,  $t_{PLZ}(\overline{CS})$ ,  $t_{PZH}(\overline{WE})$  and  $t_{PZH}(\overline{CS})$  are measured with  $S_1$  closed and  $C_L = 30$  pF and with both the input and output timing referenced to 1.5 V.
4. For 3-state output,  $t_{PZH}(\overline{WE})$  and  $t_{PZH}(\overline{CS})$  are measured with  $S_1$  open,  $C_L = 30$  pF and with both the input and output timing referenced to 1.5 V.  $t_{PHZ}(\overline{WE})$  and  $t_{PHZ}(\overline{CS})$  are measured with  $S_1$  closed,  $C_L = 30$  pF and with both the input and output timing referenced to 1.5 V.  $t_{PLZ}(\overline{WE})$  and  $t_{PLZ}(\overline{CS})$  are measured with  $S_1$  open and  $C_L \leq 5$  pF and are measured between the 1.5 V level on the input to the  $V_{OH} - 500$  mV level on the output.  $t_{PLZ}(\overline{WE})$  and  $t_{PLZ}(\overline{CS})$  are measured with  $S_1$  closed and  $C_L \leq 5$  pF and are measured between the 1.5 V level on the input and the  $V_{OL} + 500$  mV level on the output.

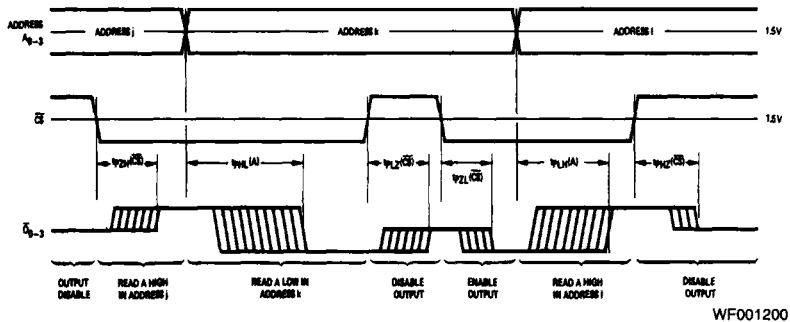
\*See the last page of this spec for Group A Subgroup Testing information.

## SWITCHING WAVEFORMS



### Write Mode

**Write Cycle Timing.** The cycle is initiated by an address change. After  $t_s(A)$  min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse,  $t_h(A)$  min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03A/03) while the write enable is (WE) LOW.



### Read Mode

**Switching delays from address and chip select inputs to the data output.** For the Am27S03A/03 disabled output is "OFF", represented by a single center line. For the Am27S02A/02, a disabled output is HIGH.

## GROUP A SUBGROUP TESTING

### DC CHARACTERISTICS

Parameter Symbol	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub>	1, 2, 3
I <sub>IH</sub>	1, 2, 3
I <sub>IH</sub>	1, 2, 3
I <sub>SC</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
V <sub>CL</sub>	1, 2, 3
I <sub>CEX</sub>	1, 2, 3

### SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t <sub>PLH</sub> (A)	9, 10, 11	9	t <sub>s</sub> (DI)	9, 10, 11
2	t <sub>PHL</sub> (A)				
3	t <sub>PZH</sub> ( $\overline{CS}$ )	9, 10, 11	10	t <sub>h</sub> (DI)	9, 10, 11
4	t <sub>PZL</sub> ( $\overline{CS}$ )				
5	t <sub>PZH</sub> ( $\overline{WE}$ )	9, 10, 11	11	t <sub>pw</sub> ( $\overline{WE}$ )	9, 10, 11
6	t <sub>PZL</sub> ( $\overline{WE}$ )				
7	t <sub>s</sub> (A)	9, 10, 11	12	t <sub>PHZ</sub> ( $\overline{CS}$ )	9, 10, 11
			13	t <sub>PLZ</sub> ( $\overline{CS}$ )	
8	t <sub>h</sub> (A)	9, 10, 11	14	t <sub>PLZ</sub> ( $\overline{WE}$ )	9, 10, 11
			15	t <sub>PHZ</sub> ( $\overline{WE}$ )	