VOICE OTP IC

aP89682K – 682sec

aP89341K – 341sec

aP89170K – 170sec

aP89085K – 85sec

APLUS INTEGRATED CIRCUITS INC.

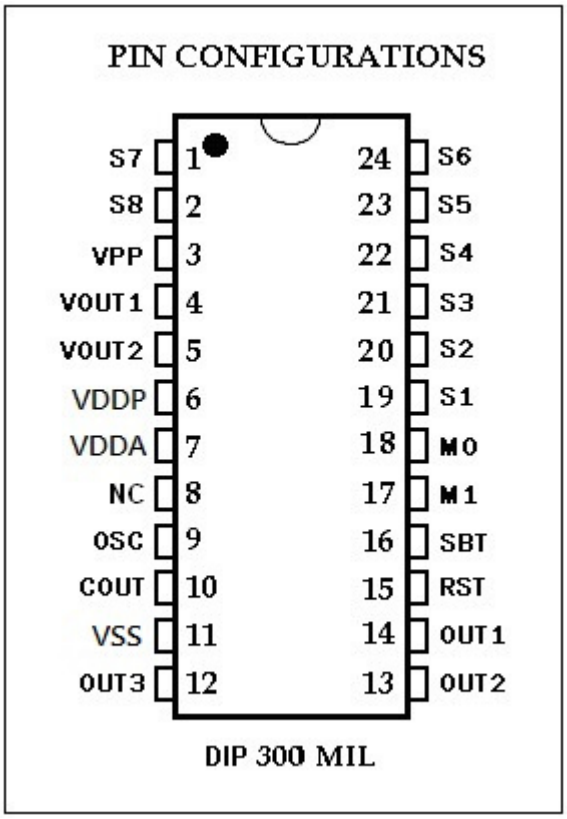
▪ FEATURES :

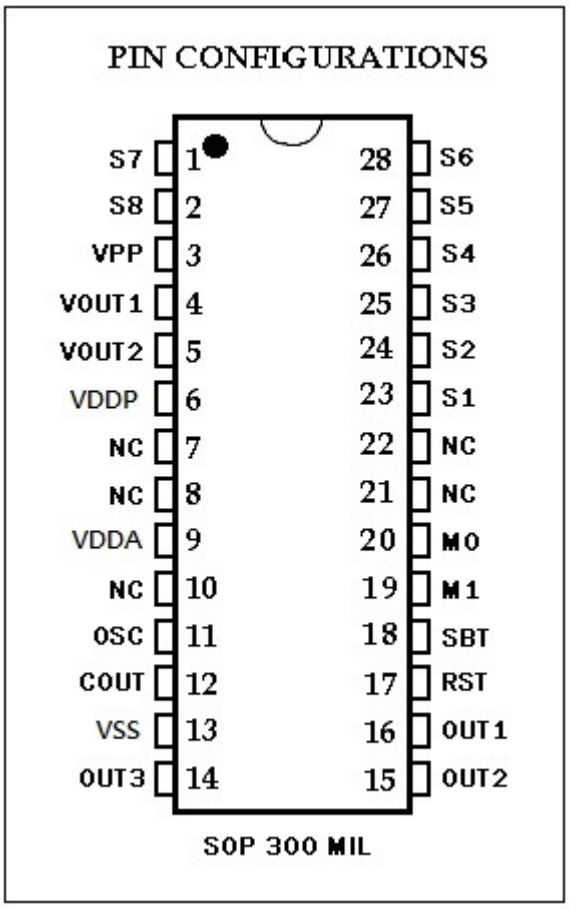
- Standard CMOS process.
- Embedded 16M/8M/4M/2M EPROM.
- **682/341/170/85** sec Voice Length at 6KHz sampling and 4-bits ADPCM compression.
- Maximum 1024 voice groups.
- Maximum 48KHz sample rate.
- Combination of voice blocks to extend playback duration.
- User selectable PCM16 or ULAW8 or PCM8 or ADPCM4 data compression.
- 7 triggering modes are available :
  - Key Mode :
    S1 ~ S8 to trigger up to 57 voice groups; Power on play function.
  - SBT Mode :
    SBT to trigger up to 1024 voice groups sequentially; Power on play function.
  - CPU Parallel Mode :
    S[8:1] services as 8-bits address to trigger up to 256 voice groups.
    with SBT goes HIGH to strobe the address bits.
  - SPI Mode : CSB , SCK , DI.
    3 wire address control up to 1024 voice groups.
  - I2C Mode : SCK , DI.
    2 wire address control up to 1024 voice groups.
  - MP3 Mode :
    S1:Backward , S2: Forward , S3: (Pause/Stop) , S4:Reset ,
    SBT: (Play/Pause) or (Play/Stop) Trigger up to 1024 voice groups.
  - aP89 Mode – Function setting similar aP89341/aP89170/aP89085.
- Voice Group Trigger Options: Edge / Level; Hold / Unholdable; Retrigger / Non-retrigger.
- Optional 16ms or 65us selectable debounce time.
- RST pin set HIGH to stop the playback at once.
- LVD (Low voltage detect).
- Programmable outputs pin out1,out2,out3 :
  for busy-H , busy-L , stop-H , stop-L , prog busy-H , prog busy-L , Load,
  LED flash (LED high active) , ~LED flash (LED low active).
- Three kind oscillator: Internal-Rosc、External-Rosc、Crystal.
- 2V – 5V single power supply and < 5uA low stand-by current.
- 16/8/4 level volume control setting available.
- 16 bits audio out.
- PWM Vout1 and Vout2 drive speaker directly.
- D/A COUT pin drives speaker through an external BJT or audio AMP.
- Development System support for voice compilation.

▪ DESCRIPTION :

aP89682K/341K/170K/085K series high performance Voice OTP is fabricated with Standard CMOS process with embedded 16M/8M/4M/2M bits EPROM. It can store up to 682/341/170/85 sec voice message with 4-bits ADPCM compression at 6KHz sampling rate. 16-bits PCM、8-bits PCM and 8-bits ULAW at (4K to 48K sample rate) is also available for user selecting.

User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 16-bits current mode DAC output and 14-bits PWM direct speaker driving output minimize the number of external components. PC controlled programmer and developing software are available.





- **PIN NAMES :**

PIN (24-pin)	Playback Mode	OTP Program Mode	Description
1	S7		Trigger pin (I/O pin with internal pull-down).
2	S8		Trigger pin (I/O pin with internal pull-down).
3	VPP	VPP	Supply ground.
4	VOUT1		PWM output to drive speaker directly.
5	VOUT2		PWM output to drive speaker directly.
6	VDDP	VDDP	Supply voltage.
7	VDDA	VDDA	Analog supply voltage.
8	NC		
9	OSC		Oscillator input.
10	COUT		DAC current output.
11	VSS	VSS	Supply ground.
12	OUT3		Programmable output (I/O pin).
13	OUT2		Programmable output (I/O pin).
14	OUT1		Programmable output (I/O pin).
15	RST	RST	Reset pin (input pin with internal pull-down).
16	SBT	SBT	Trigger pin (I/O pin with internal pull-down).
17	M1		Mode select pin 1 (input with internal pull-down).
18	M0		Mode select pin 0 (input with internal pull-down).
19 ~ 24	S1~S6	S2、S3	Trigger pin (I/O pin with internal pull-down).

▪ PIN DESCRIPTIONS :

• S1 ~ S8 :

Input Trigger Pins:
- In Key Mode : S1 to S8 is used to trigger 57 Voice groups.
- In CPU Parallel Mode : this pin low to high [Latch] the address at S1(lsb) to S8(msb) and starts the voice playback.
- In SPI Mode :
  S1 is Chip Select (CSB) pin to initiate the command input.
  S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip.
  S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In I2C Mode :
  S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip.
  S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In MP3 Mode :
  S1:Backward. S2:Forward. S3:(Pause/Stop). S4:Reset.

- In aP89 Mode : similar with APLUS 1st Generation OTP IC. (aP89341/aP89170/aP89085) usage.

• SBT :

Input Trigger Pin:
- In SBT Mode :This pin is trigger pin to play Voice Groups one time or looping sequentially up to 1024 Voice Groups.
- In CPU Parallel Mode : This pin is used as address strobe to latch the Voice Group address input at S1 to S8 and starts the voice playback.
- In MP3 Mode : This pin is (Play/Pause) or (Play/Stop).

• VDDP and VDDA :

Power Supply Pins: These two pins must be connected to the positive power supply.

• VSS :

Power Ground Pins: VSS and VPP pins must be connected together to the power ground during voice playback.
In circuit program: VSS and VPP pins must be separated to the power ground. Connect resistor between power ground and VPP.

• M0 and M1 :

In Key Mode、SBT Mode、CPU Parallel Mode、MP3 Mode、SPI Mode、and I2C Mode ,
M0 and M1 can be used for Crystal oscillator or volume control.

In aP89 Mode Operating Mode Setting Pins:
- M1=0, M0=0 set the chip into Key Trigger Mode.
- M1=0, M0=1 set the chip into CPU Parallel Command Mode.
- M1=1, M0=0 set the chip into CPU Serial Command Mode.

• VOUT1 and VOUT2 :

14-bits PWM output pins which can drive speaker and buzzer directly for voice playback.

• OSC :

During voice playback, an external resistor is connected between this pin and the VDD pin to set the sampling frequency. Or keep OSC floating if choosing INT-Rosc.
Note : External resistor is 68K Ω.

- **VPP :**

During voice playback, this pin and VSS must be connected together to the power ground.
In Circuit Program : This pin is connected to a separate 8.5V power supply voltage for OTP programming. Connect resistor between power ground and VPP.
Note : Resistor is 10K Ω.

- **OUT1, OUT2 and OUT3 :**

OUT1,OUT2 and OUT3 can select output function as below :

1. Busy- H : When voice is playing, output high level signal.
2. Busy- L : Inverted output of Busy- H.
3. LED- Flash : When voice is playing, output LED flash pulse.
4. ~LED- Flash : Inverted output of LED- Flash.
5. Stop- H : When voice plays finished, output stop pulse.
6. Stop- L : Inverted output of Stop- H.
7. Load : After load voice data to buffer success, output logic high signal.
8. Prog-Busy - H : When voice of Prog-Busy set 1, high pulse output.
   When voice of Prog-Busy set 0, low pulse output.
9. Prog-Busy - L : Inverted output of Prog-Busy - H.

- **COUT :**

16-bits current mode DAC output for voice playback.

- **RST :**

Chip reset in playback mode.
External reset pull high a capacitor if used internal reset not. capacitor :100nF

▪ VOICE SECTION COMBINATIONS :

Voice files created by the PC base developing system are stored in the built-in EPROM of the aP89682K/341K/170K/085K chip as a number of fixed length Voice Blocks. Voice Blocks are then selected and grouped into Voice Groups for playback. Up to 1024 Voice Groups are allowed. A Voice Blocks Table is used to store the information of combinations of Voice Blocks and then group them together to form Voice Group.

Chip	aP89682K	aP89341K	aP89170K	aP89085K
Memory size	16M bits	8M bits	4M bits	2M bits
Max no. of Voice Block	2016	2016	2016	2016
Max. no. of Voice Group	1024	1024	1024	1024
Voice Length (@ 6KHz 4-bit ADPCM)	682 sec	341 sec	170 sec	85 sec

▪ Example of Voice Block Combination :

Assume here we have three voice files, they are “How are You?”, Sound Effect and Music. Each of the voice file is divided into a number of fixed length Voice Block and stored into the memory.
Voice block :

B1 = “How”	B2 = ”are”	B3 = ”You”
B4 = Sound Effect	B5 = Music1	B6 = Music2

Voice Blocks are grouped together using Voice Table to form Voice Group for playback:

Group no.	Voice Group contents	Voice Table Entries
Group 1	“How are You?”	B1+B2+B3
Group 2	Sound Effect + “How are You?”	B4+ B1+B2+B3
Group 3	“How are You?” + Music1	B1+B2+B3+B5
Group 4	Music2	B6

▪ Voice Data Compression :

Voice File data is stored in the on-chip EPROM as either 4-bits ADPCM or 8-bits PCM/ ULAW format or 16-bits PCM format. Voice data are stored as 16-bits PCM forma is without compression. The voice playback quality is best. Voice data stored as 4-bits ADPCM or 8-bits PCM/ ULAW provide 4:2 data compression to save memory space. But voice playback quality with be lower than 16-bits PCM format.

▪ Group Options :

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger.
- Unholdable or Holdable option.
- Re-triggerable or Non-retriggerable option.
- Stop pulse disable or enable.

Fig.1 to Fig.6 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

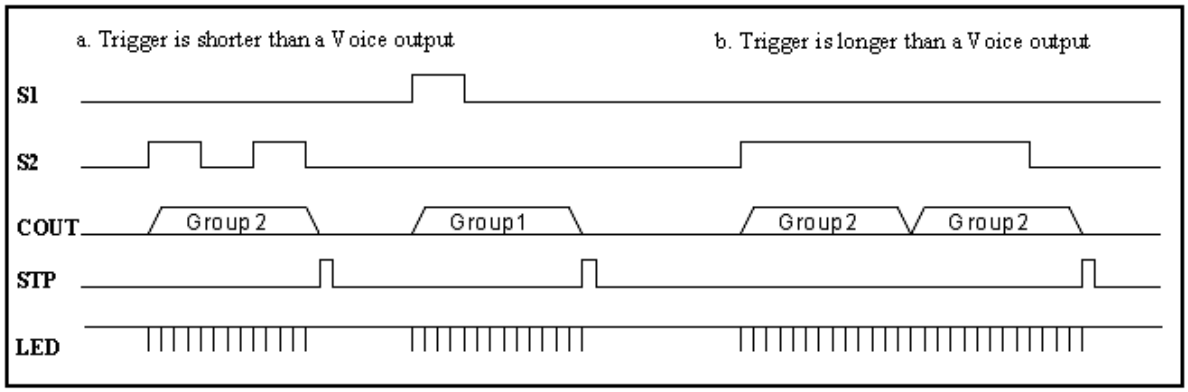


Fig.1 Level, Unholdable, Non-retriggerable

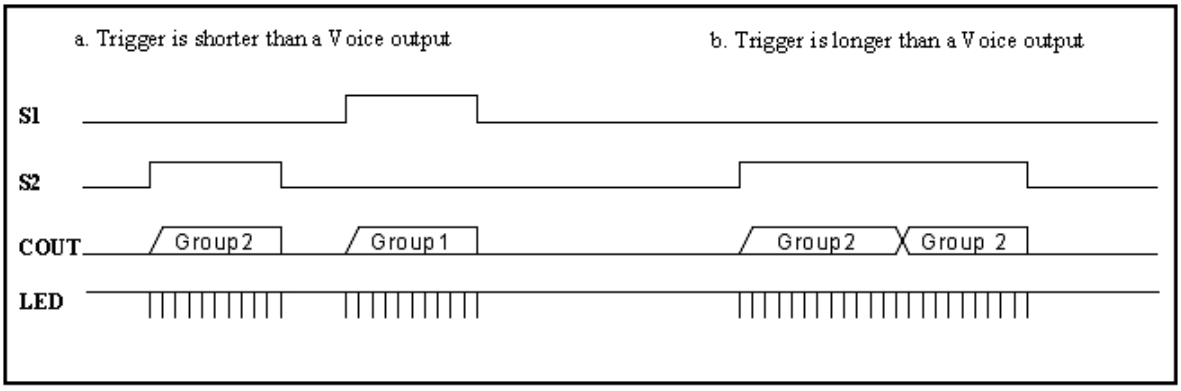


Fig. 2 Level Holdable

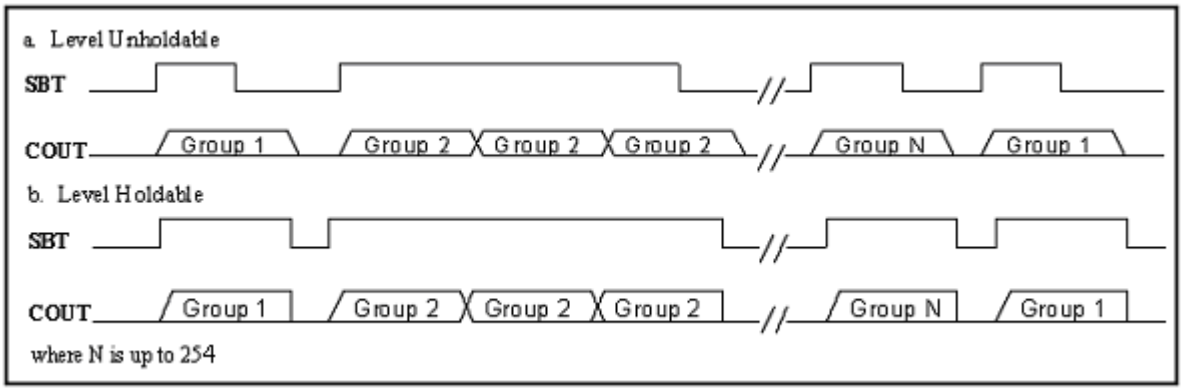


Fig. 3 SBT sequential trigger with Level Holdable and Unholdable

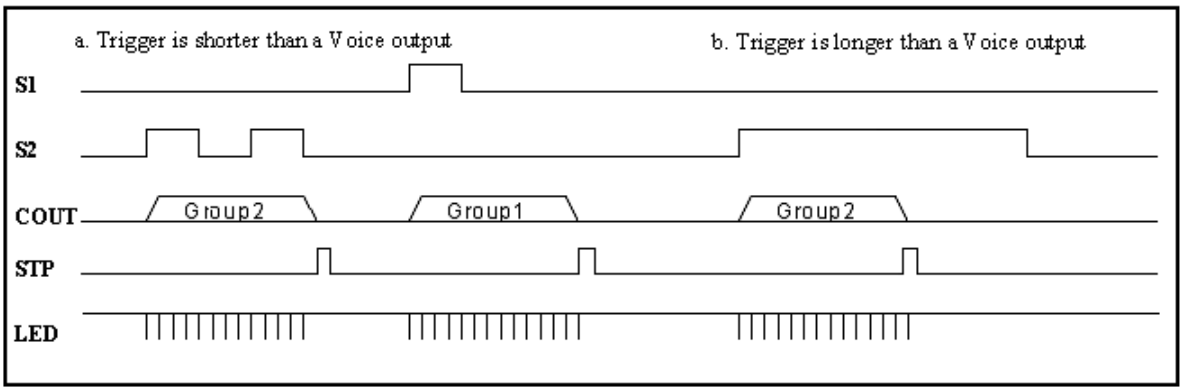


Fig. 4 Edge, Unholdable, Non-retrigger

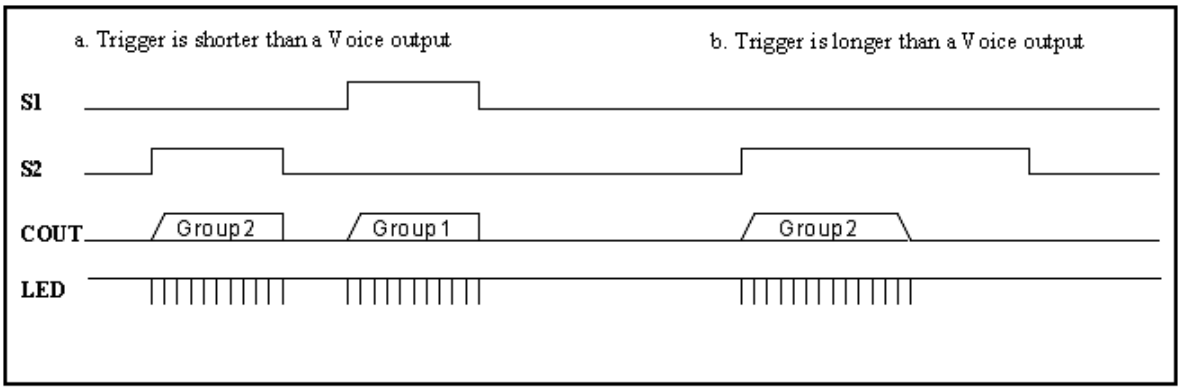


Fig. 5 Edge, Holdable

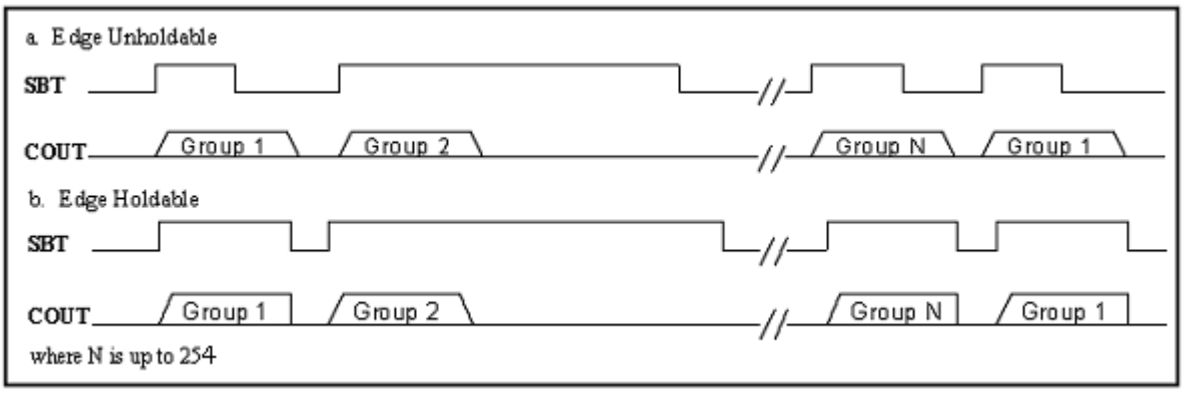


Fig. 6 SBT sequential trigger with Edge Holdable and Unholdable

▪ TRIGGER MODES :

There are seven trigger modes available for aP89682K/341K/170K/085K series.

- Key Mode.
- SBT Mode.
- CPU Parallel Mode.
- SPI Mode.
- I2C Mode.
- MP3 Mode.
- aP89 Mode.

Key Mode :

With this trigger mode, the beginning 57 Voice Groups are triggered by setting S1 to S8 to HIGH or LOW in different combinations. Each Voice Group can have its only independent trigger options (See Fig. 1,2,4 and 5 for trigger options definition).

The setting of S1 to S8 for triggering the 1st to the 57nd Voice Groups are as follow:

Voice Group	S1	S2	S3	S4	S5	S6	S7	S8
SW1	HIGH	NC	NC	NC	NC	NC	NC	NC
SW2	NC	HIGH	NC	NC	NC	NC	NC	NC
SW3	NC	NC	HIGH	NC	NC	NC	NC	NC
SW4	NC	NC	NC	HIGH	NC	NC	NC	NC
SW5	NC	NC	NC	NC	HIGH	NC	NC	NC
SW6	NC	NC	NC	NC	NC	HIGH	NC	NC
SW7	NC	NC	NC	NC	NC	NC	HIGH	NC
SW8	NC	NC	NC	NC	NC	NC	NC	HIGH
SW9	HIGH	HIGH	NC	NC	NC	NC	NC	NC
SW10	NC	HIGH	HIGH	NC	NC	NC	NC	NC
SW11	NC	NC	HIGH	HIGH	NC	NC	NC	NC
SW12	NC	NC	NC	HIGH	HIGH	NC	NC	NC
SW13	NC	NC	NC	NC	HIGH	HIGH	NC	NC
SW14	NC	NC	NC	NC	NC	HIGH	HIGH	NC
SW15	NC	NC	NC	NC	NC	NC	HIGH	HIGH
SW16	HIGH	NC	NC	NC	NC	NC	NC	HIGH
SW17	HIGH	HIGH	HIGH	NC	NC	NC	NC	NC
SW18	NC	HIGH	HIGH	HIGH	NC	NC	NC	HIGH
SW19	NC	NC	HIGH	HIGH	HIGH	NC	NC	NC
SW20	NC	NC	NC	HIGH	HIGH	HIGH	NC	NC
SW21	NC	NC	NC	NC	HIGH	HIGH	HIGH	NC
SW22	NC	NC	NC	NC	NC	HIGH	HIGH	HIGH
SW23	HIGH	NC	NC	NC	NC	NC	HIGH	HIGH
SW24	HIGH	HIGH	NC	NC	NC	NC	NC	HIGH
SW25	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	NC
SW26	NC	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
SW27	NC	NC	HIGH	HIGH	HIGH	HIGH	NC	NC
SW28	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	NC
SW29	NC	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
SW30	HIGH	NC	NC	NC	NC	HIGH	HIGH	HIGH
SW31	HIGH	HIGH	NC	NC	NC	NC	HIGH	HIGH
SW32	HIGH	HIGH	HIGH	NC	NC	NC	NC	HIGH
SW33	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
SW34	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
SW35	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW36	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW37	HIGH	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
SW38	HIGH	HIGH	NC	NC	NC	HIGH	HIGH	HIGH
SW39	HIGH	HIGH	HIGH	NC	NC	NC	HIGH	HIGH
SW40	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	HIGH
SW41	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
SW42	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW43	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW44	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW45	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH
SW46	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH
SW47	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH
SW48	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH
SW49	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW50	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW51	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW52	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW53	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH

SW54	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH
SW55	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH
SW56	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH
SW57	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

★★★ Note: NC represents open or no connection

SBT Mode :

A maximum of 1024 Voice Groups are available. And can be triggered one by one sequentially with the SBT key (See Fig. 3 and 6).

CPU Parallel Mode :

In this mode, S8 to S1 serve as 8-bit addresses input for 256 Voice Groups with S8 represents the MSB and S1 represents LSB. After Group address is set and ready, setting the SBT input pin LOW to HIGH will [LATCH] and trigger the corresponding Voice Group to playback.

Trigger options defined in Fig. 1,2, 4 and 5 are valid for this mode.

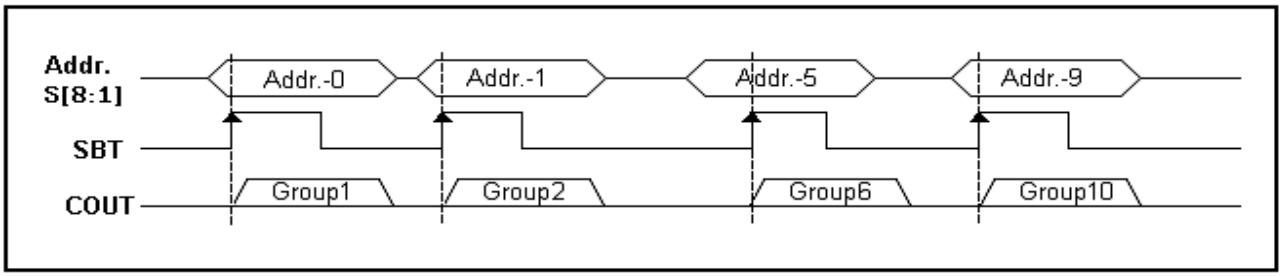


Fig. 7 CPU Parallel Trigger Mode

Note that SBT pin cannot be used as Single Button Sequential trigger in this mode. Instead, it acts as a Strobe input to clock-in the Voice Group address set at S8 to S1 into the chip.

Voice Groups are represented in Binary address format. For example:

[S8:S1] = 0000 0000 (00 hex) for Voice Group #1
[S8:S1] = 0000 0001 (01 hex) for Voice Group #2
• • •
[S8:S1] = 0000 1000 (08 hex) for Voice Group #9
• • •
[S8:S1] = 1000 1000 (88 hex) for Voice Group #137
• • •
[S8:S1] = 1111 1111 (FF hex) for Voice Group #256

CPU Serial Command Description :

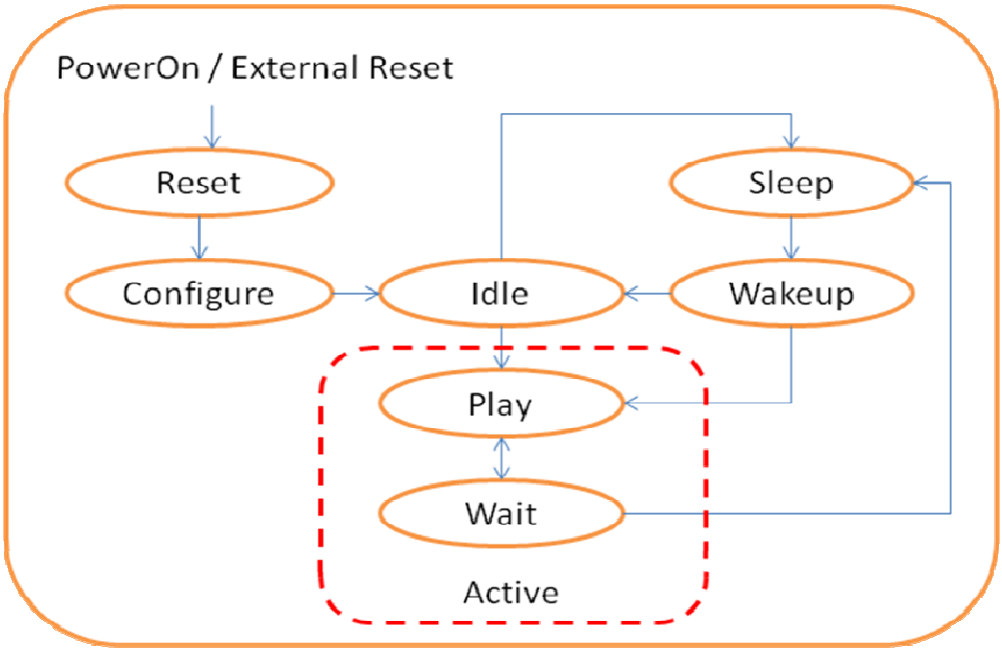
CPU Serial Command include **SPI Mode、I2C Mode** and **aP89 CPU Serial Command Mode.**
The command support to reference Fig.8 CPU Serial Command Description.

LOAD / PREFETCH	1. This command pre-load the next Voice Group Address into the address buffer. 2. The "Full/Load" signal will become HIHG once the Group Address is loaded. 3. The Voice Group will be played once the playing of the current Voice Group is finished. 4. The "Full/Load" signal will become LOW once the Voice Group is played and the address buffer is released and ready for next PREFECT action. 5. Using this command make sure there is **no gap** between each Voice Group.
PLAY	1. This command load the Voice Group Address into the address buffer. 2. The current Voice Group will be stopped and play the new one.
PU1	Power up the chip without ramp-up (suitable for PWM direct drive).
PU2	Power up the chip with ramp-up (suitable for COUT transistor drive).
PD1	Power down the chip without ramp-down (suitable for PWM direct drive).
PD2	Power down the chip with ramp-down (suitable for COUT transistor drive).
VOL	Set Volume index of volume Table.
VOL--	Decrease the volume index of volume Table.
VOL++	Increase the volume index of volume Table.
PAUSE	Pause the current Voice Group.
RESUME	Resume the current Voice Group.
STOUT	Device Status Output.

Fig. 8 CPU Serial Command Description

***Note:** If not selecting volume control function in CPU serial control, its default value would be fixed at "16 level". (In Compiler software: 23KW-Software-V2.5).

State Description :



State Name	Description
Reset	Include Power On Reset (typ 5us) and external reset (depends on the external reset circuit). All pins are input floating. **Serial Command inhibited**. After reset, state transfer to the " Configure " state.
Configure	Internal Chip Configuration. All pins are input floating. **Serial Command inhibited**. **(Max configure time = 2ms)** After configuration, state transfer to the "Idle" state.
Idle	State transfer to the **"Play"** state if **"active command"** received before timeout. After **time out** without active command, state transition to the **"Sleep"** State.
Play	Playing Voice Group include ramp. State transfer to the "Wait" state if nothing to be played.
Wait	Wait new Serial command and back to the play state without time limit. State transition to the **"Sleep"** state if **"de-active command"** received. Ramp down before transition to the sleep if the "PD2" command be accepted.
Sleep	State transition to the "Wakeup" state if selected by the host CPU. **(Wait sleep to wake up state time = 20us.)**
Wakeup	**Single command be buffered and wait to execute after wakeup state!!** **(Max wakeup time = 2ms).** State transition to the "Play" state if active command received else to the "Idle" state.

Fig. 9 State Description

*** Active commands are "Load", "Play", "PU1" and "PU2".
De-Active commands are "PD1" and "PD2".

In CPU Serial Command Control :

a. Using PU1/PU2 command first from de-active state.
Add 2ms delay after PU1/PU2 command is necessary.
b. Max "Output Delay of Busy/Full Signal" equal 2ms during active.
c. OUT2's select is different from the aP89xxx Series. (POUT)
Output select to reference PIN DESCRIPTIONS of OUT1、OUT2 and OUT3.

aP89 Mode :

This trigger mode is function setting similar with APLUS 1st Generation OTP IC (aP89341/aP89170/aP89085).

In aP89 Mode Operating Mode Setting:

M1=0, M0=0 set the chip into Key Trigger Mode.
It operates to reference Key Mode.

M1=0, M0=1 set the chip into CPU Parallel Command Mode.
It operates to reference CPU Parallel Mode.

M1=1, M0=0 set the chip into CPU Serial Command Mode.

The CPU serial command compatible with APLUS 1st Generation OTP IC.
It is controlled by command sent to it from the host CPU.S1 to S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S1 acts as CS (Chip Select) to initiate the command word input
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state(include play and ramp).
- OUT2 acts as OUT function to output user selected information.
- OUT3 acts as Load signal to indicate the Voice Group address buffer is full and waiting for play.

aP89Mode -CPU Serial Command Table [LSB First, Command Byte First]:

	D7	D6	D5	D4	D3	D2	D1	D0	G7	G6	G5	G4	G3	G2	G1	G0
PREFETCH	0	1	1	1	0	0	0	1	Voice Group Address Number							
PLAY	0	1	0	1	0	1	0	1	Voice Group Address Number							
PU1 w/o Ramp	1	1	0	0	0	1	0	1	None							
PU2 with Ramp	1	0	0	0	1	1	0	1	None							
PD1 w/o Ramp	1	1	1	0	0	0	0	1	None							
PD2 with Ramp	1	0	1	0	1	0	0	1	None							
VOL	1	0	1	1	0	0	1	0	0	0	0	0	VOL[3:0]			
VOL++	1	0	1	1	0	0	0	1	None							
VOL--	1	0	1	1	0	1	0	0	None							
PAUSE	0	0	1	1	1	0	0	1	None							
RESUME	0	0	0	1	1	1	0	1	None							

Fig. 10 aP89Mode CPU Serial Command Table

aP89Mode -CPU Serial Command Timing Diagram:

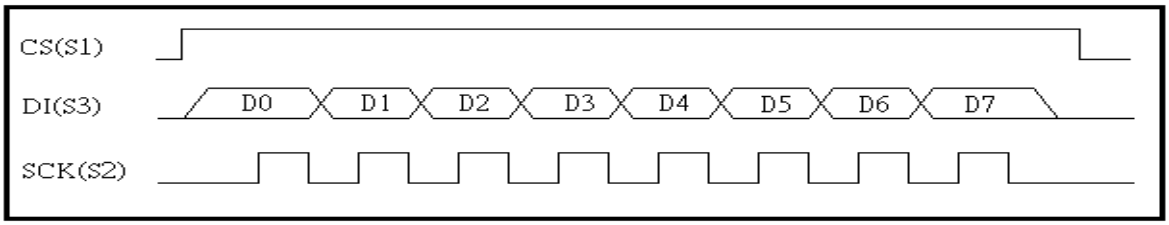


Fig.11(a) aP89Mode CPU Serial Command timing

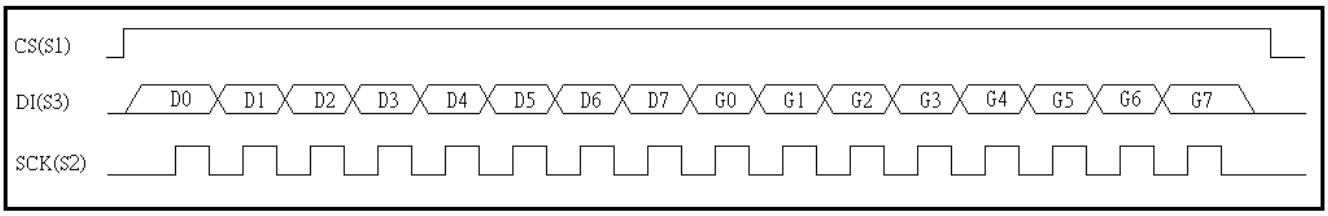


Fig.11(b) aP89Mode CPU Serial Command timing

* Data is latched at rising edge of SCK.

* aP89Mode CPU Serial Command function reference Fig. 8 CPU Serial Command Description.

Power up with RAMP-UP(PU2) or without RAMP-UP(PU1)

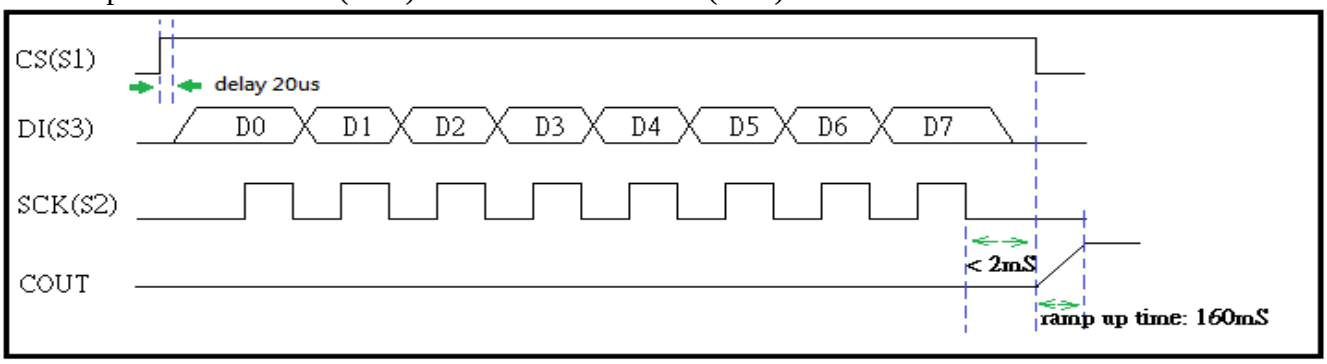


Fig. 12 Power-Up command timing

* Ramp up time : 160mS

Power down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1)

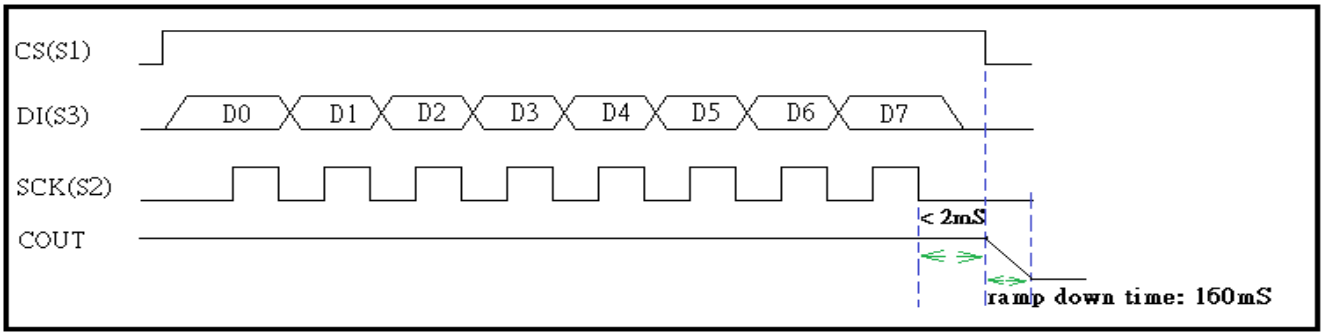


Fig. 13 Power-Down command timing

* Ramp down time : 160mS

(1). Prefetch Voice Group Address :
a. Command timing reference Fig.11(b) aP89Mode CPU Serial Command timing.
b. G7 to G0 total 8 bits to be the Group Address.
c. The OUT3 output (Load) will become logic high once the Group Address is successfully loaded.
d. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

(2). Play Voice Group Address :
a. Command timing reference Fig.11(b) aP89Mode CPU Serial Command timing.
b. G7 to G0 total 8 bits to be the Group Address.
c. Playing assign group address immediately.

(3). Power up with RAMP-UP(PU2) or without RAMP-UP(PU1) :
a. Command timing reference Fig.12 Power-up Command timing.
b. PU1 : will power-up the chip and set the VOUT to center value immediately and stay there.
c. PU2 : will power-up the chip and ramp-up COUT from bottom to center value and stay there.

(4).Power down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1) :
a. Command timing reference Fig.13 Power-down Command timing.
b. PDN1 will power-down the chip and set the VOUT data to bottom value immediately.
PDN1 will be executed correctly only if PU1 is executed before.
c. PDN2 will power-down the chip and ramp-down the COUT from its current to bottom value.
PDN2 will be executed correctly only if PU2 is executed before.

(5). Volume Set (VOL[3:0]) :
a. Command timing reference Fig.11(b) aP89Mode CPU Serial Command timing.
b. G3 to G0 total 4bits(0 ~ 15) set volume level (max : 0, min : 15), if volume level is 16.
c. G2 to G0 total 3bits(0 ~ 7) set volume level (max : 0, min : 7), if volume level is 8.
d. G1 to G0 total 2bits(0 ~ 3) set volume level (max : 0, min : 3), if volume level is 4.

(6).Volume + + (VOL++) :
a. Command timing reference Fig.11(a) aP89Mode CPU Serial Command timing.
b. Set volume level increase.

(7).Volume - - (VOL--) :
a. Command timing reference Fig.11(a) aP89Mode CPU Serial Command timing.
b. Set volume level decrease.

(8). Pause and Resume (PAUSE; RESUME) :
a. Command timing reference Fig.11(a) aP89Mode CPU Serial Command timing.
b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level. When Resume, the COUT data will continue at the current D/A data level.

SPI Mode :

This trigger mode is specially designed for simple CPU interface. The aP89682K/341K/170K/085K is controlled by command sent to it from the host CPU. S1 to S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S1 acts as CSB (Chip Select) to initiate the command word input.
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state(include play and ramp).
- OUT2 acts as OUT function to output user selected information.
- OUT3 acts as Load signal to indicate the Voice Group address buffer is full and waiting for play.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

SPI Command Table [MSB First] : Command input into the chip 16-bits data.

Command	D15	D14	D13	D12	D11	D10	D[9:0]
LOAD	1	0	0	1	0	1	Voice Group Address Number.
PLAY	1	0	0	1	1	0	Voice Group Address Number.
PU1 w/o Ramp	1	0	1	0	0	1	don't care.
PU2 with Ramp	1	0	1	0	1	0	don't care.
PD1 w/o Ramp	1	0	1	1	0	1	don't care.
PD2 with Ramp	1	0	1	1	1	0	don't care.
VOL	0	1	0	0	0	1	0 0 0 0 0 0 VOL[3:0]
VOL++	0	1	0	0	1	0	don't care.
VOL--	0	1	0	1	0	1	don't care.
PAUSE	0	1	1	0	0	1	don't care.
RESUME	0	1	1	0	1	0	don't care.

Fig. 14 SPI Command Table

SPI Command Timing Diagram:

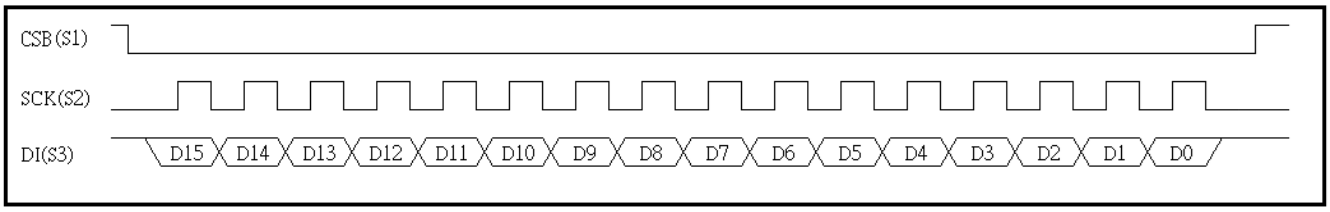


Fig.15 SPI Command timing

* Data is latched at rising edge of SCK.

* SPI Command function reference Fig. 8 CPU Serial Command Description.

Power up with RAMP-UP(PU2) or without RAMP-UP(PU1)

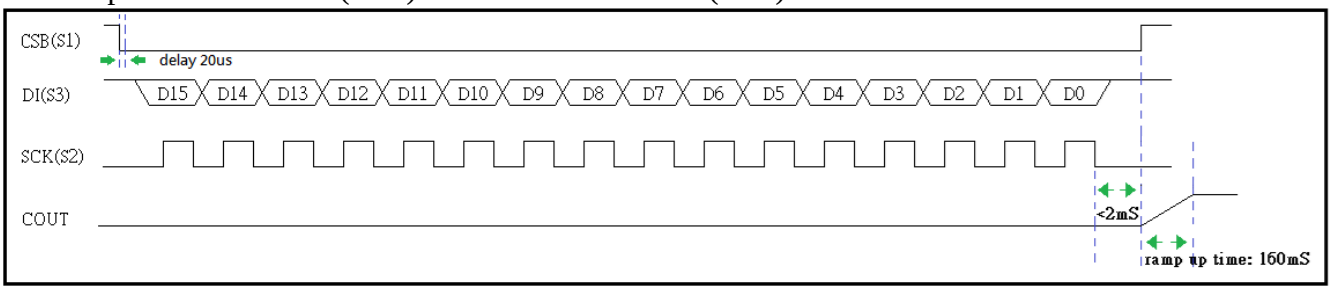


Fig. 16 Power-Up command timing

* Ramp up time : 160mS

Power down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1)

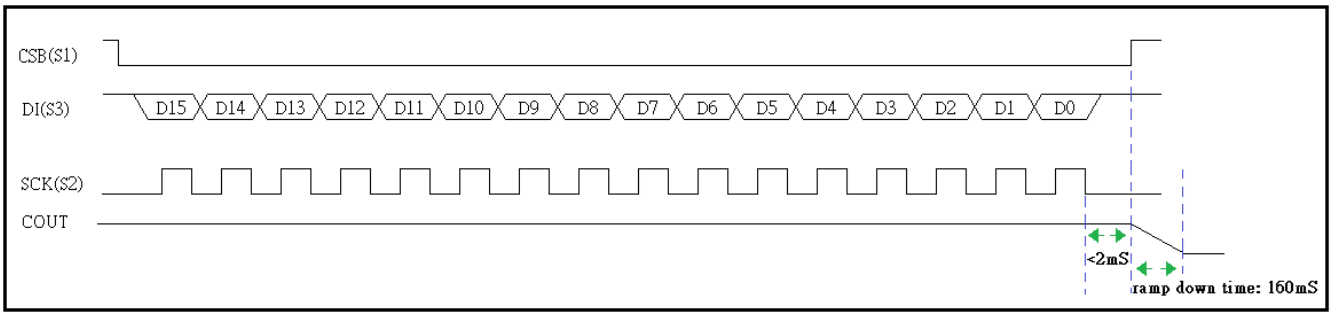


Fig. 17 Power-Down command timing

* Ramp down time : 160mS

(1). Load Voice Group Address :
a. Command timing reference Fig.15 SPI Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. The OUT3 output (Load) will become logic high once the Group Address is successfully loaded.
d. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

(2). Play Voice Group Address :
a. Command timing reference Fig.15 SPI Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. Playing assign group address immediately.

(3). Power up with RAMP-UP(PU2) or without RAMP-UP(PU1) :
a. Command timing reference Fig. 16 Power-Up command timing.
b. PU1 : will power-up the chip and set the VOUT to center value immediately and stay there.
c. PU2 : will power-up the chip and ramp-up COUT from bottom to center value and stay there.

(4). Power-down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1) :
a. Command timing reference Fig. 17 Power-Down command timing.
b. PDN1 will power-down the chip and set the VOUT data to bottom value immediately.
PDN1 will be executed correctly only if PU1 is executed before.
c. PDN2 will power-down the chip and ramp-down the COUT from its current to bottom value.
PDN2 will be executed correctly only if PU2 is executed before.

(5). Volume Set (VOL[3:0]) :
a. Command timing reference Fig.15 SPI Command timing.
b. D3 to D0 total 4bits(0 ~ 15) set volume level (max : 0, min : 15), if volume level is 16.
c. D2 to D0 total 3bits(0 ~ 7) set volume level (max : 0, min : 7), if volume level is 8.
d. D1 to D0 total 2bits(0 ~ 3) set volume level (max : 0, min : 3), if volume level is 4.

(6). Volume + + (VOL++) :
a. Command timing reference Fig.15 SPI Command timing.
b. Set volume level increase.

(7). Volume - - (VOL--) :
a. Command timing reference Fig.15 SPI Command timing.
b. Set volume level decrease.

(8). Pause and Resume (PAUSE; RESUME) :
a. Command timing reference Fig.15 SPI Command timing.
b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level. When Resume, the COUT data will continue at the current D/A data level.

I2C Mode :

This trigger mode is specially designed for simple CPU interface. The aP89682K/341K/170K/085K is controlled by command sent to it from the host CPU. S2 and S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state(include play and ramp).
- OUT2 acts as OUT function to output user selected information.
- OUT3 acts as Load signal to indicate the Voice Group address buffer is full and waiting for play.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

P.S. :
This mode named "I2C mode" in the document/software, but it's NOT compatible with standard I2C device(e.g. NOT implemented ACK, and no device/register address supported).

I2C Command Table [MSB First] : Command input into the chip 16-bits data.

Command	D15	D14	D13	D12	D11	D10	D[9:0]
LOAD	1	0	0	1	0	1	Voice Group Address Number.
PLAY	1	0	0	1	1	0	Voice Group Address Number.
PU1 w/o Ramp	1	0	1	0	0	1	don't care.
PU2 with Ramp	1	0	1	0	1	0	don't care.
PD1 w/o Ramp	1	0	1	1	0	1	don't care.
PD2 with Ramp	1	0	1	1	1	0	don't care.
VOL	0	1	0	0	0	1	0 0 0 0 0 0 VOL[3:0]
VOL++	0	1	0	0	1	0	don't care.
VOL--	0	1	0	1	0	1	don't care.
PAUSE	0	1	1	0	0	1	don't care.
RESUME	0	1	1	0	1	0	don't care.

Fig. 18 I2C Command Table

I2C Command Timing Diagram:

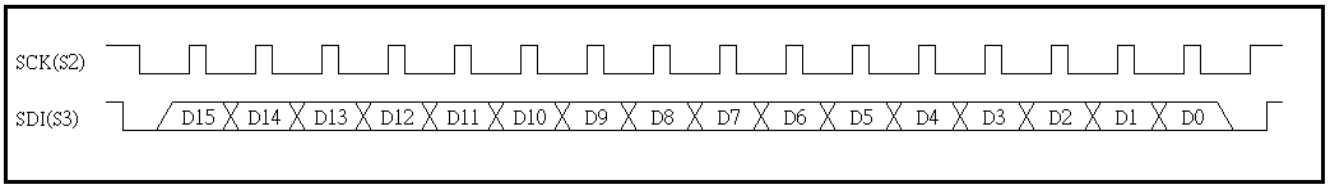


Fig.19 I2C Command timing

* The data bit only can be changed in SCK low level , but it has to be latched before rising edge of SCK.

* I2C Command function reference Fig. 8 CPU Serial Command Description.

Power up with RAMP-UP(PU2) or without RAMP-UP(PU1)

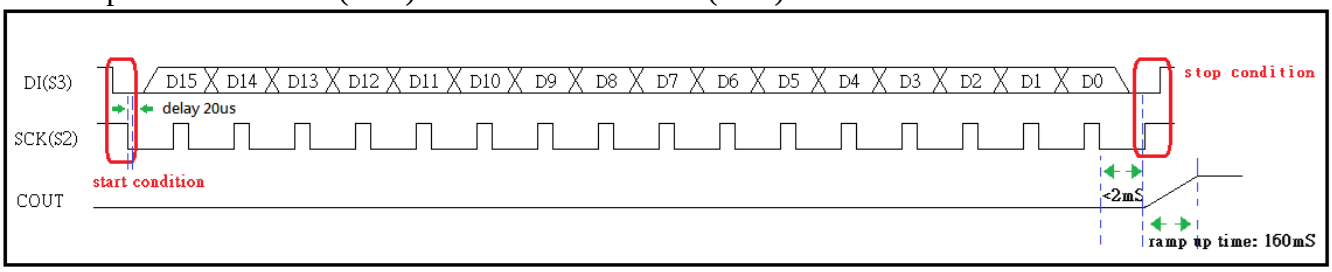


Fig. 20 Power-Up command timing

* Ramp up time : 160mS

Add stop condition after power on and internal chip configuration time finish.
In Power up command : After start condition signal, add delay time more than 300us to wake up device.

Power-down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1)

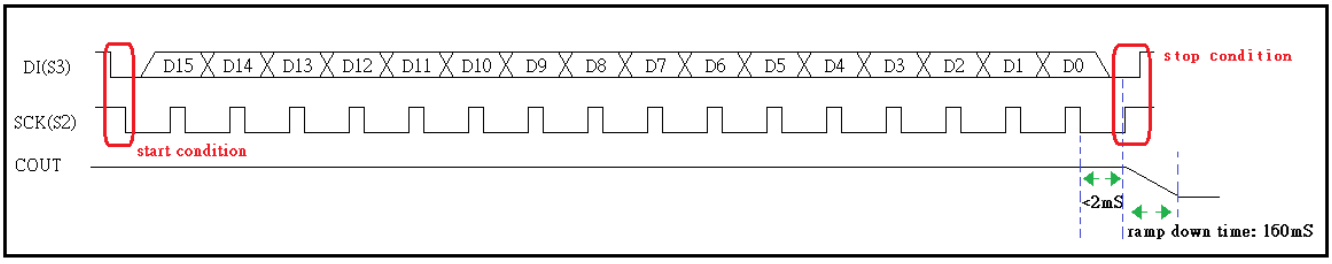


Fig. 21 Power-Down command timing

* Ramp down time : 160mS

(1). Load Voice Group Address :
a. Command timing reference Fig.19 I2C Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. The OUT3 output (Load) will become logic high once the Group Address is successfully loaded.
d. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

(2). Play Voice Group Address :
a. Command timing reference Fig.19 I2C Command timing.
b. D9 to D0 total 10 bits to be the Group Address.
c. Playing assign group address immediately.

(3). Power up with RAMP-UP(PU2) or without RAMP-UP(PU1) :
a. Command timing reference Fig. 20 Power-Up command timing.
b. PU1 : will power-up the chip and set the VOUT to center value immediately and stay there.
c. PU2 : will power-up the chip and ramp-up COUT from bottom to center value and stay there.

(4). Power-down with RAMP-DOWN(PD2) or without RAMP-DOWN (PD1) :
a. Command timing reference Fig. 21 Power-Down command timing.
b. PDN1 will power-down the chip and set the VOUT data to bottom value immediately.
PDN1 will be executed correctly only if PU1 is executed before.
c. PDN2 will power-down the chip and ramp-down the COUT from its current to bottom value.
PDN2 will be executed correctly only if PU2 is executed before.

(5). Volume Set (VOL[3:0]) :
a. Command timing reference Fig.19 I2C Command timing.
b. D3 to D0 total 4bits(0 ~ 15) set volume level (max : 0, min : 15), if volume level is 16.
c. D2 to D0 total 3bits(0 ~ 7) set volume level (max : 0, min : 7), if volume level is 8.
d. D1 to D0 total 2bits(0 ~ 3) set volume level (max : 0, min : 3), if volume level is 4.

(6). Volume + + (VOL++) :
a. Command timing reference Fig.19 I2C Command timing.
b. Set volume level increase.

(7). Volume - - (VOL--) :
a. Command timing reference Fig.19 I2C Command timing.
b. Set volume level decrease.

(8). Pause and Resume (PAUSE; RESUME) :
a. Command timing reference Fig.19 I2C Command timing.
b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level. When Resume, the COUT data will continue at the current D/A data level.

MP3 Mode :

This trigger mode is specially designed for simple MP3 function.

User can start to Play or Pause the voice by SBT pin, and Backward or Forward play by S1 pin or S2 pin, up to 1024 Voice Sections.

- SBT acts as (play/pause) or (play/stop).
- S1 acts as backward.
- S2 act as forward.
- S3 acts as stop (SBT = play/pause) or S3 acts as pause (SBT = play/stop).
- S4 act as reset.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

Option :

SPI Mode and I2C Mode are Pin S4 as data output (DO)using.
DO (Pin S4) as output from the chip to the host CPU for feedback response.

DO(Pin S4) Output the status bits :

Status	Description
S [15:9]	Reserved.
S [8]	**STO_TAG.**
S [7]	**STO_BUSYB.**
S [6]	**STO_FULLB / STO_EMPTY.**
S [5]	Reserved.
S [4]	Reserved.
S [3]	Reserved.
S [2]	**STO_VALIDB.**
S [1]	**STO_PARITY.**
S [0]	**STO_TAG.**

Fig. 22 SPI Output Status Table

S [15:9] : Reserved.

S [8] : STO_TAG : When received valid command the bit toggle.

S [7] : STO_BUSYB : When voice is playing the bit indicate 0 otherwise 1.

S [6] : STO_FULLB/STO_EMPTY : If voice group is waiting to be played ,the bit indicate 0 otherwise 1.

S [5:3] : Reserved.

S [2] : STO_VALIDB : If the last serial command is valid the bit indicate 0 otherwise 1.

S [1] : STO_PARITY : If digit 1 in group address[D9~D0] total are odd numbers, the bit indicate 0 otherwise 1.

S [0] : STO_TAG : When received valid command the bit toggle.

SPI Mode :

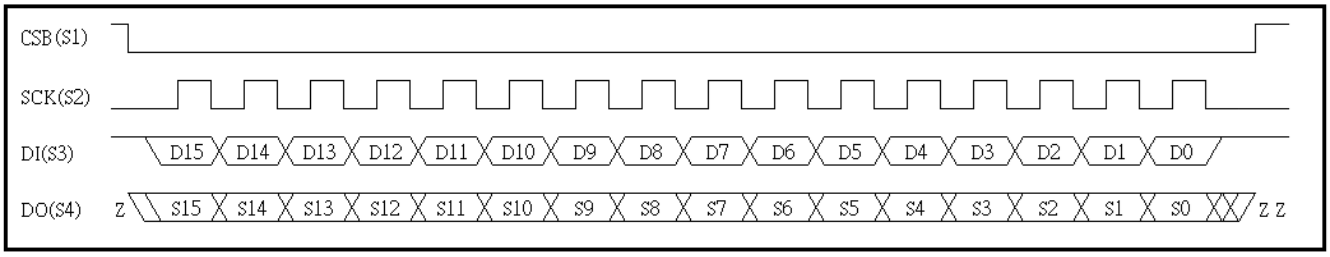


Fig. 23 SPI Data Output Command timing

* Data output to be changed at falling edge of SCK.

SPI TIMING WAVEFORMS

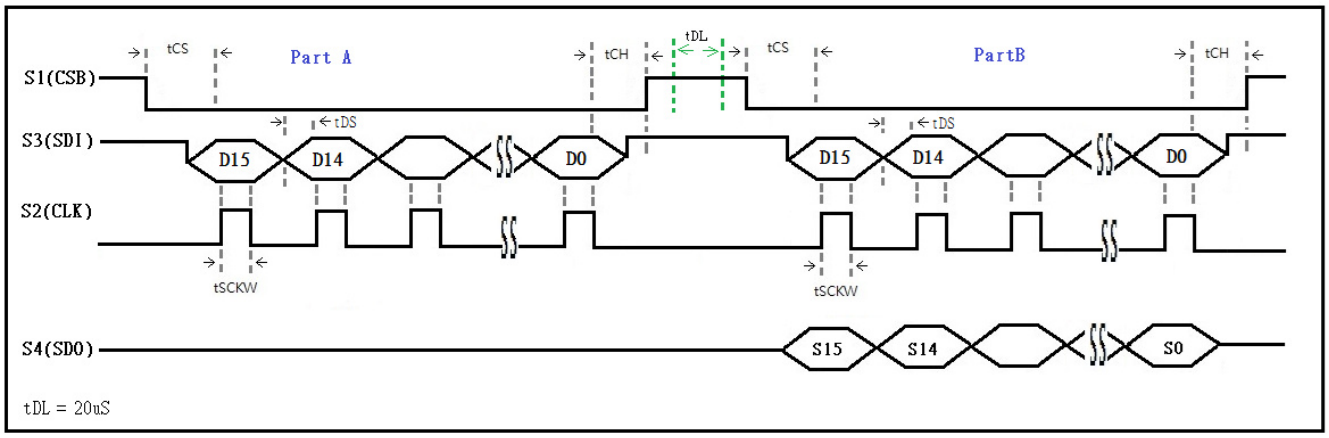


Fig. 24

Part A : Using command reference Fig. 14 SPI Command Table.

Part B : Using command is STOUT.

STOUT Command [MSB First] : Command input into the chip 16-bits data.

Command	D15	D14	D13	D12	D11	D10	D[9:0]
STOUT	0	1	1	1	1	0	don't care.

(1). STOUT(Status Out) :
a. Command timing reference Fig. 23 SPI Data Output Command timing.
b. Get Device Status.

I2C Mode :

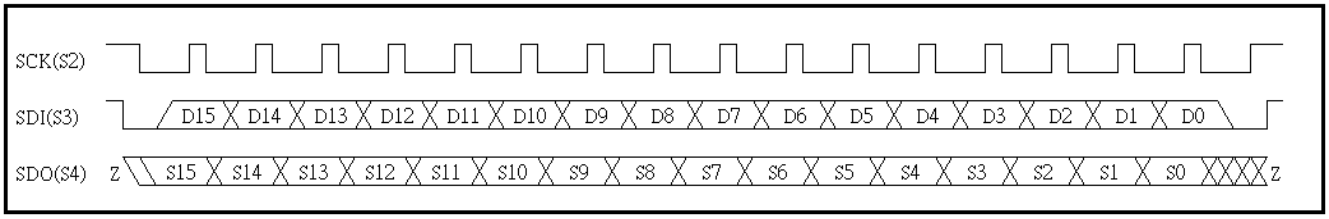


Fig. 25 I2C Data Output Command timing

* Data output to be changed at falling edge of SCK.

I2C TIMING WAVEFORMS

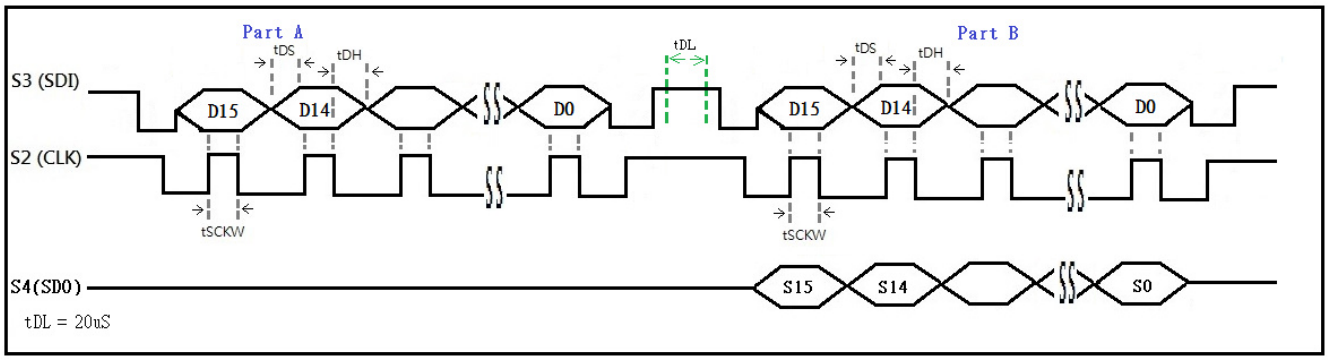


Fig. 26

Part A : Using command reference Fig. 18 I2C Command Table.

Part B : Using command is STOUT.

STOUT Command [MSB First] : Command input into the chip 16-bits data.

Command	D15	D14	D13	D12	D11	D10	D[9:0]
STOUT	1	1	1	1	1	1	don't care.

(1). STOUT(Status Out) :
a. Command timing reference Fig. 25 I2C Data Output Command timing.
b. Get Device Status.

▪ Oscillator Resistance :

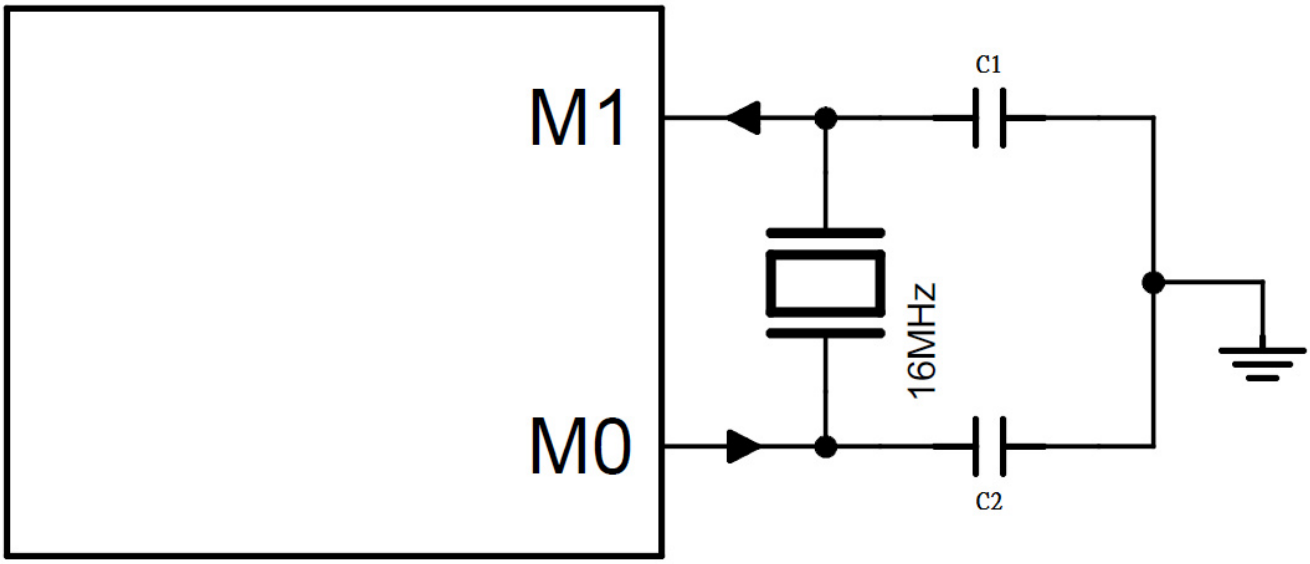
We have 3 modes can choose: Internal resistor、External resistor、Crystal resistance.

Rosc Int – No need to add resistor for OSC.

Rosc Ext – Use 68K ohm resistor in OSC pin.

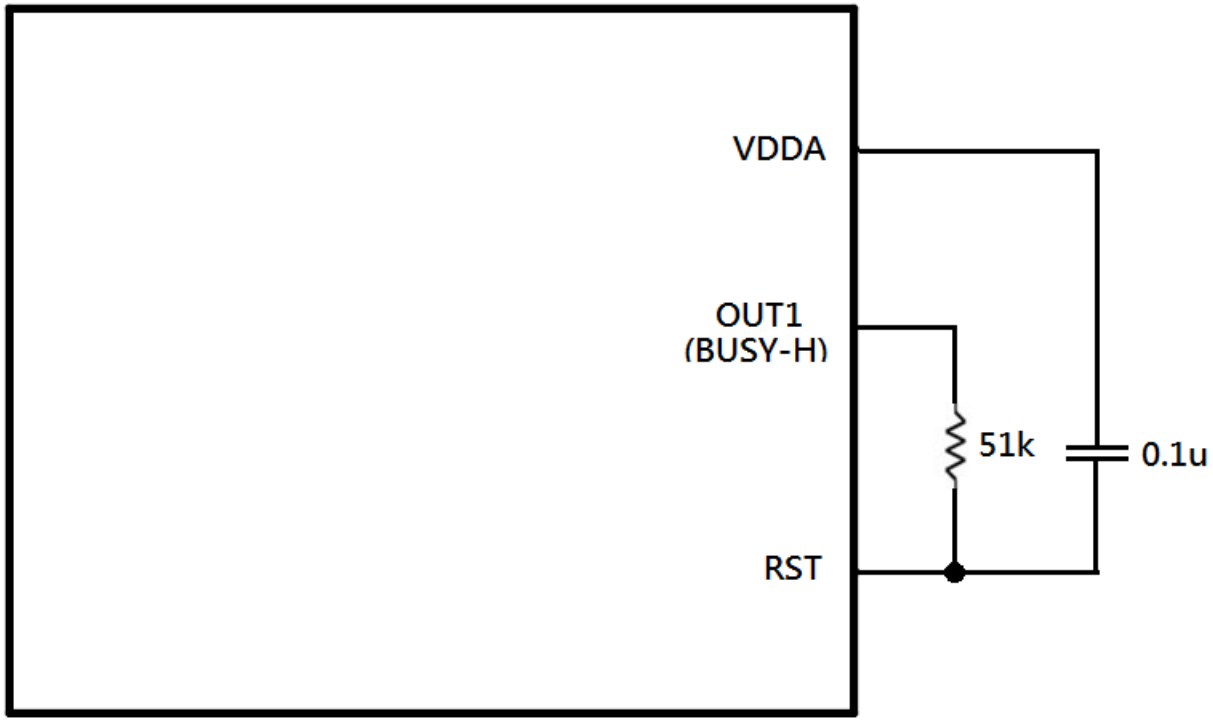
XT - Setting Crystal mode in M0 pin and M1 pin.

1. The crystal use 16MHz.
2. Use C1 , C2 for capacitor depend on Crystal spec.

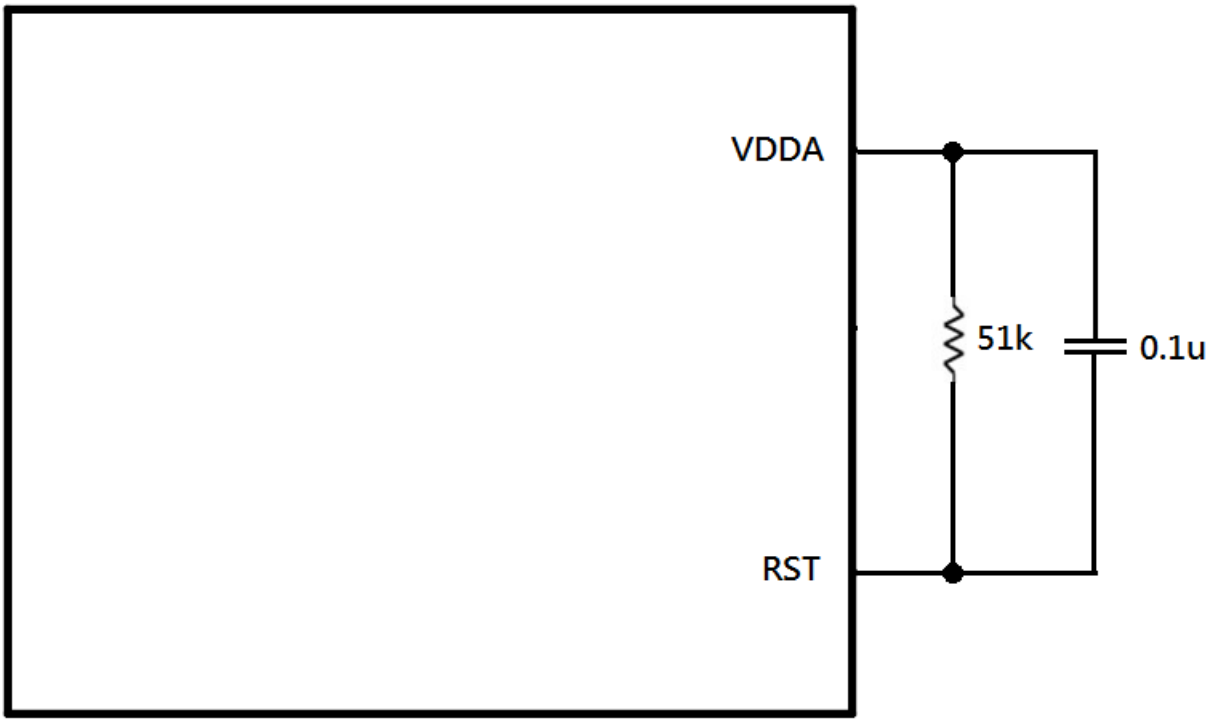


▪ Reset Circuit for Hot Plug-in Applications :

LVD provide basic voltage monitoring and prevent chip malfunction at low supply voltage which is around 1.3v to 2.0v.The supply voltage may be lower than 1.3v in hot plug-in applications.
We recommend adding a resistor as an external low voltage reset circuit to promote system stability in hot plug-in applications. The drawing shown below is the external low voltage reset circuit.



If there is no more OUT pin to act as busy-h, you can add a resistor between VDDA and RST to implement the external low voltage reset circuit. But there is dc current which is about 100uA.



▪ BLOCK DIAGRAM :

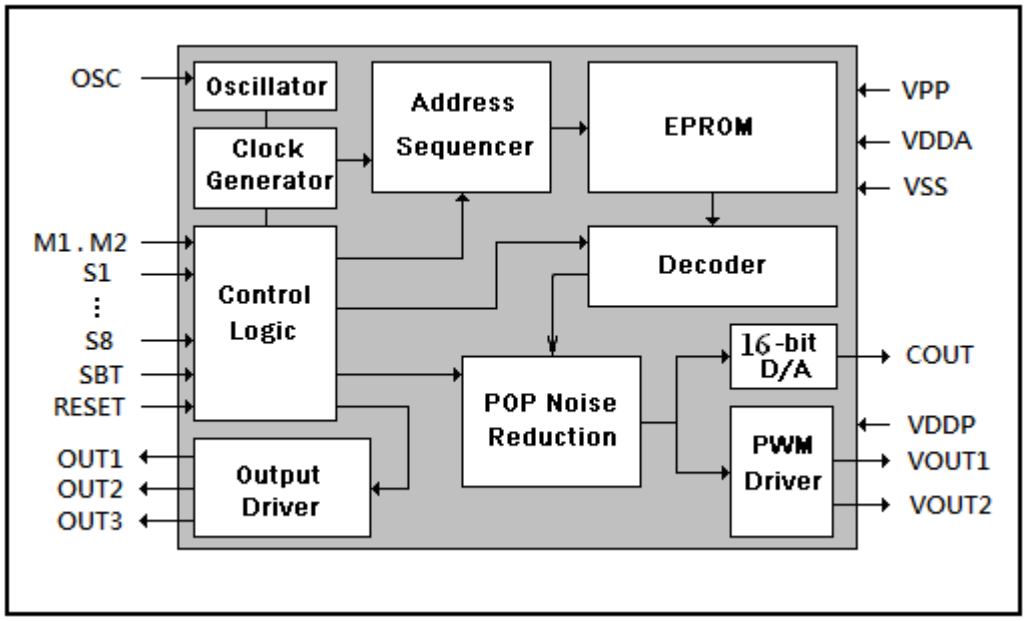


Fig. 27 Block Diagram

▪ ABSOLUTE MAXIMUM RATINGS :

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +5.0	V
V_{IN}	V_{SS} - 0.3 < V_{IN} < V_{DD} + 0.3	V
V_{OUT}	V_{SS} < V_{OUT} < V_{DD}	V
T (Operating):	-10 ~ +85	℃
T (Junction)	-10 ~ +85	℃
T (Storage)	-10 ~ +85	℃

DC CHARACTERISTICS (T_A = 0 to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.0		5.0	V	
ΔFc/Fc	Chip to chip frequency variation	-1.5		+1.5	%	

Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Condition
ISB	Standby current	3.3			1.0	uA	
		4.5			1.0		
IOP	Operating current	3.3		2.5		mA	Note3
		4.5		3.4			
IIH	Input current	3.3		7		uA	VIL=3.3V
		4.5		17			VIL=4.5V
VIH	Input high voltage	3.3		2/3 VDD		V	
		4.5					
VIL	Input low voltage	3.3		1/3 VDD		V	
		4.5					
IOH	Output high current	3.3		-16		mA	VOH=2.0V
		4.5		-25			VOH=3.5V
IOL	Output low current	3.3		26		mA	VOL=1.0V
		4.5		36			
IVOUT	VOUT Current	3.3		150		mA	Load=8Ω
		4.5		220			
ICOUT	COUT Current	3.3		4		mA	VCOUT=1.0V full scale
		4.5		4			
ΔF/F	Frequency Stability	3.3		1.5		%	Note1
		4.5		1.5			Note2

Note1:

$$\frac{Fosc(3.3) - Fosc(2.7)}{Fosc(3.3)}$$

Note2:

$$\frac{Fosc(5.0) - Fosc(4.5)}{Fosc(4.5)}$$

Note3:

No Load、DAC off、PWM on

TIMING WAVEFORMS :

- KEY 、SBT and MP3 Trigger Mode :

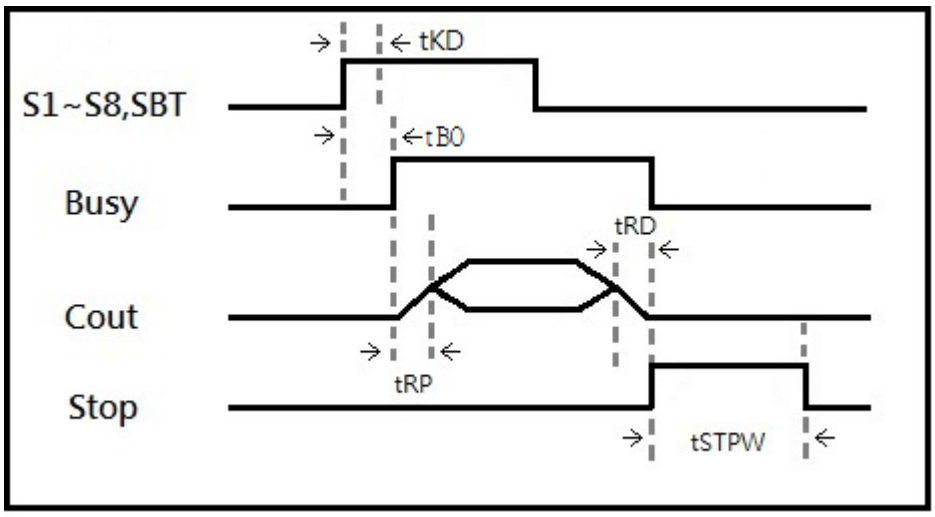


Fig. 28

- CPU Parallel Mode :

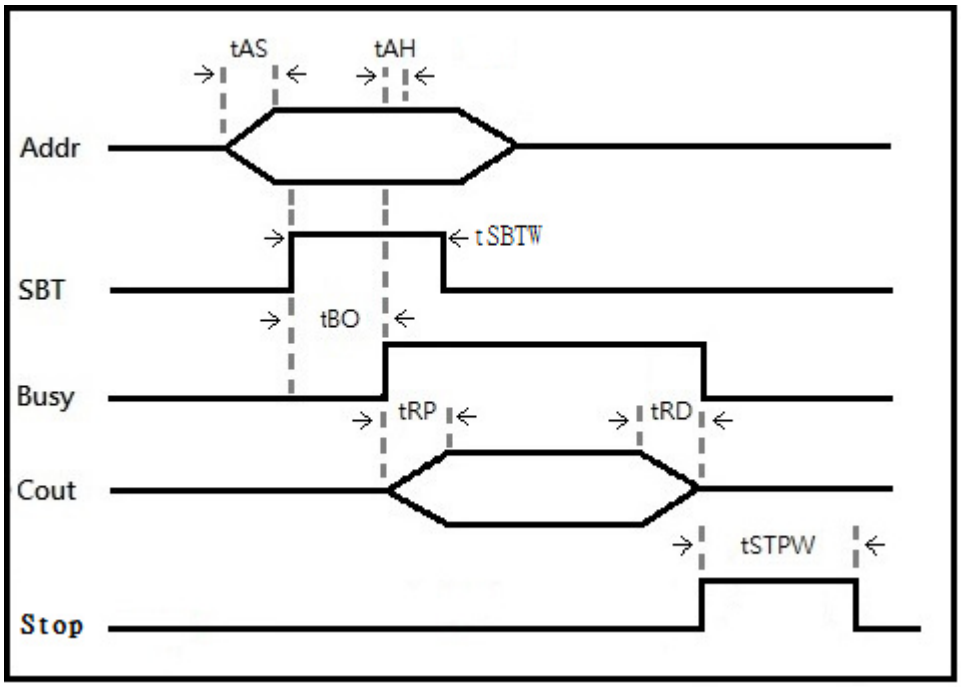


Fig. 29

- SPI Mode :

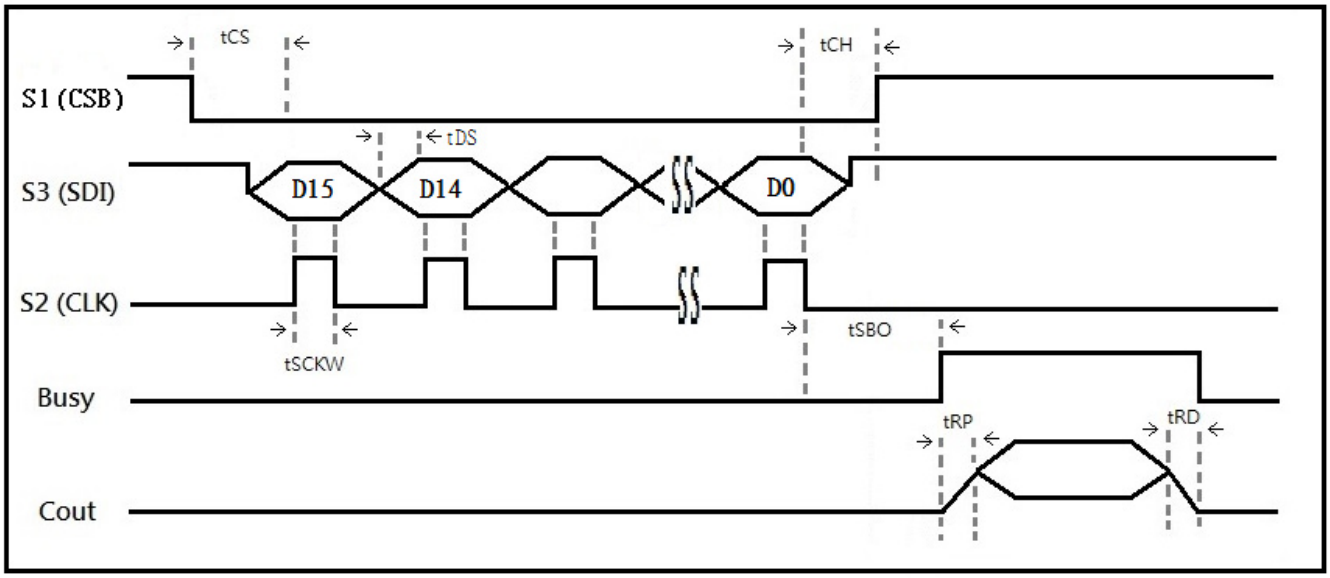


Fig. 30

- aP89 Mode CPU Serial :

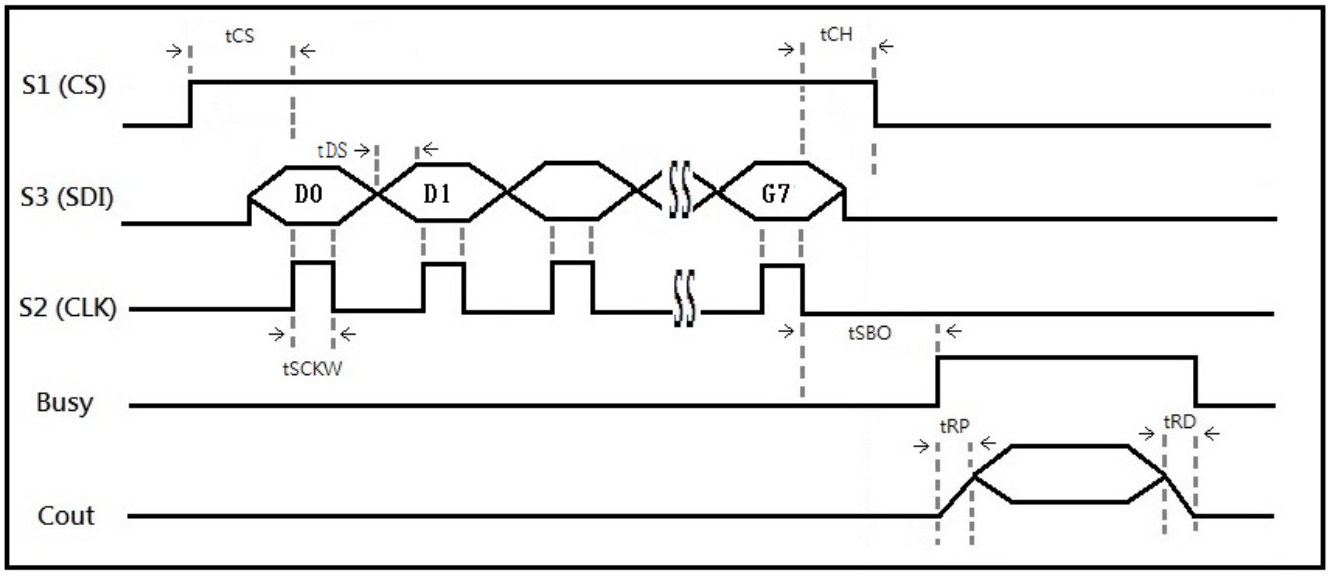


Fig. 31

- I2C Mode :

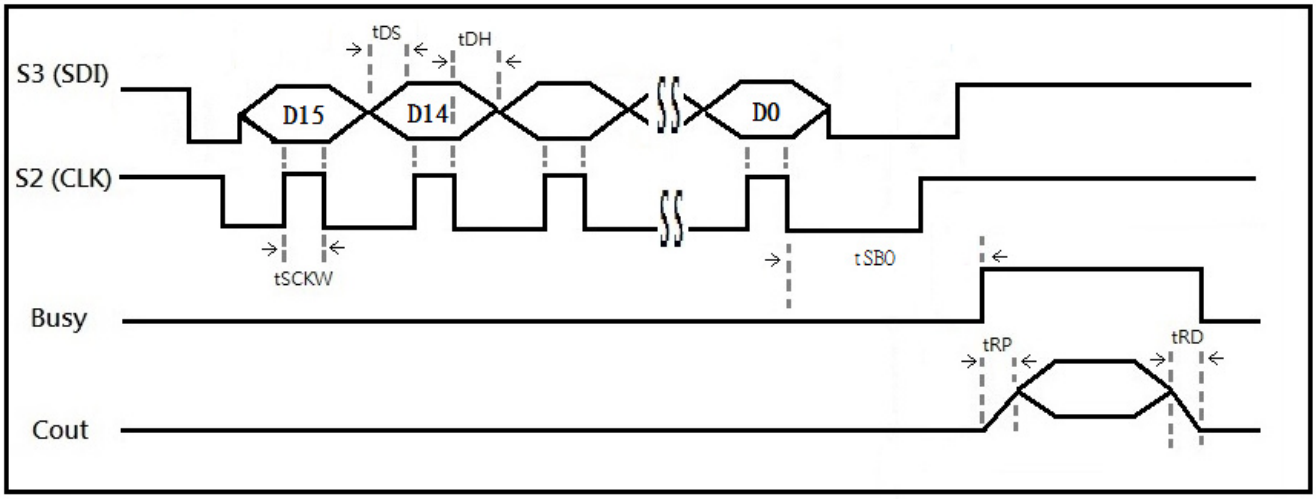


Fig. 32

▪ AC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.3V, V_{SS} = 0V, 8KHz sampling)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_{KD}	Key trigger debounce time (long)	—	16	—	ms	1
t_{KD}	Key trigger debounce time (long) – Retrigger during voice playback.	—	24	—	ms	1
t_{KD}	Key trigger debounce time (short)	—	1	—	ms	1
t_{KD}	Key trigger debounce time (short) – Retrigger during voice playback.	—	1.5	—	ms	1
t_{STPW}	STOP pulse width (long)	—	128	—	ms	1
t_{STPW}	STOP pulse width (short)	—	500	—	μs	1
t_{AS}	Address set-up time	300	—	—	ns	
t_{AH}	Address hold time	300	—	—	ns	
t_{SBTW}	SBT stroke pulse width (long)	16	—	—	ms	1
t_{SBTW}	SBT stroke pulse width (short)	1	—	—	ms	1
t_{BO}	BUSY signal output delay time(long)	—	24	—	ms	1
t_{BO}	BUSY signal output delay time(short)	—	1	—	ms	1
t_{CS}	Chip select set-up time	100	—	—	ns	
t_{CH}	Chip select hold time	100	—	—	ns	
t_{SCKW}	Serial clock pulse width	1	—	—	μs	
t_{DS}	Data set-up time	100	—	—	ns	
t_{DH}	Data hold time	100	—	—	ns	
t_{SBO}	BUSY signal output delay time	—	—	2	ms	
t_{RP}	Ramp Up time	—	160	—	ms	
t_{RP}	Ramp Up time at cpu parallel mode	—	20	—	ms	
t_{RD}	Ramp Down time	—	160	—	ms	
t_{RD}	Ramp Down time at cpu parallel mode	—	20	—	ms	
t_{FD}	Full signal output delay time	—	—	2	ms	

Notes :

1. The long or short debounce time is selectable as whole chip option during Voice Files Compiling.

In Circuit Program Applications :

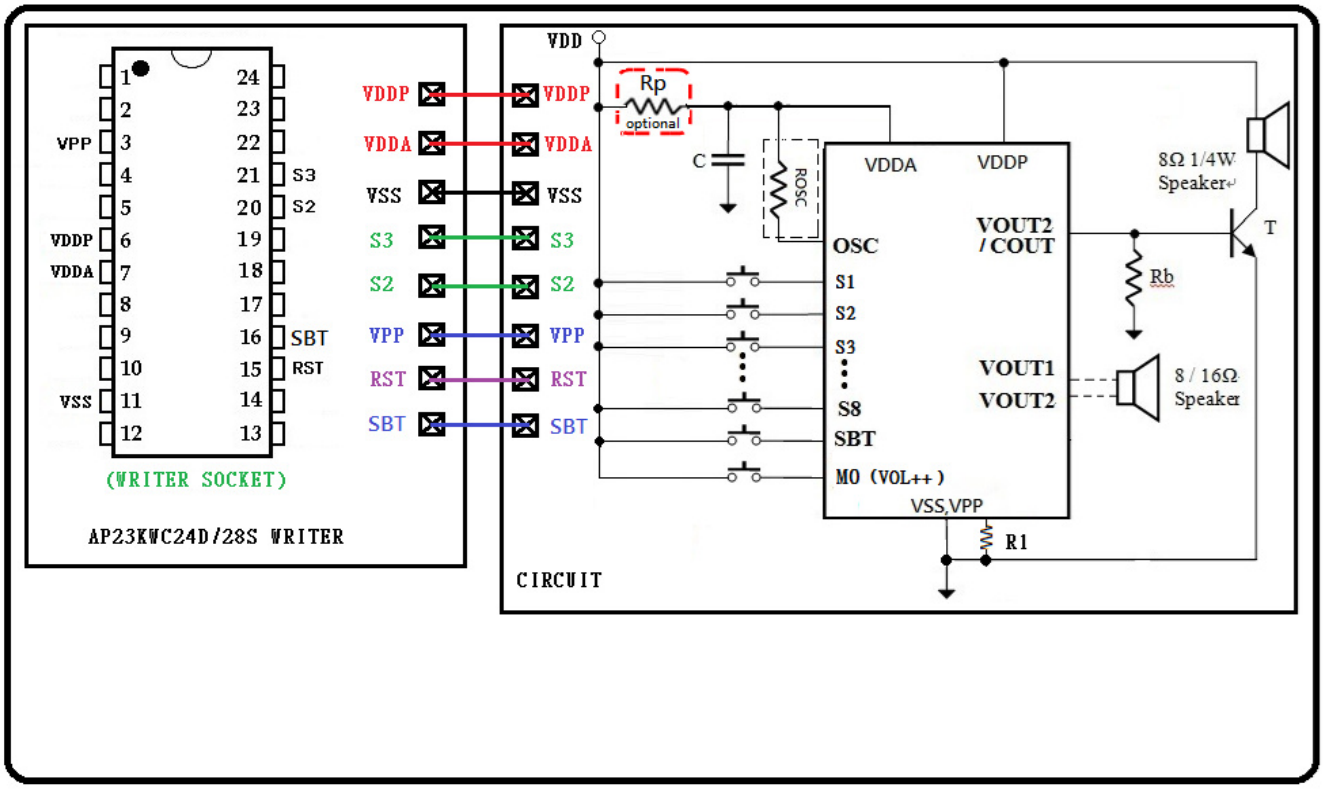


Fig. 33

Note:

1. Between VPP and GND should add R1(10K)Ω.
2. Between Writer and Circuit connect wire less than 10cm is the better.
3. If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance.
   Distance between caps and ICs should be minimized to reduce spreading inductance.
   The wiring length between the IC and caps may be less than 150mil.
4. Rp is used to filter noise from power line.
   A. Rp is unnecessary in DAC mode or VDD less than 3.6v.
      The value of Rp is 0 ohm in DAC mode.
   B. If voltage is higher than 3.6V and chip is configured as PWM mode,
      Rp is necessary for system stability.
      The value of Rp is 56 ohm in PWM mode.
      The minimum operating voltage would be lifted from 2.0v to 2.2v, when Rp is added.
   C. If Rp is added and there are LED drove by OUT[1:3] pin,
      please configure the OUT pin as active low to drive LED.

TYPICAL APPLICATIONS :

Key Mode

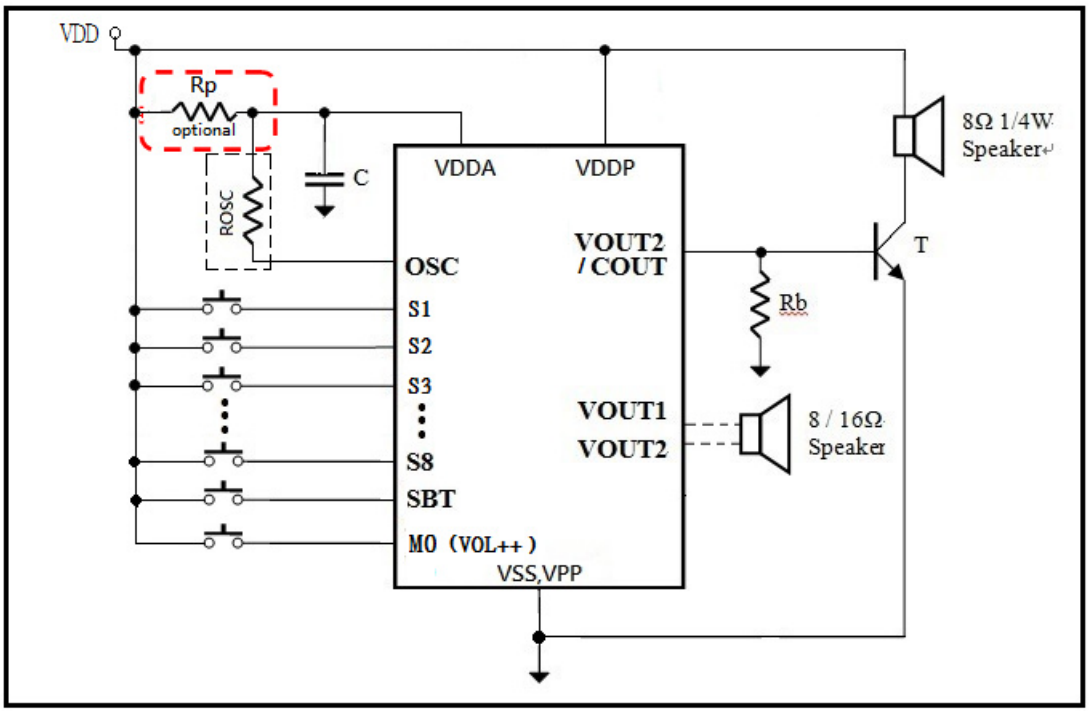


Fig. 34

Note:

1. If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance.
   Distance between caps and ICs should be minimized to reduce spreading inductance.
   The wiring length between the IC and caps may be less than 150mil.

2. Rp is used to filter noise from power line.
   A. Rp is unnecessary in DAC mode or VDD less than 3.6v.
      The value of Rp is 0 ohm in DAC mode.
   B. If voltage is higher than 3.6V and chip is configured as PWM mode,
      Rp is necessary for system stability.
      The value of Rp is 56 ohm in PWM mode.
      The minimum operating voltage would be lifted from 2.0v to 2.2v, when Rp is added.
   C. If Rp is added and there are LED drove by OUT[1:3] pin,
      please configure the OUT pin as active low to drive LED.

Ex: Single key control volume.

If volume level is 8 , 1→2→3→4→5→6→7→8→1→2→3→ 4→….

CPU Parallel Mode

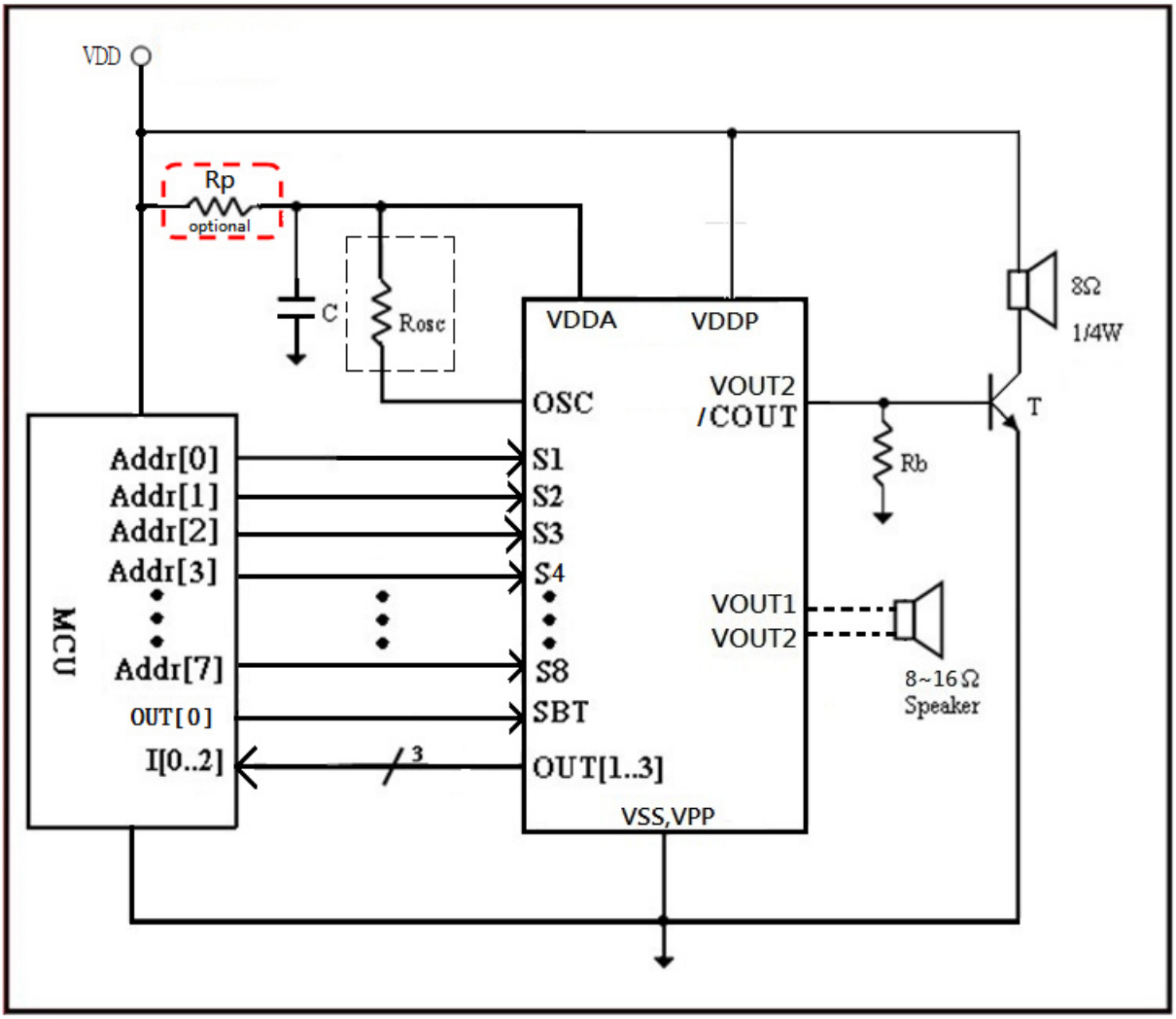


Fig. 35

Note:

1. C is capacitor from 0.1uF to 4.7uF depends on the kind of Vdd source and sound loudness.
2. Rb is base resistor from 120 Ohm to 390 Ohm depends on Vdd value and transistor gain.
3. T is an NPN transistor with beta larger than 150.
4. Reference value for the above components are Rb = 390 Ohm and T = 8050D.
5. If voltage is higher than 4.0V, C ($0.1uF_{(typ)}$) is necessary for endure high voltage and protect it from noise which may affect its performance.
   Distance between caps and ICs should be minimized to reduce spreading inductance.
   The wiring length between the IC and caps may be less than 150mil.
6. Rp is used to filter noise from power line.
   A. Rp is unnecessary in DAC mode or VDD less than 3.6v.
      The value of Rp is 0 ohm in DAC mode.
   B. If voltage is higher than 3.6V and chip is configured as PWM mode,
      Rp is necessary for system stability.
      The value of Rp is 56 ohm in PWM mode.
      The minimum operating voltage would be lifted from 2.0v to 2.2v, when Rp is added.
   C. If Rp is added and there are LED drove by OUT[1:3] pin,
      please configure the OUT pin as active low to drive LED.

SPI Mode

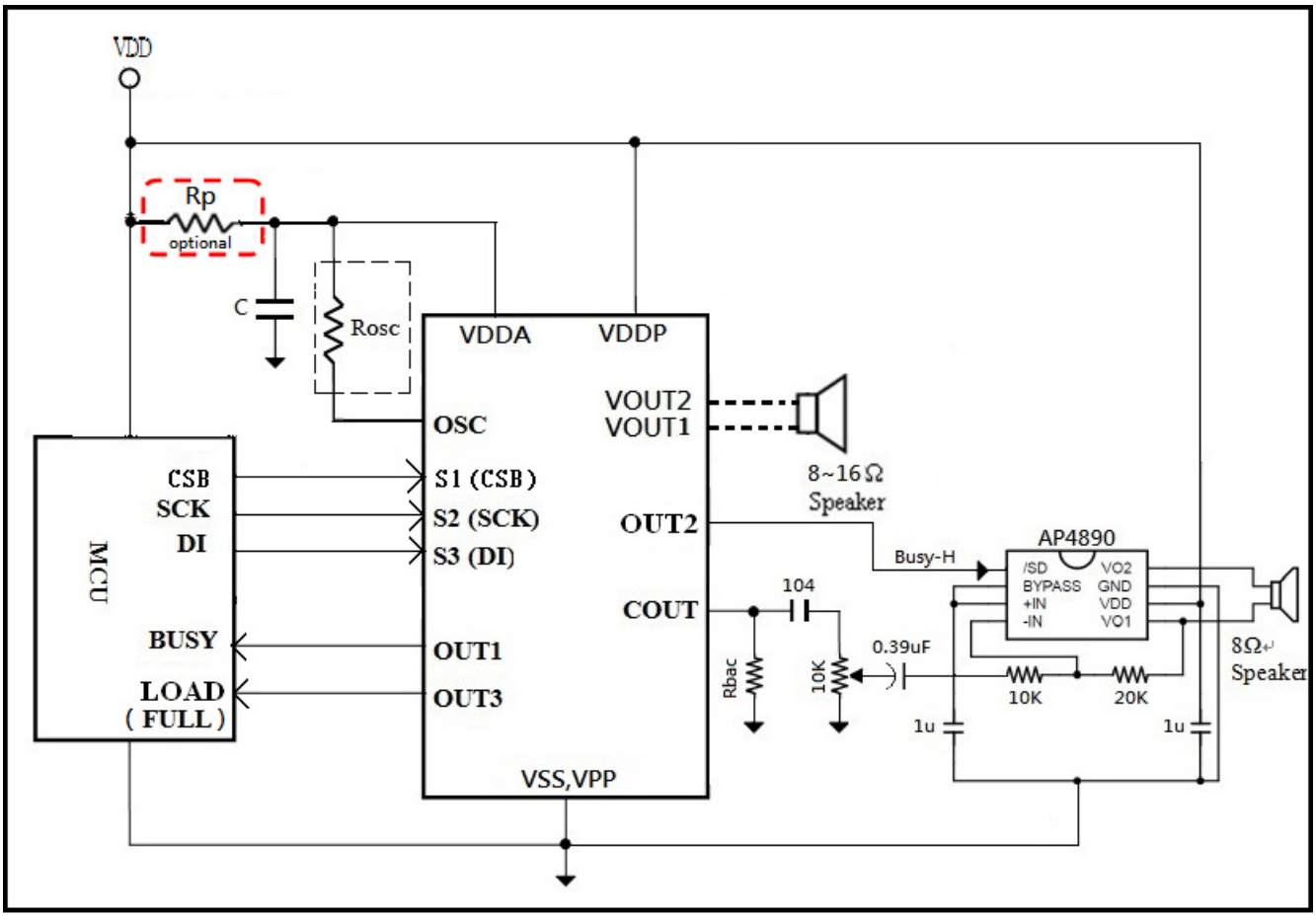


Fig. 36

Note:

1. If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance.
   Distance between caps and ICs should be minimized to reduce spreading inductance.
   The wiring length between the IC and caps may be less than 150mil.

2. Rp is used to filter noise from power line.
   A. Rp is unnecessary in DAC mode or VDD less than 3.6v.
      The value of Rp is 0 ohm in DAC mode.
   B. If voltage is higher than 3.6V and chip is configured as PWM mode,
      Rp is necessary for system stability.
      The value of Rp is 56 ohm in PWM mode.
      The minimum operating voltage would be lifted from 2.0v to 2.2v, when Rp is added.
   C. If Rp is added and there are LED drove by OUT[1:3] pin,
      please configure the OUT pin as active low to drive LED.

I2C Mode

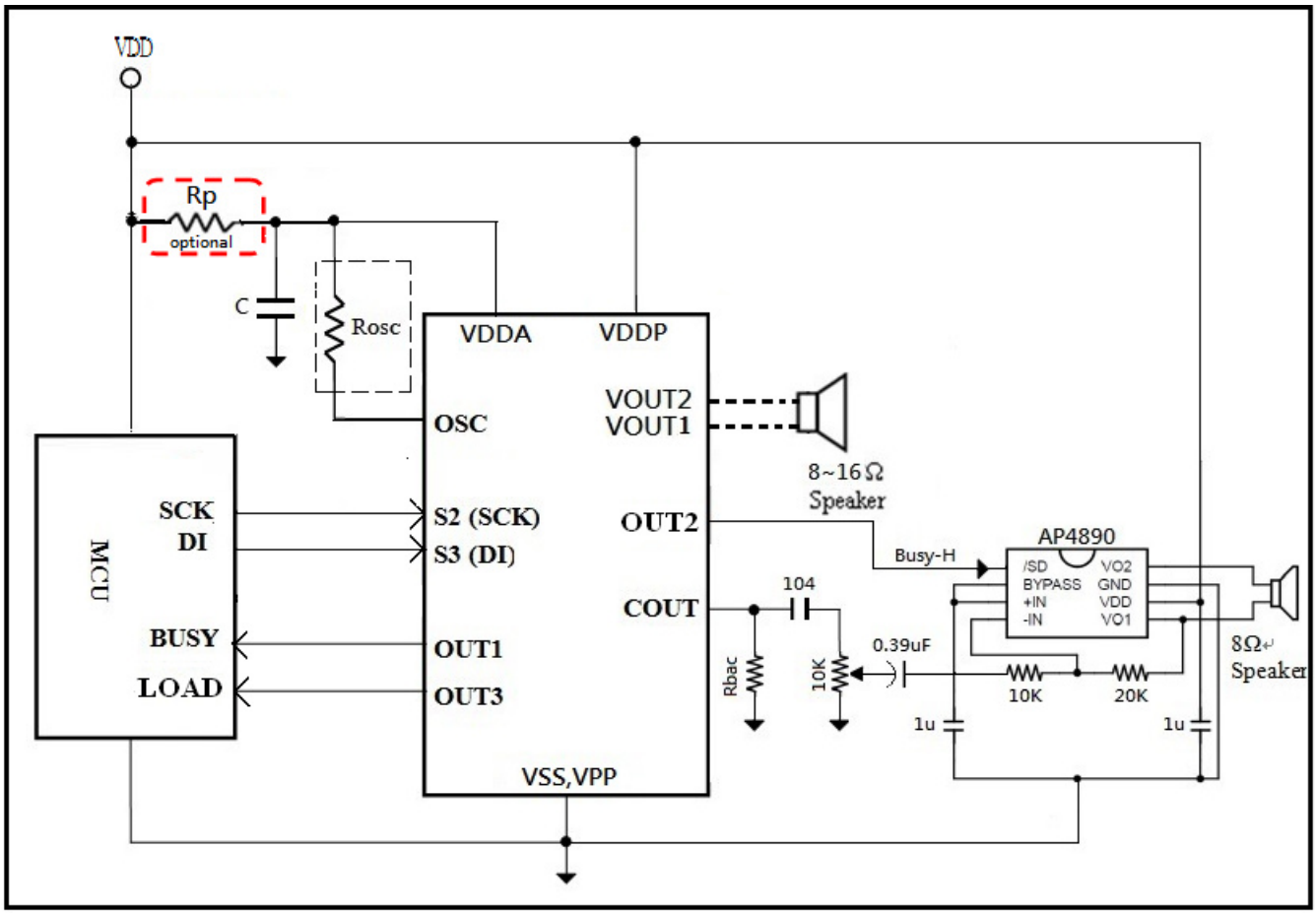


Fig. 37

Note:

1. If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance.
   Distance between caps and ICs should be minimized to reduce spreading inductance.
   The wiring length between the IC and caps may be less than 150mil.

2. Rp is used to filter noise from power line.
   A. Rp is unnecessary in DAC mode or VDD less than 3.6v.
      The value of Rp is 0 ohm in DAC mode.
   B. If voltage is higher than 3.6V and chip is configured as PWM mode,
      Rp is necessary for system stability.
      The value of Rp is 56 ohm in PWM mode.
      The minimum operating voltage would be lifted from 2.0v to 2.2v, when Rp is added.
   C. If Rp is added and there are LED drove by OUT[1:3] pin,
      please configure the OUT pin as active low to drive LED.

MP3 Mode

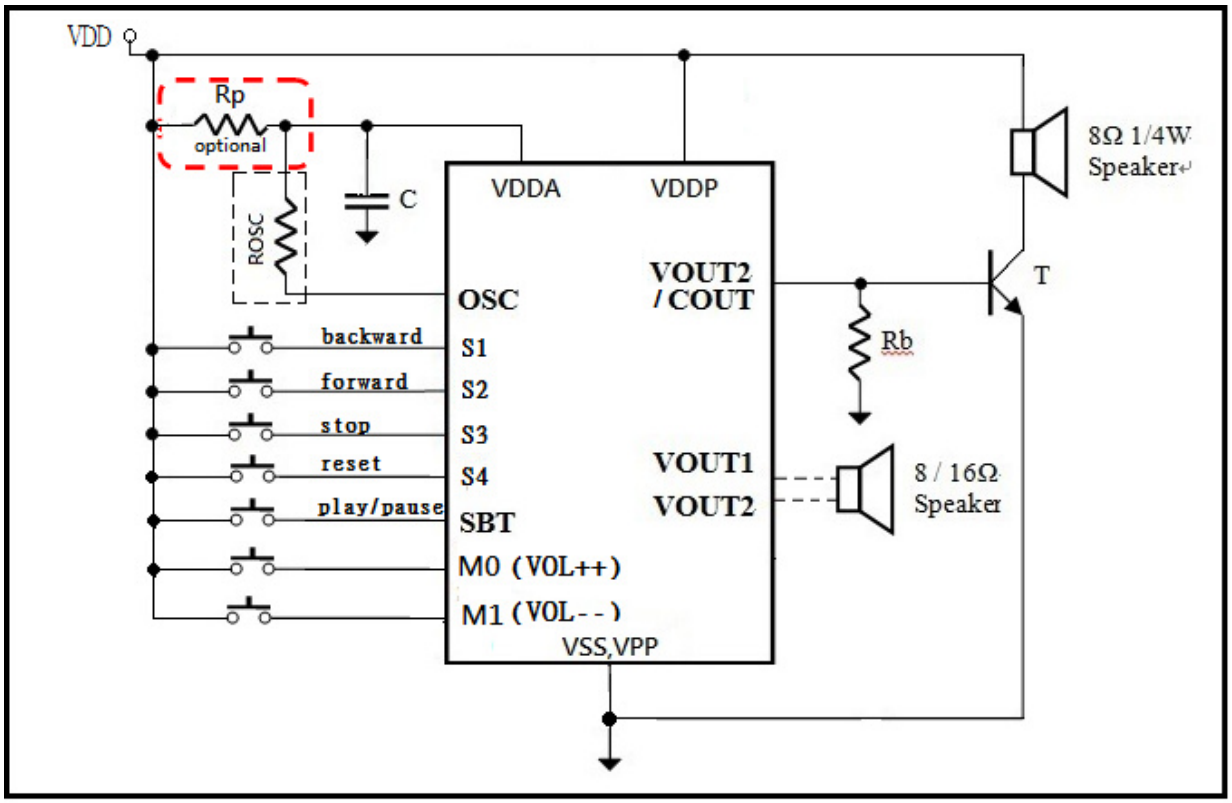


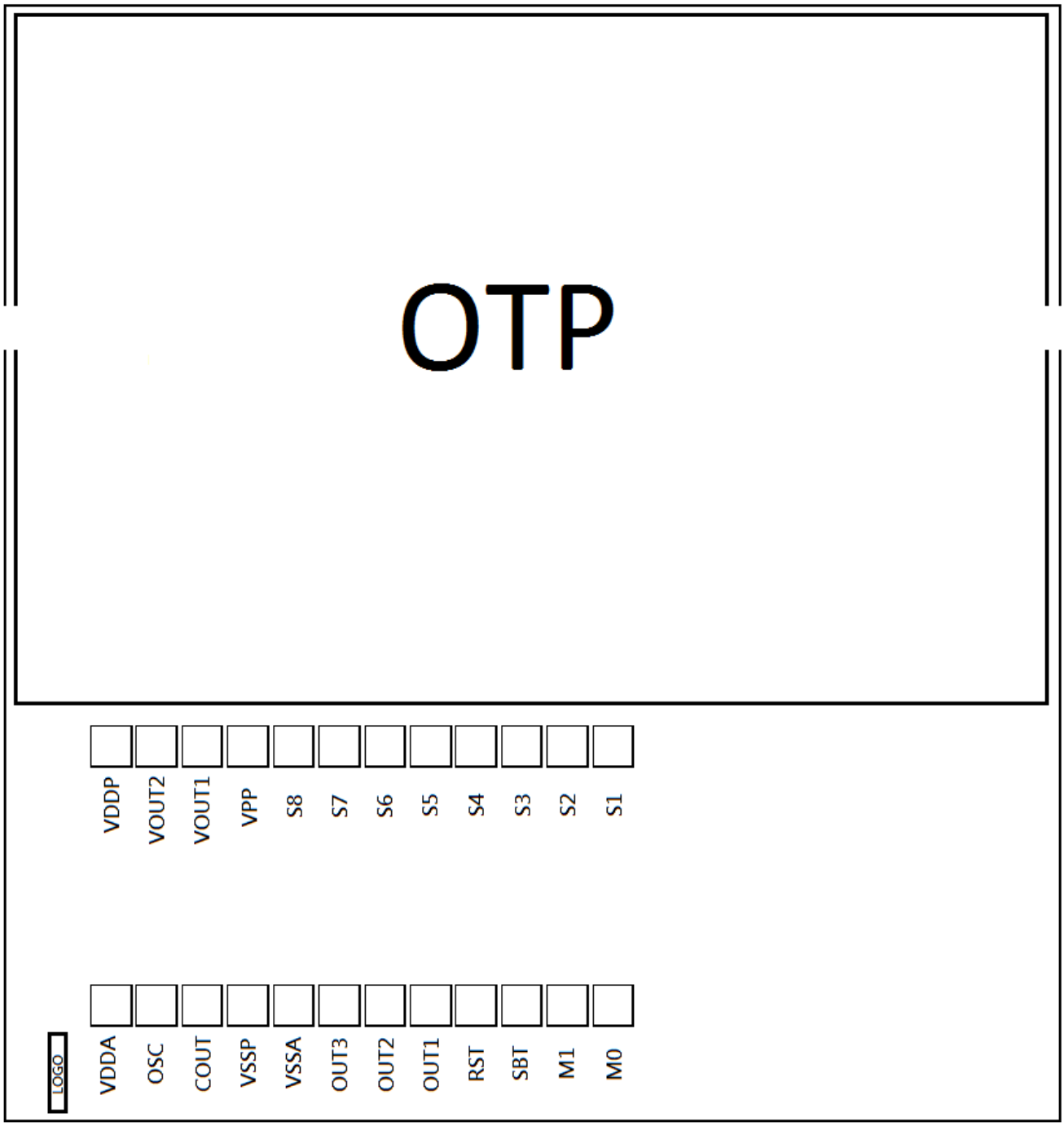
Fig. 38

Note:

1 .If voltage is higher than 4.0V, C (0.1uF(typ)) is necessary for endure high voltage and protect it from noise which may affect its performance.
Distance between caps and ICs should be minimized to reduce spreading inductance.
The wiring length between the IC and caps may be less than 150mil.

2. Rp is used to filter noise from power line.
A. Rp is unnecessary in DAC mode or VDD less than 3.6v.
The value of Rp is 0 ohm in DAC mode.
B. If voltage is higher than 3.6V and chip is configured as PWM mode,
Rp is necessary for system stability.
The value of Rp is 56 ohm in PWM mode.
The minimum operating voltage would be lifted from 2.0v to 2.2v, when Rp is added.
C. If Rp is added and there are LED drove by OUT[1:3] pin,
please configure the OUT pin as active low to drive LED.

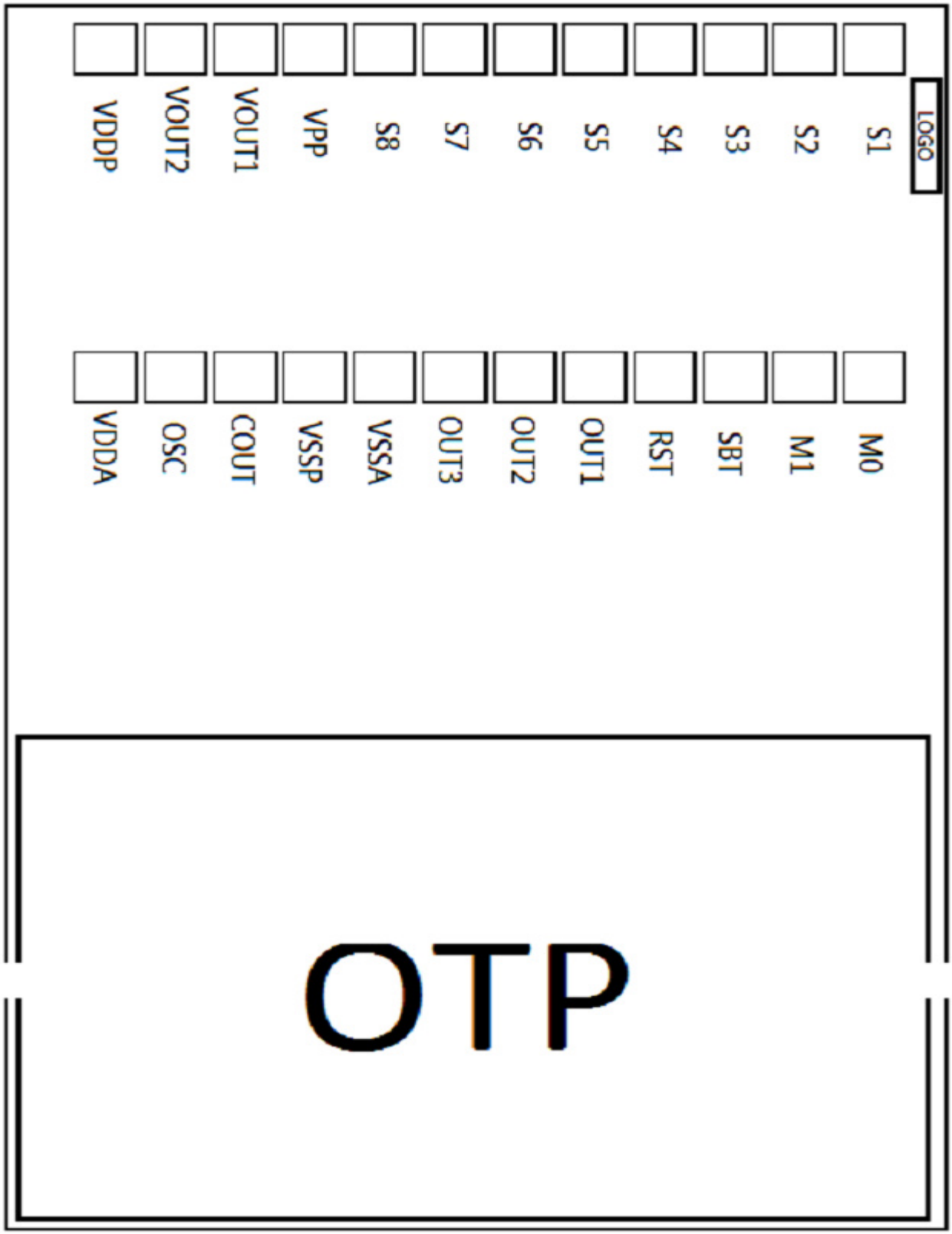
BONDING PAD DIAGRAMS (aP89682K/aP89341K)



Notes:

1. Between VPP and GND should add 10KΩ.
2. VDDA and VDDP should be connected to the Positive Power Supply.
3. VSSA and VSSP should be connected to the Power GND.
4. Substrate should be connected to the Power GND.

BONDING PAD DIAGRAMS (aP89170K/aP89085K)

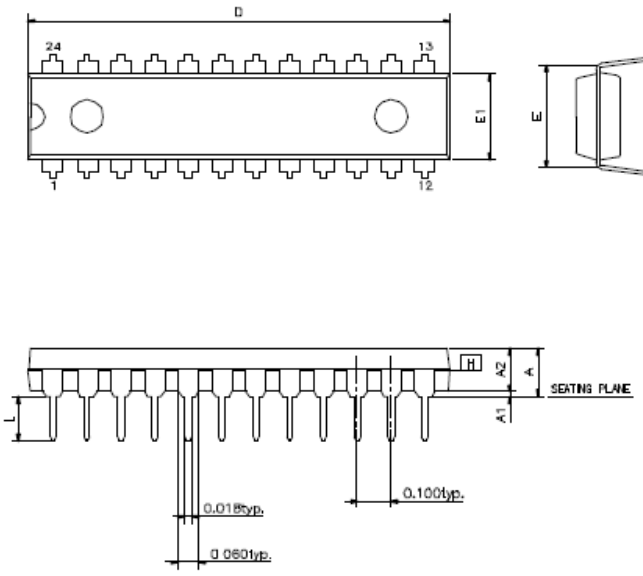


Notes:

1.Between VPP and GND should add 10KΩ.
2.VDDA and VDDP should be connected to the Positive Power Supply.
3.VSSA and VSSP should be connected to the Power GND.
4.Substrate should be connected to the Power GND.

PACKAGES DIMENSION OUTLINES

24-Pin 300mil P-DIP Package

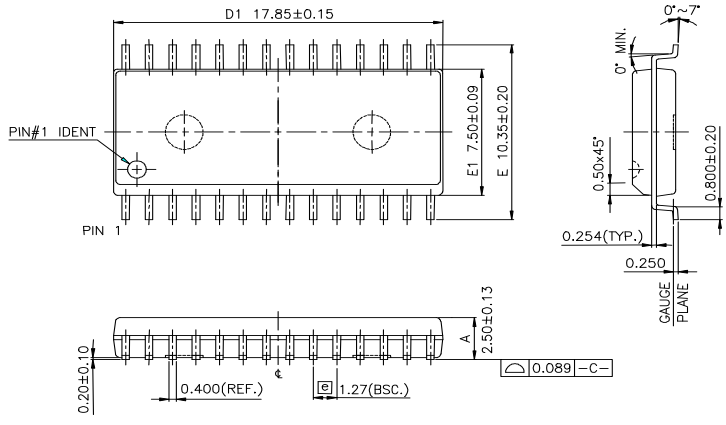


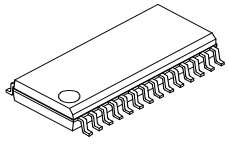
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E		0.300 BSC.	
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-001 AF
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

28-Pin 300mil SOP Package





NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLMETERS (MM).
2. DIMENSION D1 & E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.089 MAX. FORM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

HISTORY

2015/03/10
aP89682K_341K__170K_085K SPEC.

2015/07/20
aP89682K_341K__170K_085K SPEC : Modify cpu control timing waveforms
Modify Page. 18 DC CHARACTERISTICS
Reduce output function from 14 to 9.
Remove aP89 mode1 and aP89 mode2 and new adding aP89mode.

2015/09/08
aP89682K_341K__170K_085K SPEC : Modify ULAW5 to ULAW8
Add SBT mode independent description.
Optimize the CPU mode control.
Add In Circuit Program application on page. 34.

2016/01/20
aP89682K_341K__170K_085K SPEC : Add decoupling cap suggestion at high voltage application.
Page 34 to 39.
Add testing condition of Iop on page 29.

2016/04/26
aP89682K_341K__170K_085K SPEC : Add Rp to filter noise from power line.
Page 35 to 40.
Add reset circuit for hot plug-in applications.

2016/05/24
aP89682K_341K__170K_085K SPEC : Modify in circuit program schematic to support copier.
Page 4,35.

2017/03/13
aP89682K_341K__170K_085K SPEC : Add a new description in volume control in cpu serial control, its default value would be fixed at "16 level". Page 12.
Remove rewind command of cpu serial. Page 12, 14,16,17,19,20,22.
Correct wrong typing in cpu serial command vol++ and vol- -. .
Page 14,16,17,19,20,22
Modify Fig.15 SPI Command timing change to (CPOL = 0 & CPHA = 0)
mode 0 CPOL(clock polarity)=0,the sck idle=0 CPHA(clock phase)=0,the sck low to hagh(rising) Latch the data(DI)
Fig.16 Power-Up command timing suggest add delay 20us. Page 18.
Fig.20 Power-Up command timing suggest add delay 20us. Page 21.
Modify Fig.24 SPI Command timing change to (CPOL = 0 & CPHA = 0)
mode 0. Page 25.