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VOICE OTP IC

*a*P89341 – 341sec
*a*P89170 – 170sec
*a*P89085 – 85sec

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FEATURES

- Standard CMOS process.
- Embedded 8M/4M/2M EPROM.
- 341/170/85 sec Voice Length at 6KHz sampling and 4-bit ADPCM compression.
- Maximum 254 voice groups.
- Combination of voice blocks to extend playback duration.
- 7680 table entries are available for voice block combinations.
- User selectable PCM or ADPCM data compression
- Three triggering modes are available (controlled by M1 and M0 input pins):
  - Key Trigger Mode (M1=0, M0=0) - S1 ~ S8 to trigger up to 32 voice groups; SBT to trigger up to 254 voice groups sequentially.
  - CPU Parallel Trigger Mode (M1=0, M0=1) – S[8:1] services as 8-bits address to trigger up to 254 voice groups with SBT goes HIGH to strobe the address bits.
  - CPU Serial Command Mode (M1=1, M0=0) – user commands are clocked serially into the chip which enable user to fully control the operation of the chip.
- Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Whole Chip Options: Ramp / No-ramp; Output Options; Long / Short debounce time.
- Optional 16ms or 65us (@ 8KHz sampling rate) selectable debounce time
- RST pin set to HIGH to stop the playback at once
- Three user programmable outputs for STOP pulse, BUSY signal and flashing LED.
- Built-in oscillator to control sampling frequency with an external resistor
- 2.2V – 3.6V single power supply and < 5uA low stand-by current
- PWM Vout1 and Vout2 drive speaker directly
- D/A COUT pin drives speaker through an external BJT
- Development System support voice compilation.

DESCRIPTION

aP89341/170/085 series high performance Voice OTP is fabricated with Standard CMOS process with embedded 8M/4M/2M bits EPROM. It can store up to 341/170/85 sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 8-bit PCM is also available as user selectable option. Three trigger modes, simple Key trigger mode, Parallel CPU trigger mode and CPU serial command mode, facilitate different user interface. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 8-bit current mode D/A output and PWM direct speaker driving output minimize the number of external components. PC controlled programmer and developing software are available.

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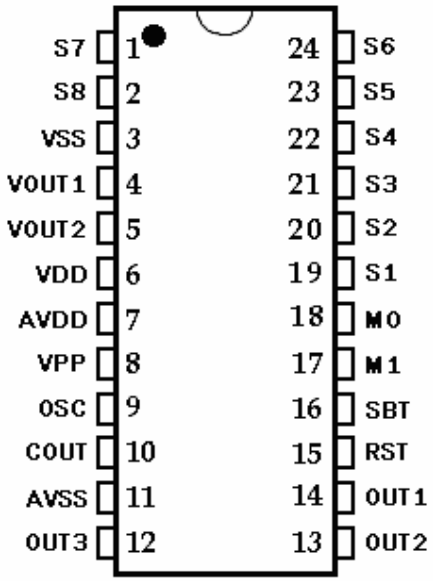
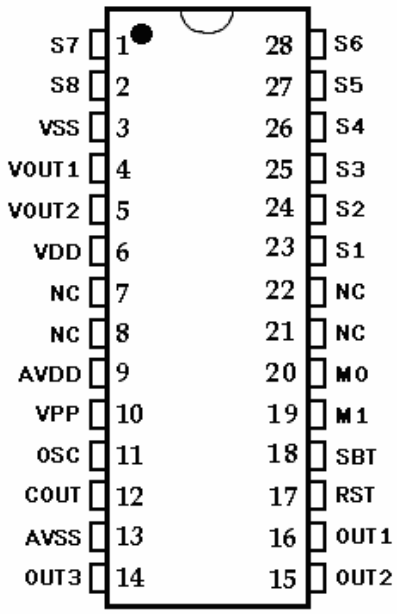
PIN CONFIGURATIONS



DIP 300 MIL

PIN CONFIGURATIONS



SOP 300 MIL

PIN NAMES

PIN (24-pin)	Playback Mode	OTP Program Mode	Description
1	S7	IO6	Trigger pin (I/O pin with internal pull-down)
2	S8	IO7	Trigger pin (I/O pin with internal pull-down)
3	VSS	VSS	Ground
4	VOUT1	-	PWM output to drive speaker directly
5	VOUT2	-	PWM output to drive speaker directly
6	VDD	VDD	Supply voltage
7	AVDD	AVDD	Analog supply voltage
8	VPP	VPP	Supply voltage for OTP programming
9	OSC	ACLK	Oscillator input
10	COUT	-	D/A current output
11	AVSS	AVSS	Analog ground
12	OUT3	-	Programmable output (I/O pin)
13	OUT2	SIO	Programmable output (I/O pin)
14	OUT1	OEB	Programmable output (I/O pin)
15	RST	DCLK	Reset pin (input pin with internal pull-down)
16	SBT	PGM	Trigger pin (I/O pin with internal pull-down)
17	M1	M1	Mode select pin 1 (input with internal pull-down)
18	M0	M0	Mode select pin 0 (input with internal pull-down)
19 ~ 24	S1~S6	IO0~IO6	Trigger input (I/O pin with internal pull-down)

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PIN DESCRIPTIONS

S1 ~ S8

Input Trigger Pins:
- In Key Trigger Mode, S1 to S8 is used to trigger the first 32 out of the total 254 Voice Groups .
- In CPU Parallel Command Mode, S1 to S8 serve as Voice Group address inputs for 254 Voice Groups with S1 as LSB and S8 as MSB.
- In CPU Serial Command Mode, S1 is Chip Select (SC) pin to initiate the command input. S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip. S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In OTP Programming Mode, S1 to S8 are used as data I/O pins.

SBT

Input Trigger Pin:
- In Key Trigger Mode, this pin is trigger pin to trigger the playback of Voice Groups one by one sequentially.
- In CPU Parallel Command Mode, this pin is used as address strobe to latch the Voice Group address input at S1 to S8 and starts the voice playback.
- In OTP Programming Mode, this pin is used as PGM signal.

VDD and AVDD

Power Supply Pins: These two pins must be connected together to the positive power supply.

VSS and AVSS

Power Ground Pins: These two pins must be connected to the power ground.

M0 and M1

Operating Mode Setting Pins:
- M1=0, M0=0 set the chip into Key Trigger Mode
- M1=0, M0=1 set the chip into CPU Parallel Command Mode
- M1=1, M0=0 set the chip into CPU Serial Command Mode
- M1=1, M0=1 set the chip into OTP Programming Mode

VOUT1 and VOUT2

Digital PWM output pins which can drive speaker and buzzer directly for voice playback.

OSC

During voice playback, an external resistor is connect between this pin and the VDD pin to set the sampling frequency. In OTP Programming Mode, this is the ACLK input signal.

VPP

During voice playback, this pin must be connected together with VDD to the positive power supply voltage. In OTP Programming Mode, this pin is connected to a separate 6.5V power supply voltage for EPROM programming.

OUT1, OUT2 and OUT3

- In Key Trigger Mode and CPU Parallel Command Mode, these pins are user programmable pins for the STOP pulse, BUSY and LED signals.
- In CPU Serial Command Mode, OUT1, OUT2 and OUT3 are fixed as BUSY, POUT and FULL status output which tell the status of the chip operation. POUT can be further configurable to BUSYB, 8K, 4K, 2K, 1K, 16Hz, 1M and EMPTY (or FULLB).
- During OTP programming, OUT1 serves as OEB while OUT2 serves as SIO (serial data IO).

COUT

Analog 8-bit current mode D/A output for voice playback

RST

Chip reset in playback mode or DCLK pin in OTP programming mode.

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VOICE SECTION COMBINATIONS

Voice files created by the PC base developing system are stored in the built-in EPROM of the aP89341/170/085 chip as a number of fixed length Voice Blocks. Voice Blocks are then selected and grouped into Voice Groups for playback. Up to 254 Voice Groups are allowed. A Voice Block Table is used to store the information of combinations of Voice Blocks and then group them together to form Voice Group.

Chip	aP89341	aP89170	aP89085
Memory size	8M bits	4M bits	2M bits
Max no. of Voice Block	2016	992	480
Max. no. of Voice Group	254	254	254
No of Voice Table entries	7680	7680	7680
Voice Length (@ 6KHz 4-bit ADPCM)	341 sec	170 sec	85 sec

Example of Voice Block Combination

Assume here we have three voice files, they are "How are You?", Sound Effect and Music. Each of the voice file is divided into a number of fixed length Voice Block and stored into the memory.

Voice File 1 - "How are You?" is stored in Voice Block B0 to B12.
Voice File 2 - Sound Effect is stored in Voice Block B13 to B15.
Voice File 3 - Music is Voice Block B16 to B40.

Voice Blocks are grouped together using Voice Table to form Voice Group for playback:

Group no.	Voice Group contents	Voice Table Entries
Group 1	"How are You?"	B0 … B12
Group 2	Sound Effect + "How are You?"	B13 … B15 + B0 … B12
Group 3	"How are You?" + Music	B0 … B12 + B16 … B40
Group 4	Music	B16 … B40

Voice Data Compression

Voice File data is stored in the on-chip EPROM as either 4-bit ADPCM or 8-bit PCM format. Voice data stored as 4-bit ADPCM provides 2:1 data compression which can save 50% of memory space. On the other hand, voice data are stored as 8-bit PCM format means no data compression is employed but voice playback quality will be better.

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Programmable Options

In Key Trigger Mode (M1=0; M0=0) and CPU Parallel Trigger Mode (M1=0; M0=1), user can select different trigger functions and output signals to be sent out from the pins OUT1, OUT2 and OUT3.

Options that affect all Voice Group playback are called Whole Chip Options. Options that only affect the playback of individual Voice Group are called Group Options.

Whole Chip Options

- Long (16ms) or short (65us) debounce time at 8KHz sampling rate.

- Ramp-up-down enable or disable:
  When COUT is used for playback, Ramp-up-down should be enabled. This function eliminates the 'POP' noise at the begin and end of voice playback.
  When VOUT1 and VOUT2 are used to drive speaker directly, Ramp-up-down should be disabled.

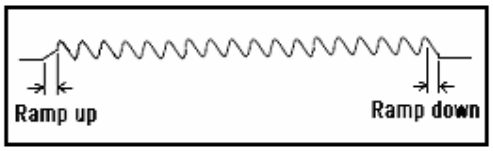

Fig. 1 Ramp-up-down Enable

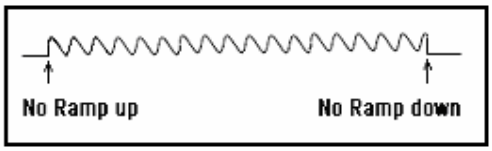

Fig.2 Ramp-up-down Disable

- Output Options:
  This option sets up the three output pins OUT1, OUT2 and OUT3 to send out different signals during voice playback. Four settings are allowed:

	OUT1	OUT2	OUT3
Option 1	LED1	LED2	BUSY
Option 2	STOP	LED1	LED2
Option 3	LED1	BUSY	STOP
Option 4	LED1	BUSY	BUSYB

Note: BUSY can be set or reset associated with each Voice Block. Stop plus must be set to enable in order to have STOP plus to come out at the end of playback.

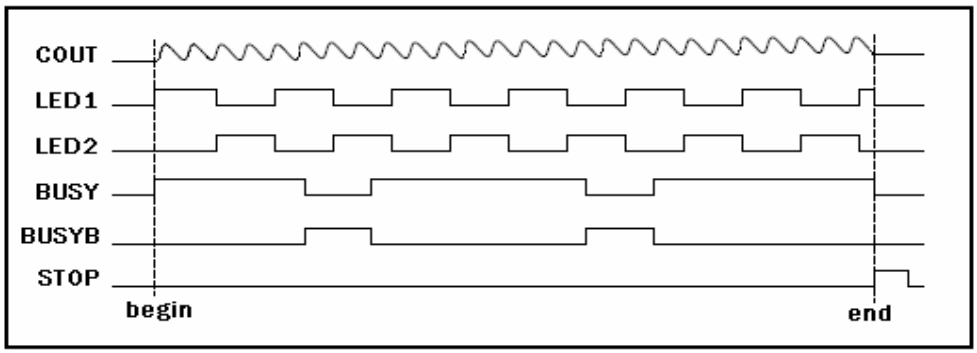

Fig. 3 Output waveforms

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Group Options

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable
- Stop pulse disable or enable

Fig. 4 to Fig. 9 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

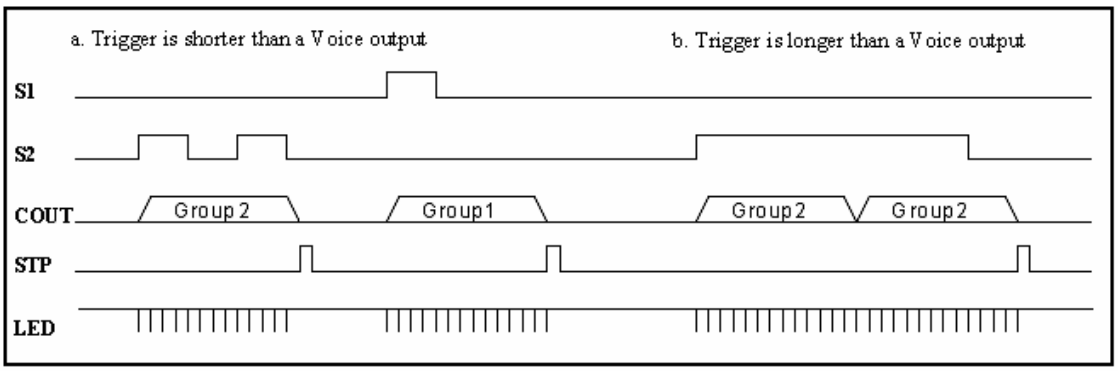

Fig. 4 Level, Unholdable, Non-retriggerable

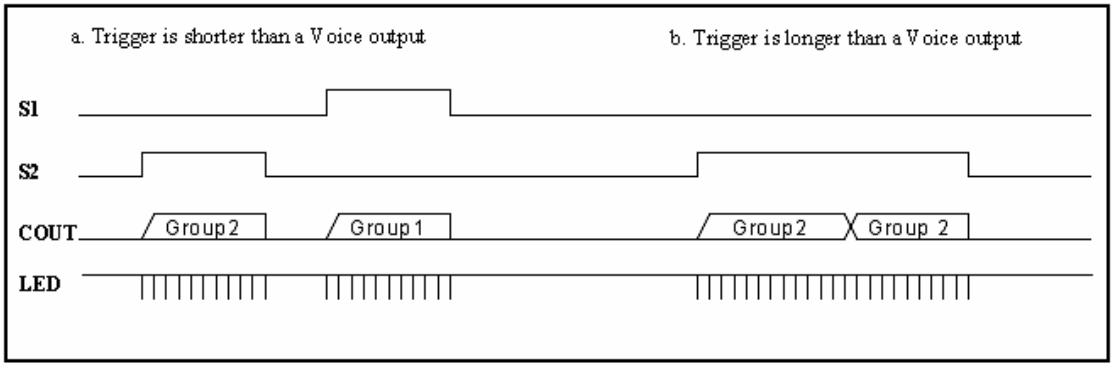

Fig. 5 Level Holdable

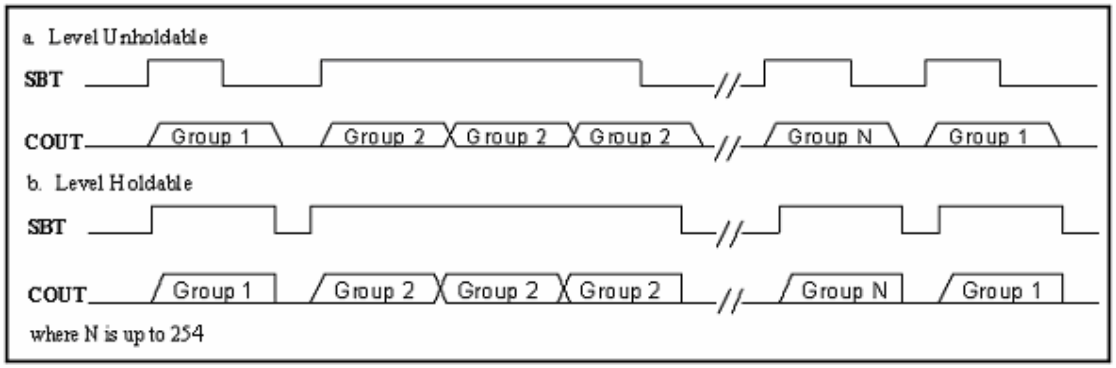

Fig. 6 SBT sequential trigger with Level Holdable and Unholdable

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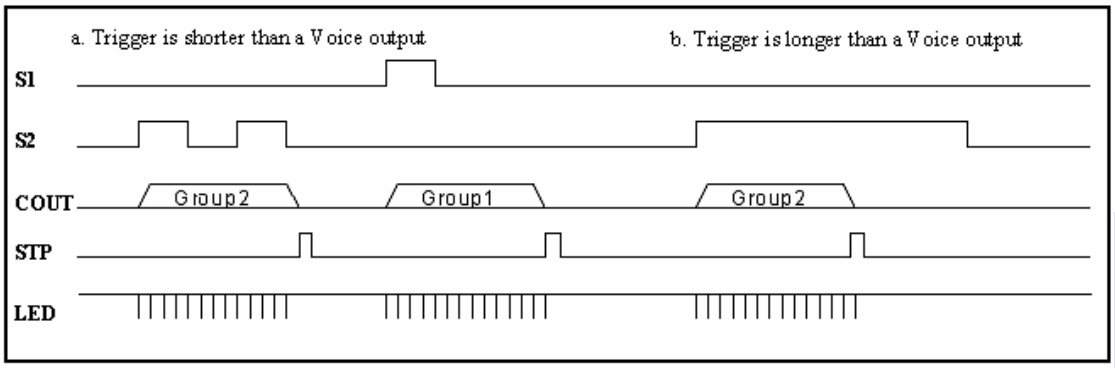

Fig. 7 Edge, Unholdable, Non-retrigger

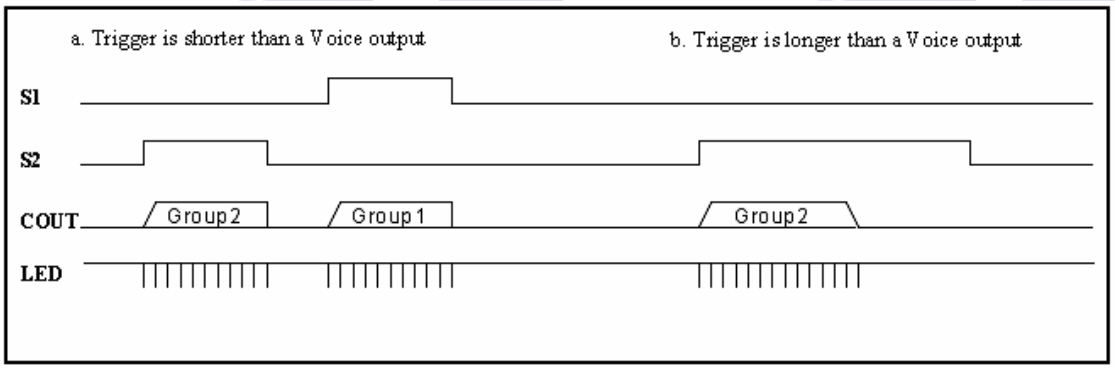

Fig. 8 Edge, Holdable

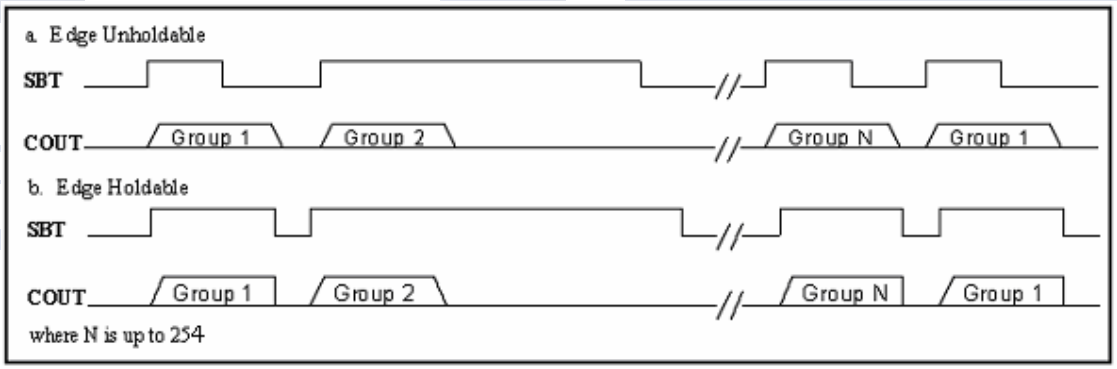

Fig. 9 SBT sequential trigger with Edge Holdable and Unholdable

TRIGGER MODES

There are three trigger modes available for aP89341/170/085 series which are determined by setting M1 and M2 pins to logic HIGH or LOW.

- Key Trigger Mode (M1=0; M0=0);
- CPU Parallel Trigger Mode (M1=0; M0=1);
- CPU Serial Command Mode (M1=1; M0=0);

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Key Trigger Mode (M1=0, M0=0)

With this trigger mode, the beginning 32 Voice Groups are triggered by setting S1 to S8 to HIHG or LOW in different combinations. Each Voice Group can have its only independent trigger options (See Fig. 4, 5, 7 and 8 for trigger options definition).

A maximum of 254 Voice Groups are available. The 33rd to 254th Voice Groups can only be triggered one by one sequentially with the SBT key (See Fig. 6 and 9).

The setting of S1 to S8 for triggering the 1st to the 32nd Voice Groups are as follow:

Voice Group	S1	S2	S3	S4	S5	S6	S7	S8
1	HIGH	NC	NC	NC	NC	NC	NC	NC
2	NC	HIGH	NC	NC	NC	NC	NC	NC
3	NC	NC	HIGH	NC	NC	NC	NC	NC
4	NC	NC	NC	HIGH	NC	NC	NC	NC
5	NC	NC	NC	NC	HIGH	NC	NC	NC
6	NC	NC	NC	NC	NC	HIGH	NC	NC
7	NC	NC	NC	NC	NC	NC	HIGH	NC
8	NC	NC	NC	NC	NC	NC	NC	HIGH
9	HIGH	HIGH	NC	NC	NC	NC	NC	NC
10	NC	HIGH	HIGH	NC	NC	NC	NC	NC
11	NC	NC	HIGH	HIGH	NC	NC	NC	NC
12	NC	NC	NC	HIGH	HIGH	NC	NC	NC
13	NC	NC	NC	NC	HIGH	HIGH	NC	NC
14	NC	NC	NC	NC	NC	HIGH	HIGH	NC
15	NC	NC	NC	NC	NC	NC	HIGH	HIGH
16	HIGH	NC	NC	NC	NC	NC	NC	HIGH
17	HIGH	HIGH	HIGH	NC	NC	NC	NC	NC
18	NC	HIGH	HIGH	HIGH	NC	NC	NC	NC
19	NC	NC	HIGH	HIGH	HIGH	NC	NC	NC
20	NC	NC	NC	HIGH	HIGH	HIGH	NC	NC
21	NC	NC	NC	NC	HIGH	HIGH	HIGH	NC
22	NC	NC	NC	NC	NC	HIGH	HIGH	HIGH
23	HIGH	NC	NC	NC	NC	NC	HIGH	HIGH
24	HIGH	HIGH	NC	NC	NC	NC	NC	HIGH
25	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	NC
26	NC	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
27	NC	NC	HIGH	HIGH	HIGH	HIGH	NC	NC
28	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	NC
29	NC	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
30	HIGH	NC	NC	NC	NC	HIGH	HIGH	HIGH
31	HIGH	HIGH	NC	NC	NC	NC	HIGH	HIGH
32	HIGH	HIGH	HIGH	NC	NC	NC	NC	HIGH

Note: NC represents open or no connection

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CPU Parallel Trigger Mode (M1=0, M0=1)

In this mode, S8 to S1 serve as 8-bit addresses input for 254 Voice Groups with S8 represents the MSB and S1 represents LSB. After Group address is set and ready, setting the SBT input pin to HIGH will trigger the corresponding Voice Group to playback.

Trigger options defined in Fig. 4, 5, 7 and 8 are valid for this mode.

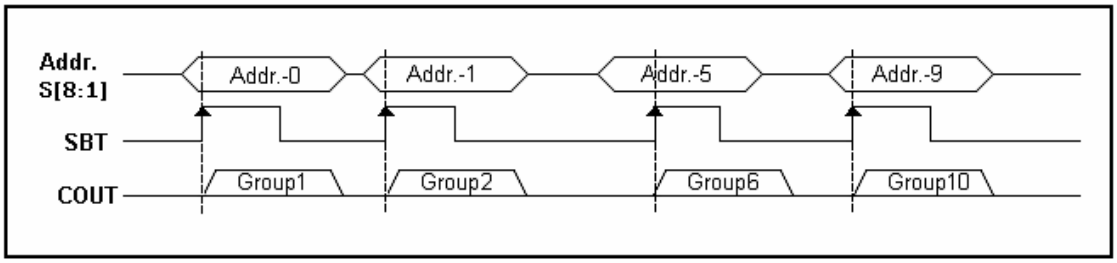

Fig. 10 CPU Parallel Trigger Mode

Note that SBT pin cannot be used as Single Button Sequential trigger in this mode. In stead, it acts as a Strobe input to clock-in the Voice Group address set at S8 to S1 into the chip.

Voice Groups are represented in Binary address format. For example:

S[8:1] = 0000 0000 (00hex) for Voice Group #1
S[8:1] = 0000 0001 (01hex) for Voice Group #2
• • •
S[8:1] = 0000 1000 (08 hex) for Voice Group #9
• • •
S[8:1] = 1000 1000 (88 hex) for Voice Group #137
• • •
S[8:1] = 1111 1101 (FD hex) for Voice Group #254

CPU Serial Command Mode (M1=1, M0=0)

This trigger mode is specially designed for simple CPU interface. The aP89341/170/085 is controlled by command sent to it from the host CPU. S1 to S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S1 acts as CS (Chip Select) to initiate the command word input
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state.
- OUT2 acts as POUT to output user selected information.
- OUT3 acts as FULL signal to indicate the Voice Group address buffer is full.

Command input into the chip may contains 8-bit or 16-bit data. The first 8-bit data is command bits while the second 8-bit data (if any) is the Voice Group address data. Table 1 summarize the available commands and their functions.

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Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1 (C5h)	1	1	0	0	0	1	0	1	Power up the chip with NO ramp-up (suitable for VOUT direct drive)
PUP2 (8Dh)	1	0	0	0	1	1	0	1	Power up the chip WITH ramp-up (suitable for COUT transistor drive)
PDN1 (E1h)	1	1	1	0	0	0	0	1	Power down the chip with NO ramp-down (suitable for VOUT direct drive)
PDN2 (A9h)	1	0	1	0	1	0	0	1	Power down the chip WITH ramp-down (suitable for COUT transistor drive)
STATUS (E3h)	1	1	1	0	0	0	1	1	Set output status for OUT2 pin
	0	0	0	1	0	G2	G1	G0	OUT2 = BUSYB (000), 8K (001), 4K, 2K, 1K, 16Hz, 1M, EMPTY (FULLB)
PAUSE (39h)	0	0	1	1	1	0	0	1	Pause the playback and hold at current COUT value
RESUME (1Dh)	0	0	0	1	1	1	0	1	Resume playback from the previous COUT value
PREFETCH (71h)	0	1	1	1	0	0	0	1	Pre-load Voice Group address into buffer for next playback
	G7	G6	G5	G4	G3	G2	G1	G0	Voice Group address (G7=MSB; G0=LSB)

- Power up with RAMP-UP (PU2-C5H) or without RAMP-UP (PU1-8DH)

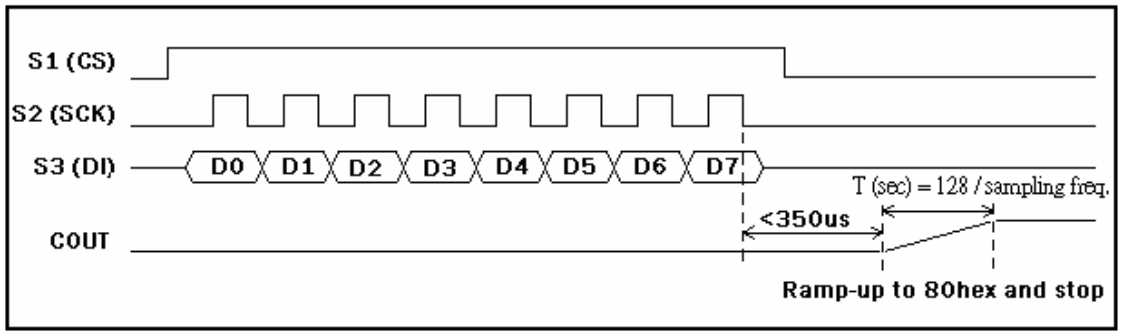

Fig. 11 Power-up command timing

1. PU1 (C5H) will power-up the chip and set the COUT to 80H immediately and stay there.
2. PU2 (8DH) will Ramp-up chip and ramp-up COUT from 00H to 80H and stay there.
3. Power-up will start after 350us (at 6KHz sampling rate).
4. Voice will be playback immediately after PU1 / PU2 completes if the section buffer is filled with the PREFETCH command before power-up.
5. OUT1 (BUSY) will output logic HIGH during Ramp-up operation.
6. PDN2 (Power-down with ramp-down) will be executed correctly only if PU2 is executed before.

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- Power-down with RAMP-DOWN (PD2-A9H) or without RAMP-DOWN (PD1-E1H)

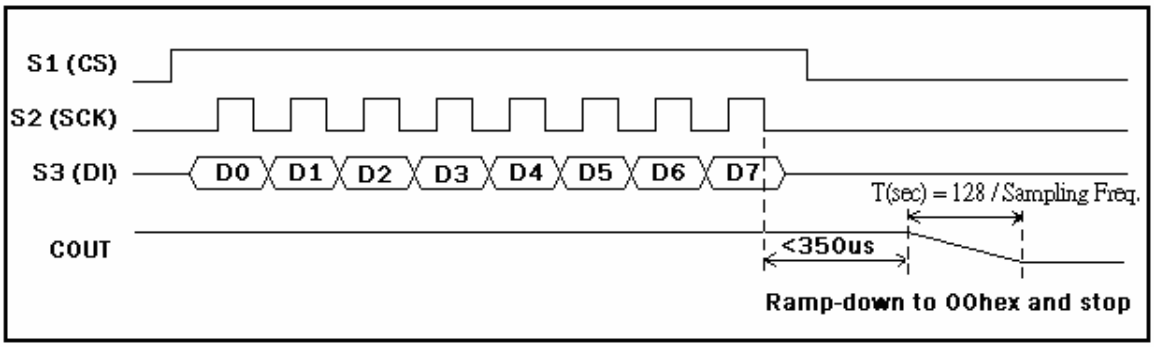

Fig. 12 Power-down commands timing

1. PDN1 will power-down the chip and set the COUT data to 00H immediately.
2. PDN2 will power-down the chip by Ramp-down the COUT from its current value to 00H.
3. Power-down will start after 350us (at 6KHz sampling rate).
4. The OUT1 pin (BUSY) will output logic HIGH during Ramp-down operation.
5. PDN2 (Power-down with ramp-down) will be executed correctly only if PU2 is executed before.

- Set OUT2 pin status (STATUS-E3H)

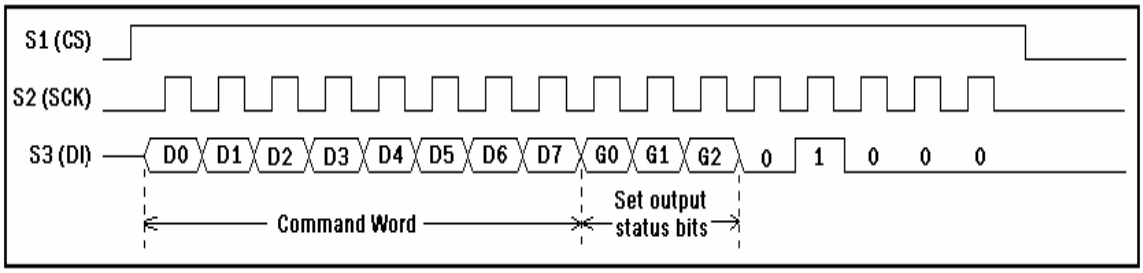

Fig. 14 Setup the status of programmable output pin, OUT2

1. Signal output from the pin, OUT2, is defined by G[3:0], as below:

G[3:0]	OUT2	G[3:0]	OUT2
000	BUSYB	100	1KHz
001	8KHz	101	16Hz
010	4KHz	110	1MHz
011	2KHz	111	FULLB

2. If the STATUS is not executed, default value of OUT2 is the internal Reset signal.
3. BUSYB is the logical inversion of BUSY.
4. EMPTY (or FULLB) is the logical inversion of FULL.
5. Only the 1MHz clock will not be stopped by the PAUSE command.

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- Pause and Resume (PAUSE-39H; RESUME-1DH)

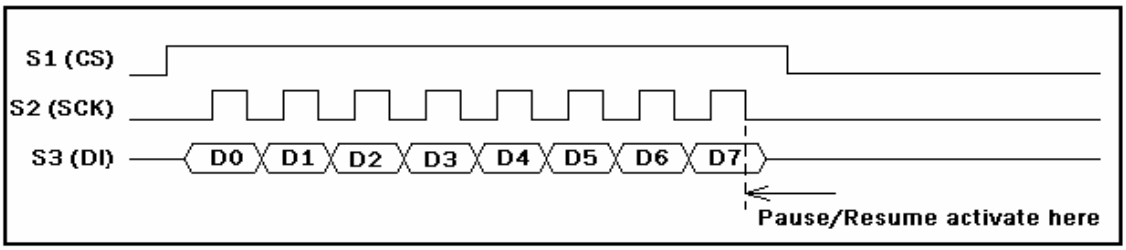

Fig. 15 Pause and Resume command timing

6. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level (i.e. COUT is kept outputting an DC current). When Resume, the COUT data will continue at the current D/A data level.
7. The Pause state will be released by PDN1, PDN2 and RESUME commands.

- Prefetch Voice Group Address (PREFETCH-71H)

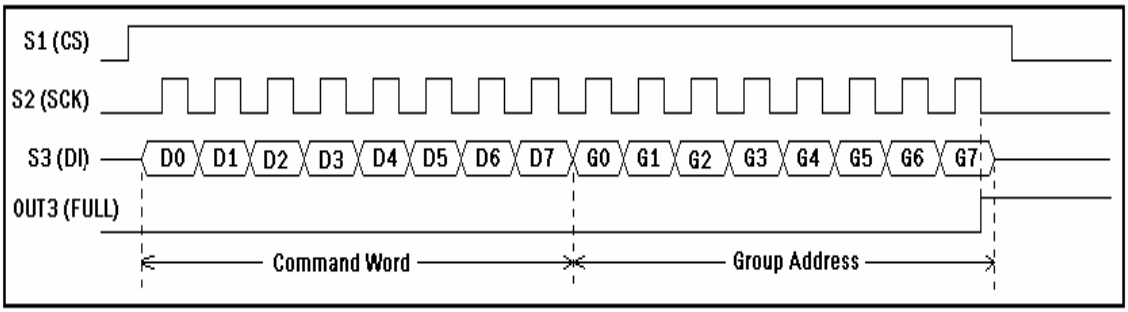

Fig. 16 Prefetch next Voice Group timing

1. The PREFETCH command pre-load the next Voice Group Address into the address buffer.
2. The OUT3 output (FULL) will become logic HIHG once the Group Address is successfully loaded.
3. The Voice Group will be played once the playing of the current Voice Group is finished.
4. The FULL signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next PREFECT action.
5. Using the PREFECT make sure there is no gap between each Voice Group.

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BLOCK DIAGRAM

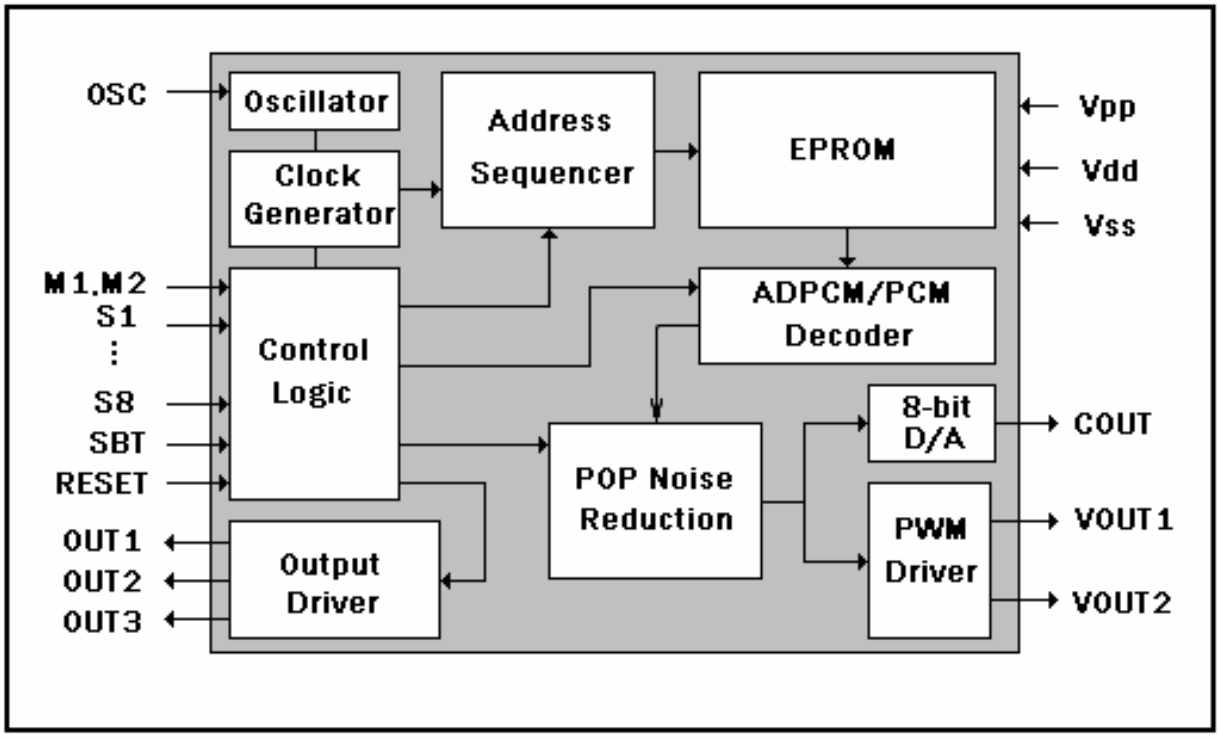

Fig. 17 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +3.8	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating):	-40 ~ +85	℃
T (Junction)	-40 ~ +125	℃
T (Storage)	-55 ~ +125	℃

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DC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.3V, V_{SS} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.2	3.0	3.6	V	
I_{SB}	Standby current	—	1	5	μA	I/O open
I_{OP}	Operating current	—	—	15	mA	I/O open
V_{IH}	"H" Input Voltage	2.5	3.0	3.5	V	V_{DD}=3.0V
V_{IL}	"L" Input Voltage	-0.3	0	0.5	V	V_{DD}=3.0V
I_{OL}	V_{OUT} low O/P Current	—	120	—	mA	Vout=0.3V
I_{OH}	V_{OUT} high O/P Current	—	-65	—	mA	Vout=2.5V
I_{CO}	C_{OUT} O/P Current	—	-3	—	mA	V_{COUT}=1.0V
I_{OH}	O/P high Current	—	-8	—	mA	V_{OH}=2.5V
I_{OL}	O/P low Current	—	8	—	mA	V_{OL}=0.3V
ΔF/F	Frequency Stability	-5	—	+5	%	$\frac{Fosc(2.7V) - Fosc(3.4V)}{Fosc(3V)}$

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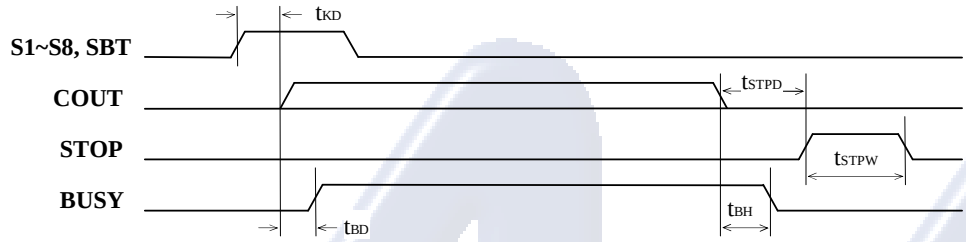
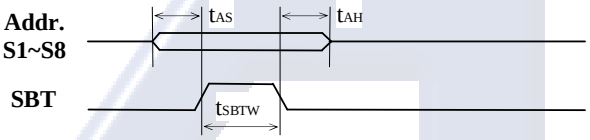
TIMING WAVEFORMS

KEY Trigger Mode



CPU Parallel Mode



CPU Serial Command Mode

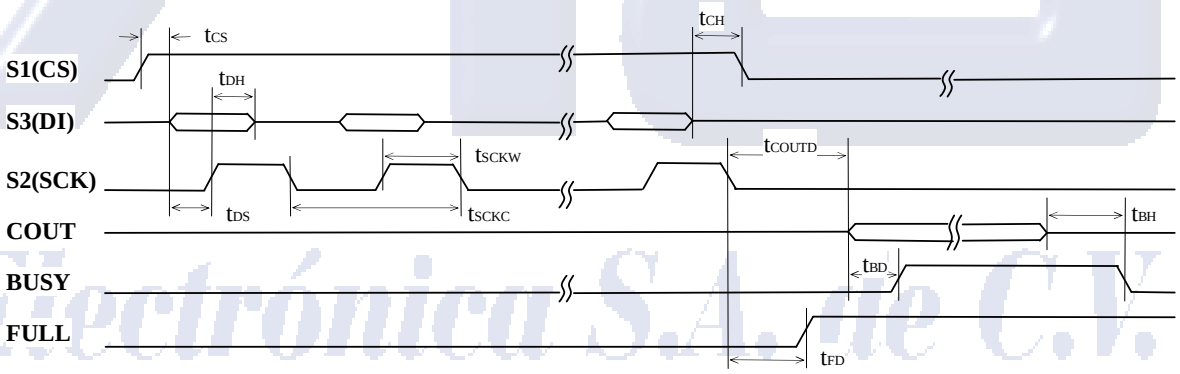


Fig. 18 Timing Waveform

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AC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.3V, V_{SS} = 0V, 8KHz sampling)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_{KD}	Key trigger debounce time (long)	16	—	—	ms	1,2
t_{KD}	Key trigger debounce time (long) – retrigger option	24	—	—	ms	1,2
t_{KD}	Key trigger debounce time (short)	65	—	—	μs	1,2
t_{KD}	Key trigger debounce time (short) – retrigger option	200	—	—	μs	1,2
t_{STPD}	STOP pulse output delay time	—	—	256	μs	
t_{STPW}	STOP pulse width	—	64	—	ms	1
t_{BD}	BUSY signal output delay time	—	—	100	ns	
t_{BH}	BUSY signal output hold time	—	100	—	ns	
t_{AS}	Address set-up time	100	—	—	ns	
t_{AH}	Address hold time	100	—	—	ns	
t_{SBTW}	SBT stroke pulse width (long)	16	—	—	ms	1,2
t_{SBTW}	SBT stroke pulse width (short)	65	—	—	μs	1,2
t_{CS}	Chip select set-up time	100	—	—	ns	
t_{CH}	Chip select hold time	100	—	—	ns	
t_{DS}	Data-in set-up time	100	—	—	ns	
t_{DH}	Data-in hold time	100	—	—	ns	
t_{SCKW}	Serial clock pulse width	1	—	—	μs	
t_{SCKC}	Serial clock cycle time	2	—	—	μs	
t_{COUTD}	COUT output delay time	—	—	256	μs	
t_{FD}	FULL signal output delay time	—	100	—	ns	
t_{LEDC}	LED flash frequency	—	3	—	Hz	3

Notes :
1. This parameter is inversely proportional to the sampling frequency.
2. The long or short debounce time is selectable as whole chip option during Voice Files Compiling.
3. This parameter is proportional to the sampling frequency.

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OSCILLATOR RESISTANCE TABLE

Sampling Frequency KHz	R_{OSC} KOhm
4.90	300
5.26	290
5.88	280
6.09	270
6.33	260
6.67	250
6.85	240
7.14	230
7.46	220
7.70	210
8.06	200
8.47	190
8.93	180
9.26	170
9.80	160
10.42	150

R_{OSC} KOhm	Sampling Frequency KHz
140	11.00
130	11.76
120	12.50
110	13.33
100	14.51
91	15.63
82	16.95
75	18.18
68	19.23
62	20.83
56	22.22
51	23.81
43	25.00

Note: The data in the above tables are within 3% accuracy and measured at V_{DD} = 3.0V. Oscillator frequency is subjected to IC lot to lot variation.

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TYPICAL APPLICATIONS

Key Trigger Mode

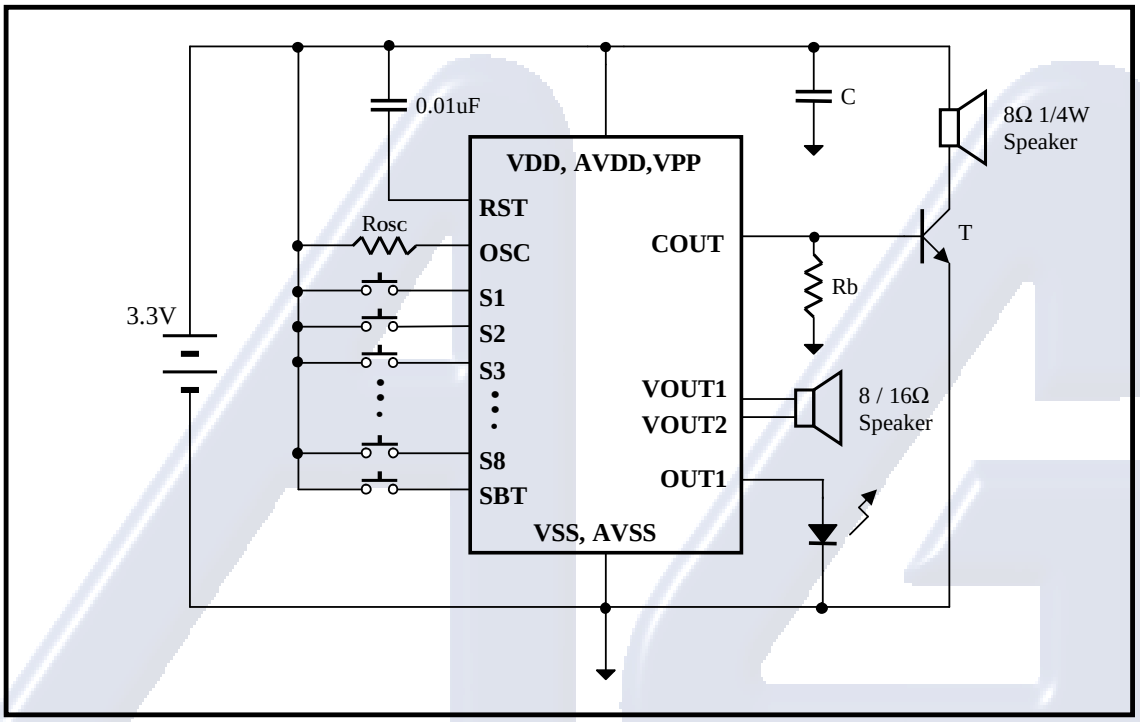

Fig. 22 Using 3.3V Battery

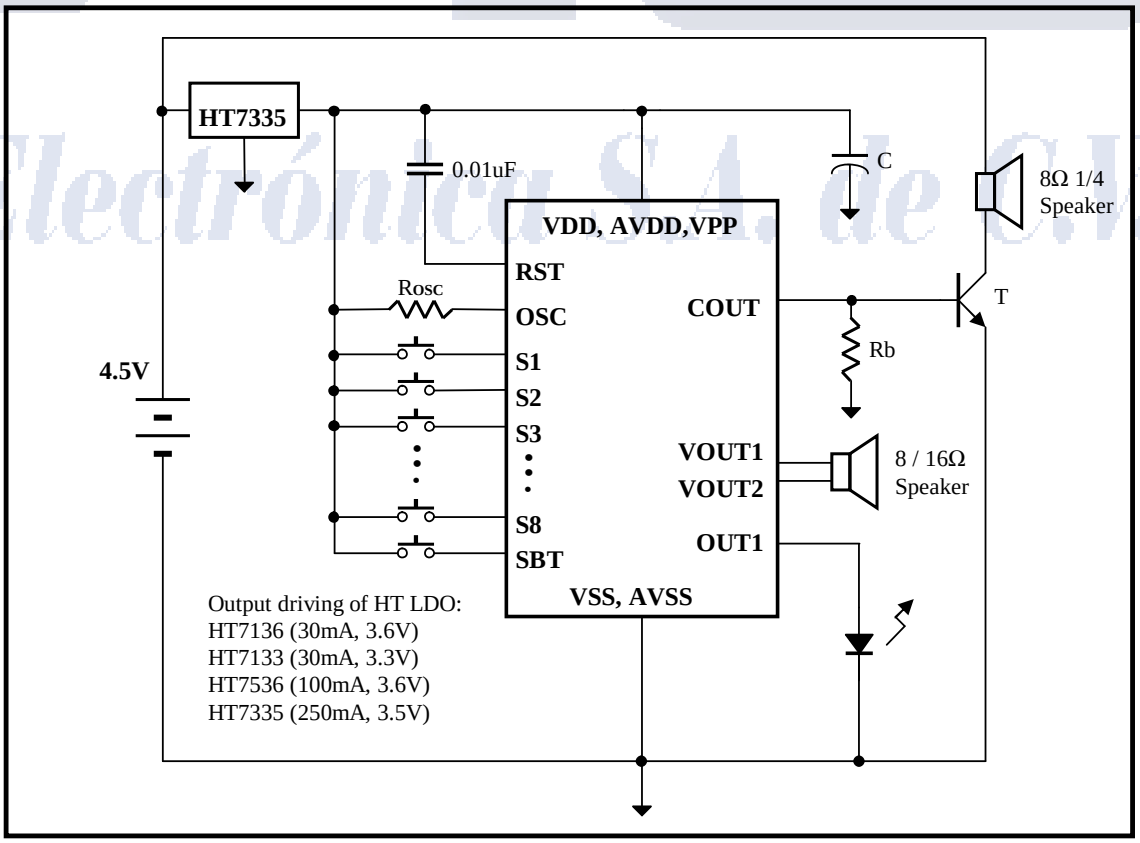

Fig. 23 Using 4.5V Battery

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CPU Parallel Mode

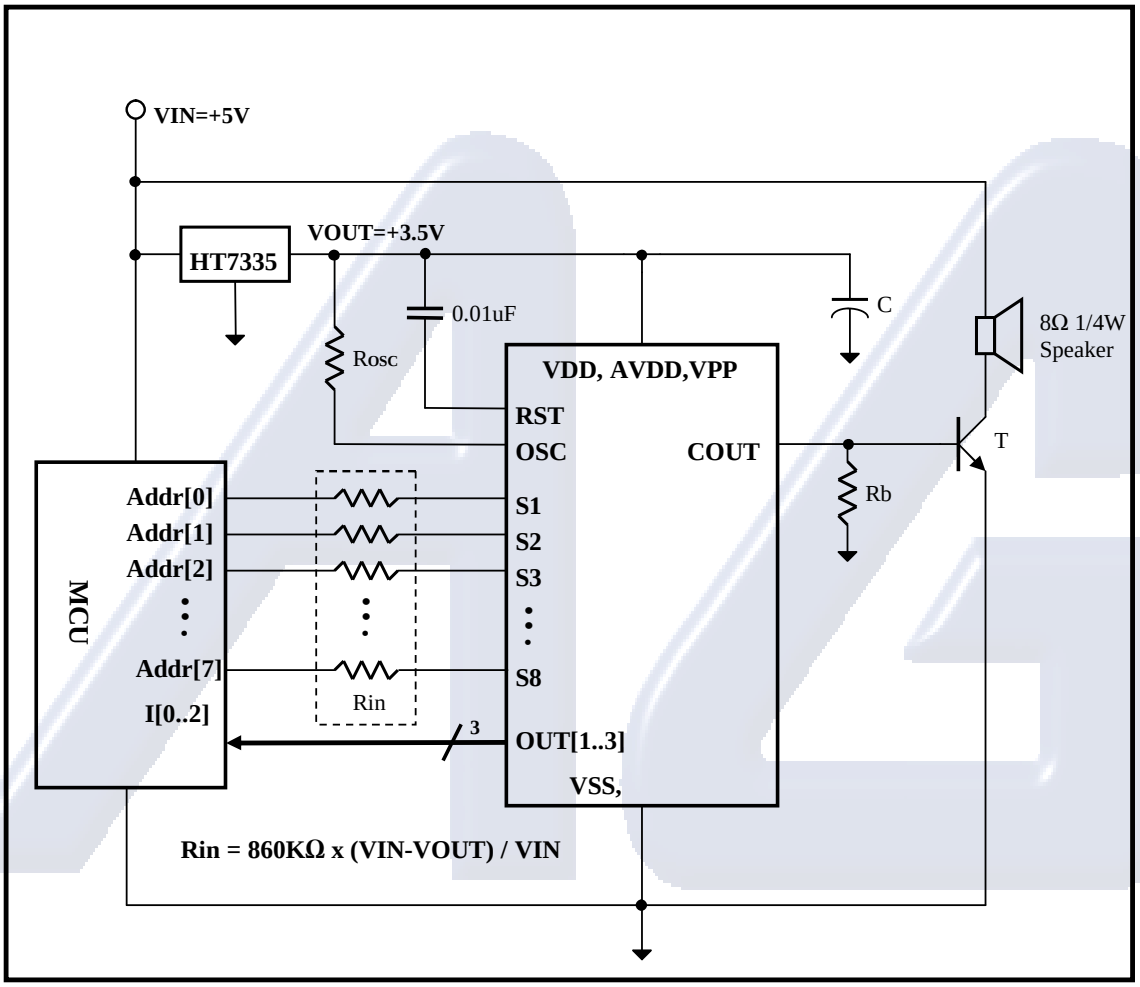

Fig. 24 5V CPU Control with COUT

Note:

1. C1 is capacitor from 0.1uF to 4.7uF depends on the kind of Vdd source and sound loudness.
2. Rb is base resistor from 120 Ohm to 390 Ohm depends on Vdd value and transistor gain.
3. T is an NPN transistor with beta larger than 150.
4. Reference value for the above components are C = 2.2uF, Rb = 390 Ohm and T = 8050D.
5. Refer to the Oscillator Resistor Table for suitable value of Rosc.

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CPU Serial Command Mode

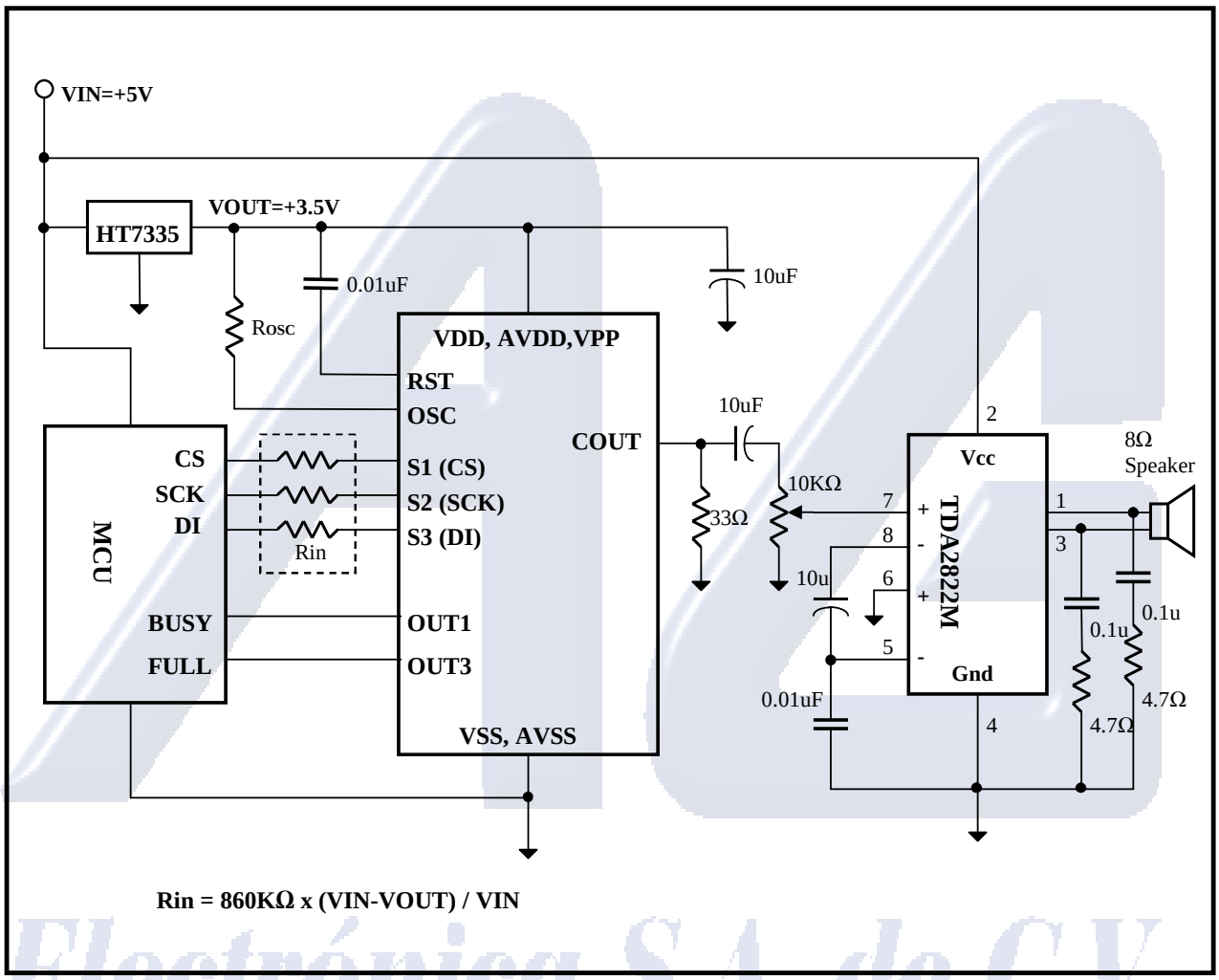

Fig. 25 5V CPU Control with TDA Power Amplifier

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BONDING PAD DIAGRAMS

Notes:

1. Two VPP pads should be connected to the Positive Power Supply during voice playback.
2. VDD and AVDD should be connected to the Positive Power Supply.
3. VSS and AVSS should be connected to the Power GND.
4. Substrate should be connected to the Power GND.

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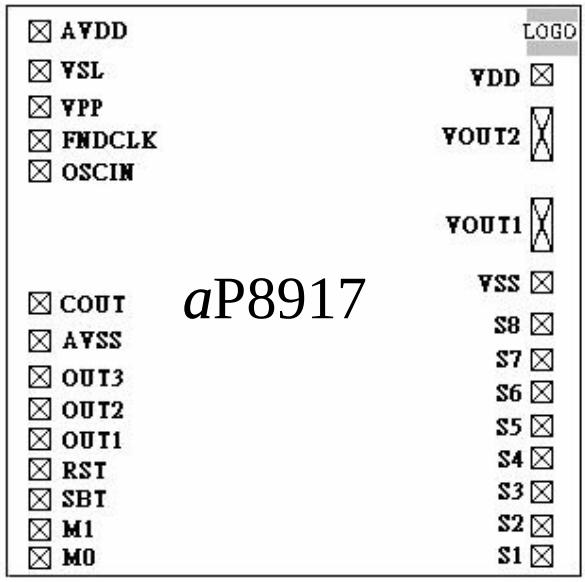

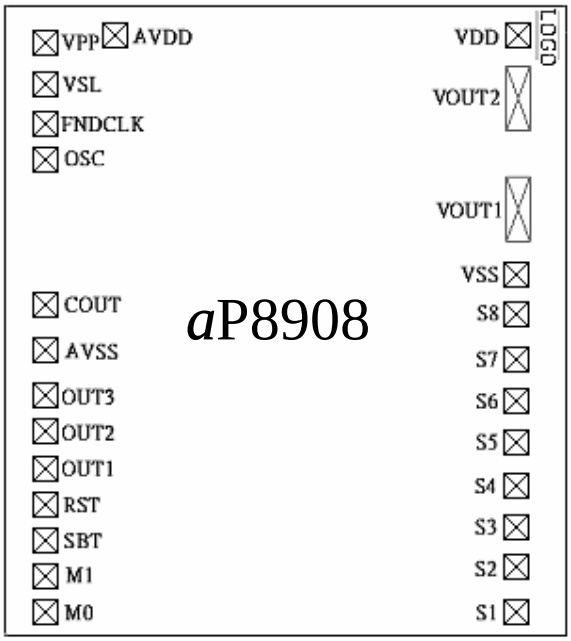

Notes:

5. VPP and VSL pads should be connected to the Positive Power Supply during voice playback.
6. VDD and AVDD should be connected to the Positive Power Supply.
7. VSS and AVSS should be connected to the Power GND.
8. Substrate should be connected to the Power GND.

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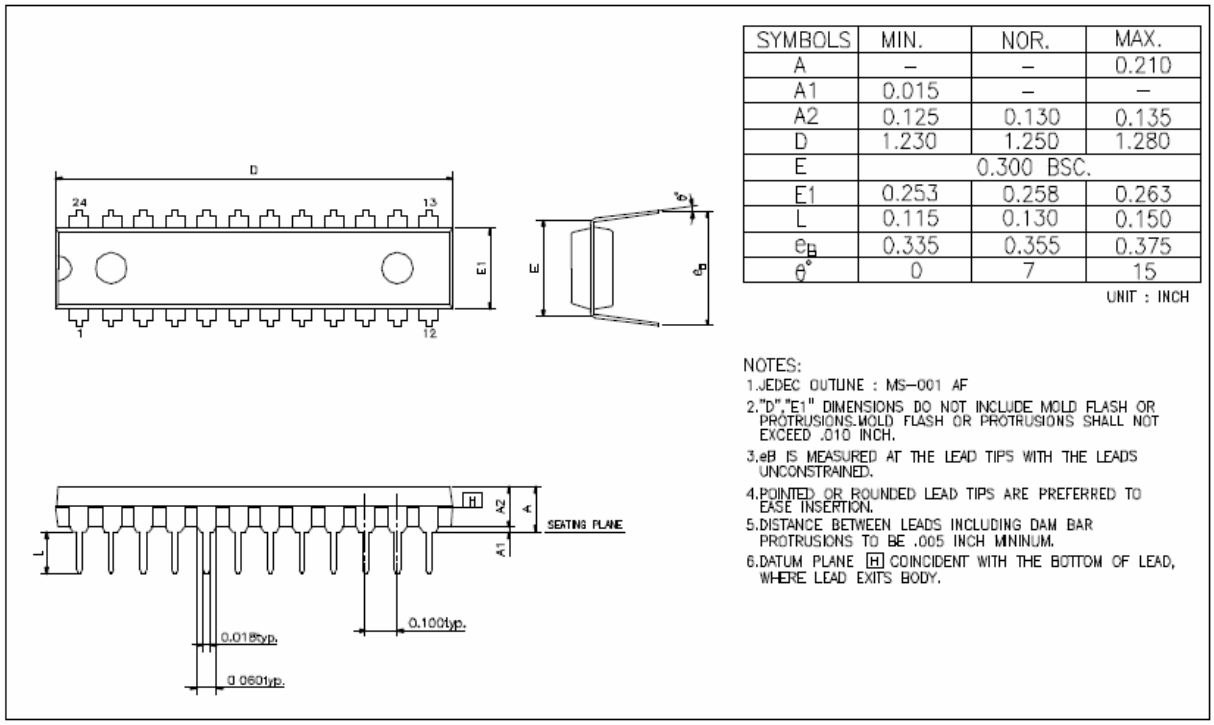
PACKAGES DIMENSION OUTLINES

24-Pin 300mil P-DIP Package

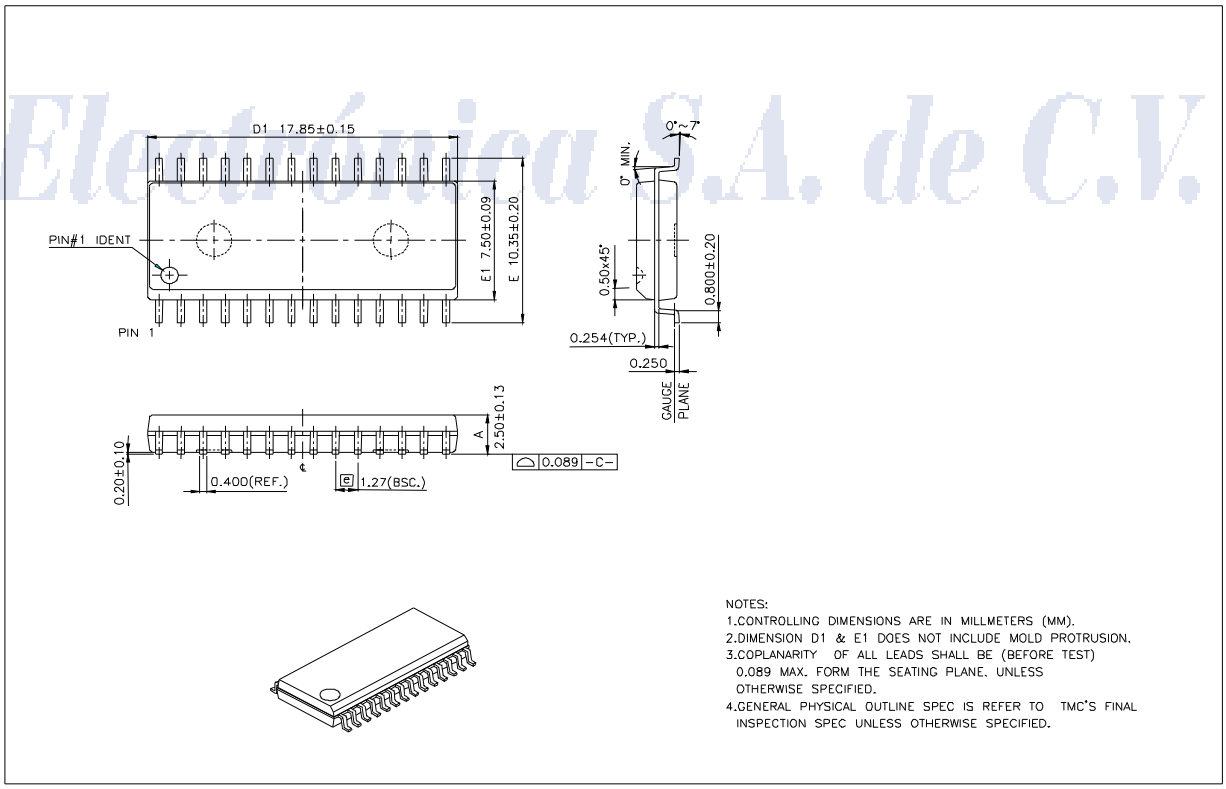


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E		0.300 BSC.	
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-001 AF
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

28-Pin 300mil SOP Package



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLMETERS (MM).
2. DIMENSION D1 & E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.089 MAX. FORM THE SEATING PLANE, UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

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