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Features

- **Industry Standard Architecture**
  - **Emulates Many 20-Pin PALs®**
  - **Low Cost Easy-to-Use Software Tools**
- **High-Speed Electrically Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**
- **Several Power Saving Options**

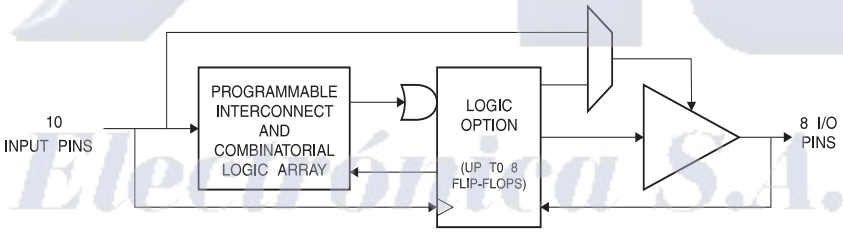
Device	I_{CC}, Stand-By	I_{CC}, Active
ATF16V8B	50 mA	55 mA
ATF16V8BQ	35 mA	40 mA
ATF16V8BQL	5 mA	20 mA

- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-Up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

High-Performance Flash PLD

ATF16V8B

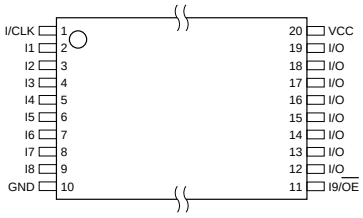
Block Diagram



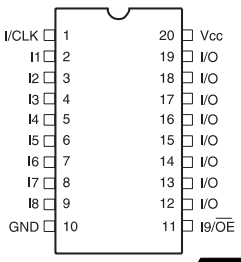
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
V_{CC}	+5 V Supply

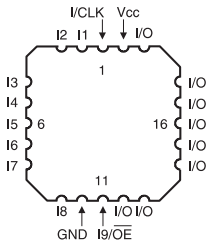
TSSOP Top View



DIP/SOIC



PLCC Top View



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Description

The ATF16V8B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns are offered. All speed ranges are specified over the full 5V ± 10% range for industrial temperature ranges, and 5V ± 5% for commercial temperature ranges.

Several low power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

The ATF16V8Bs incorporate a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%

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DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		55	85	mA
				Ind.		55	95	mA
			B-15, -25	Com.		50	75	mA
				Ind.		50	80	mA
			BQ-10	Com.		35	55	mA
			BQL-15, -25	Com.		5	10	mA
				Ind.		5	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f=15 MHz	B-7, -10	Com.		60	90	mA
				Ind.		60	100	mA
			B-15, -25	Com.		55	85	mA
				Ind.		55	95	mA
			BQ-10	Com.		40	55	mA
			BQL-15, -25	Com.		20	35	mA
				Ind.		20	40	mA
I_{OS}[1]	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OL} = -24 mA Com., Ind.				0.5	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

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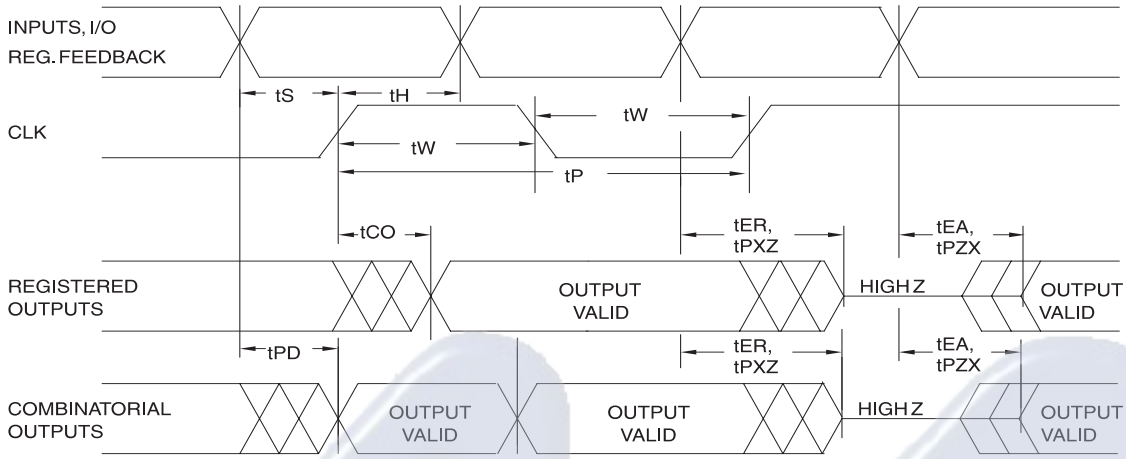
AC Waveforms(1)



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V 3.0V, unless otherwise specified.

AC Characteristics(1)

Symbol	Parameter		-7(2)		-10		-15		-25		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output	8 outputs switching	3	7.5	3	10	3	15	3	25	ns
		1 output switching		7							ns
t_{CF}	Clock to Feedback			3		6		8		10	ns
t_{CO}	Clock to Output		2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Setup Time		5		7.5		12		15		ns
t_H	Hold Time		0		0		0		0		ns
t_P	Clock Period		8		12		16		24		ns
t_W	Clock Width		4		6		8		12		ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			100		68		45		37	MHz
	Internal Feedback $1/(t_S + t_{CF})$			125		74		50		40	MHz
	No Feedback $1/(t_P)$			125		83		62		41	MHz
t_{EA}	Input to Output Enable — Product Term		3	9	3	10	3	15	3	20	ns
t_{ER}	Input to Output Disable — Product Term		2	9	2	10	2	15	2	20	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	6	2	10	2	15	2	20	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	6	1.5	10	1.5	15	1.5	20	ns

Notes: 1. See ordering information for valid part numbers and speed grades.
2. Recommend ATF16V8C-7.

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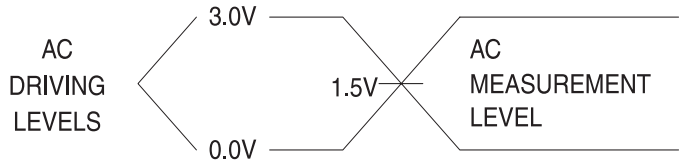
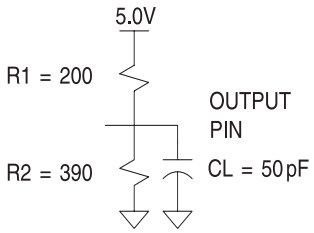
Input Test Waveforms and Measurement Levels:



t_R, t_F < 5 ns (10% to 90%)

Output Test Loads:

Commercial



Pin Capacitance

f = 1 MHz, T = 25°C[1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

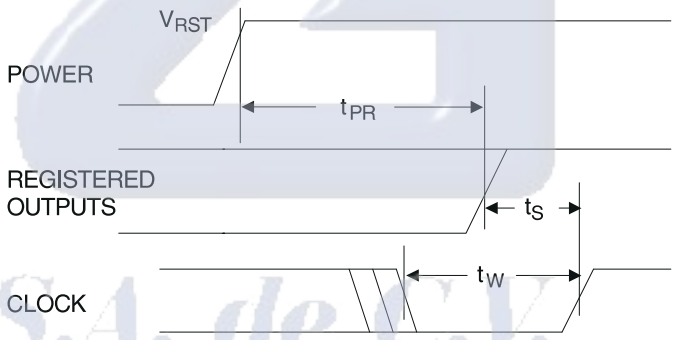
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF16V8Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3) The clock must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF16V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

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Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

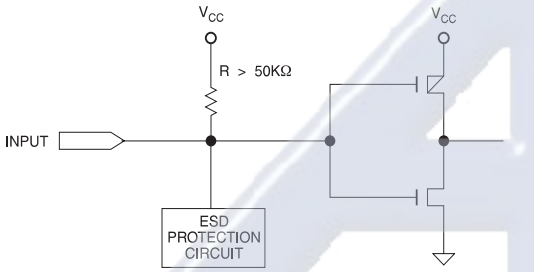
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware and Software Support* for information on software/programming.

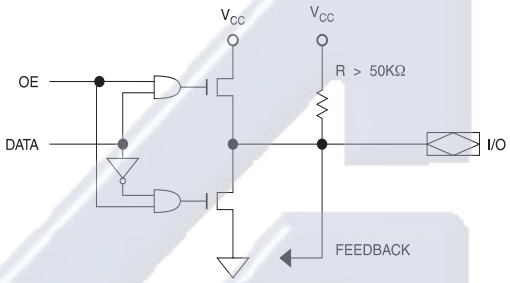
Input and I/O Pull-Ups

All ATF16V8B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to V_{CC}. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8B can be configured in one of three different modes. Each mode makes the ATF16V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF16V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R(1)	GAL16V8_C7(1)	GAL16V8_C8(1)	GAL16V8
OrCAD-PLD	“Registered”	“Complex”	“Simple”	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Only applicable for version 3.4 or lower.

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Macrocell Configuration

Software compilers support the three different OMC modes as different device types. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

ATF16V8B Registered Mode

PAL Device Emulation / PAL Replacement

The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

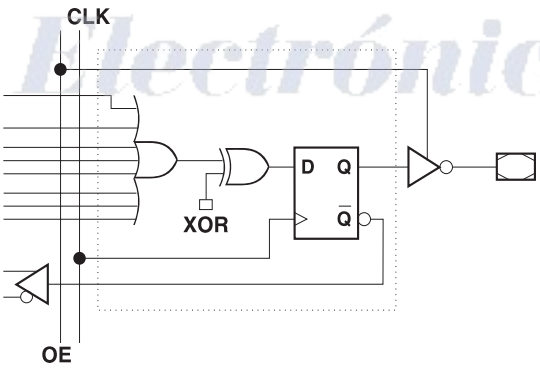
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

16R8 16RP8

16R6 16RP6

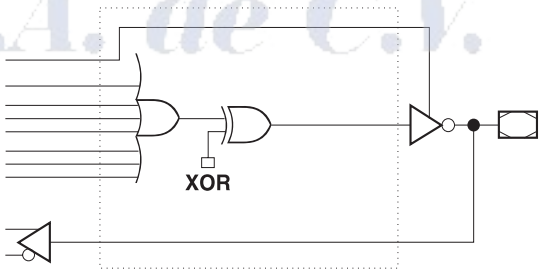
16R4 16RP4

Registered Configuration for Registered Mode(1)(2)



Notes:
1. Pin 1 cotrols common CLK for the registered outputs. Pin 11 controls common $\overline{OE}$ for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Combinatorial Configuration for Registered Mode(1)(2)



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

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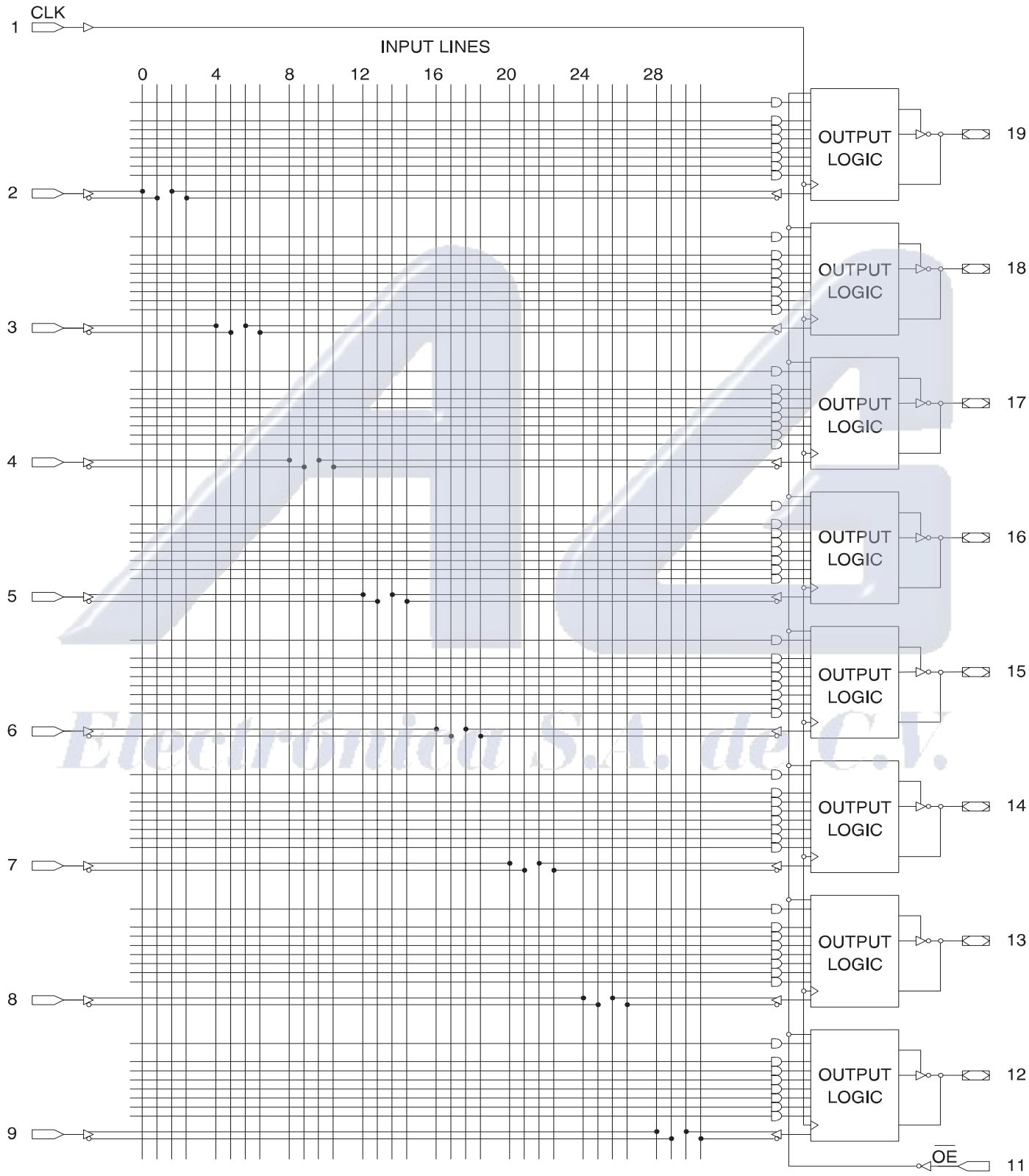
Registered Mode Logic Diagram



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ATF16V8B Complex Mode

PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

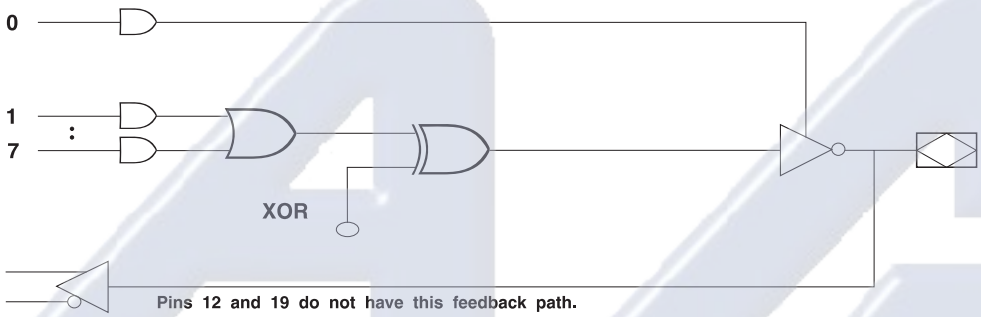
Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8

16H8

16P8

Complex Mode Option



ATF16V8B Simple Mode

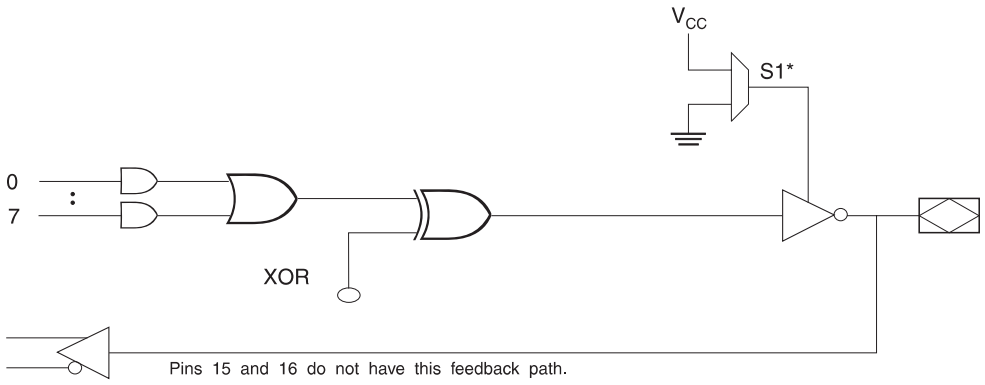
PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

10L8	10H8	10P8
12L6	12H6	12P6
14L4	14H4	14P4
16L2	16H2	16P2

Simple Mode Option



* - Pins 15 and 16 are always enabled.

* - Pins 15 and 16 are always enabled.

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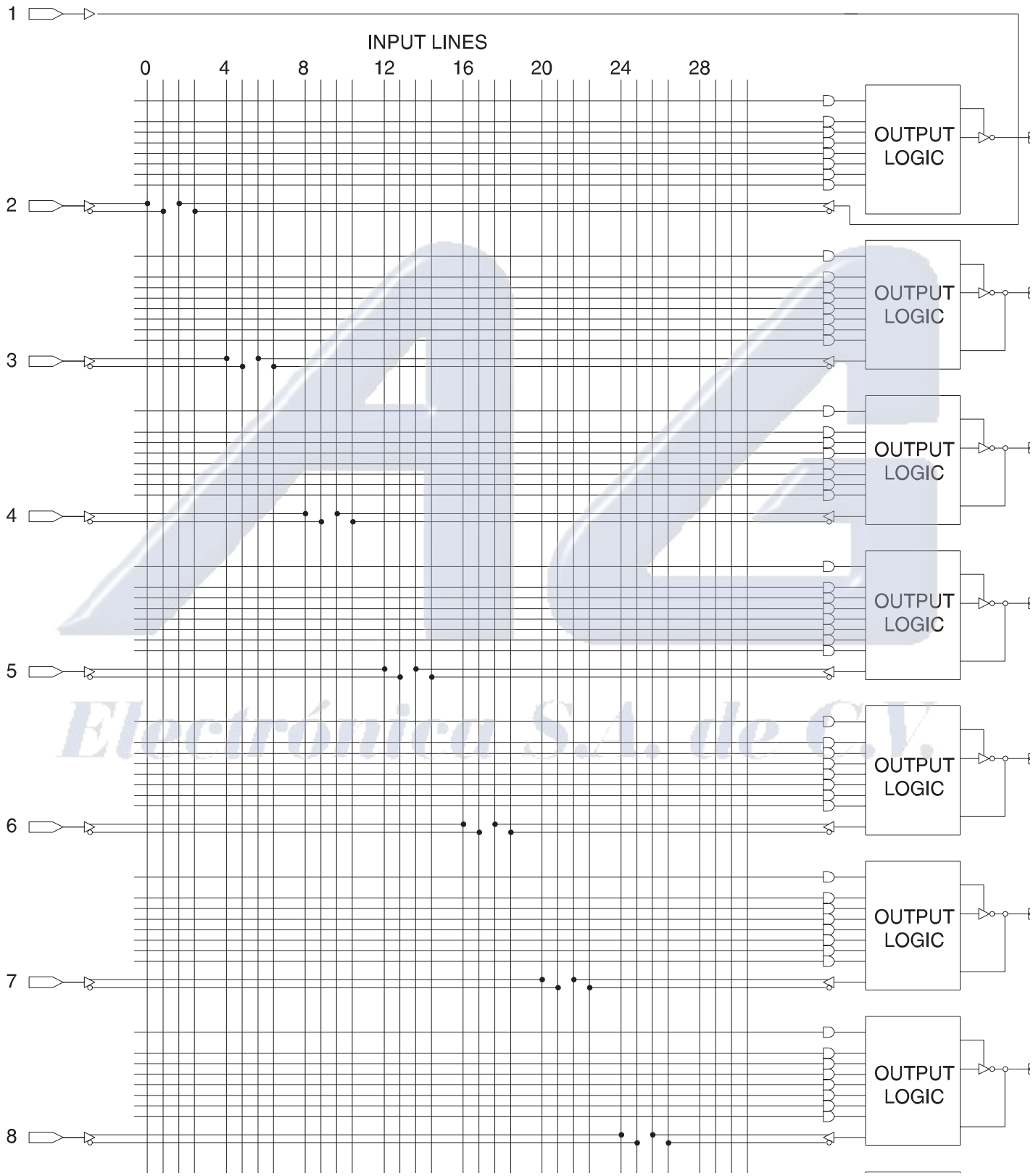
Complex Mode Logic Diagram



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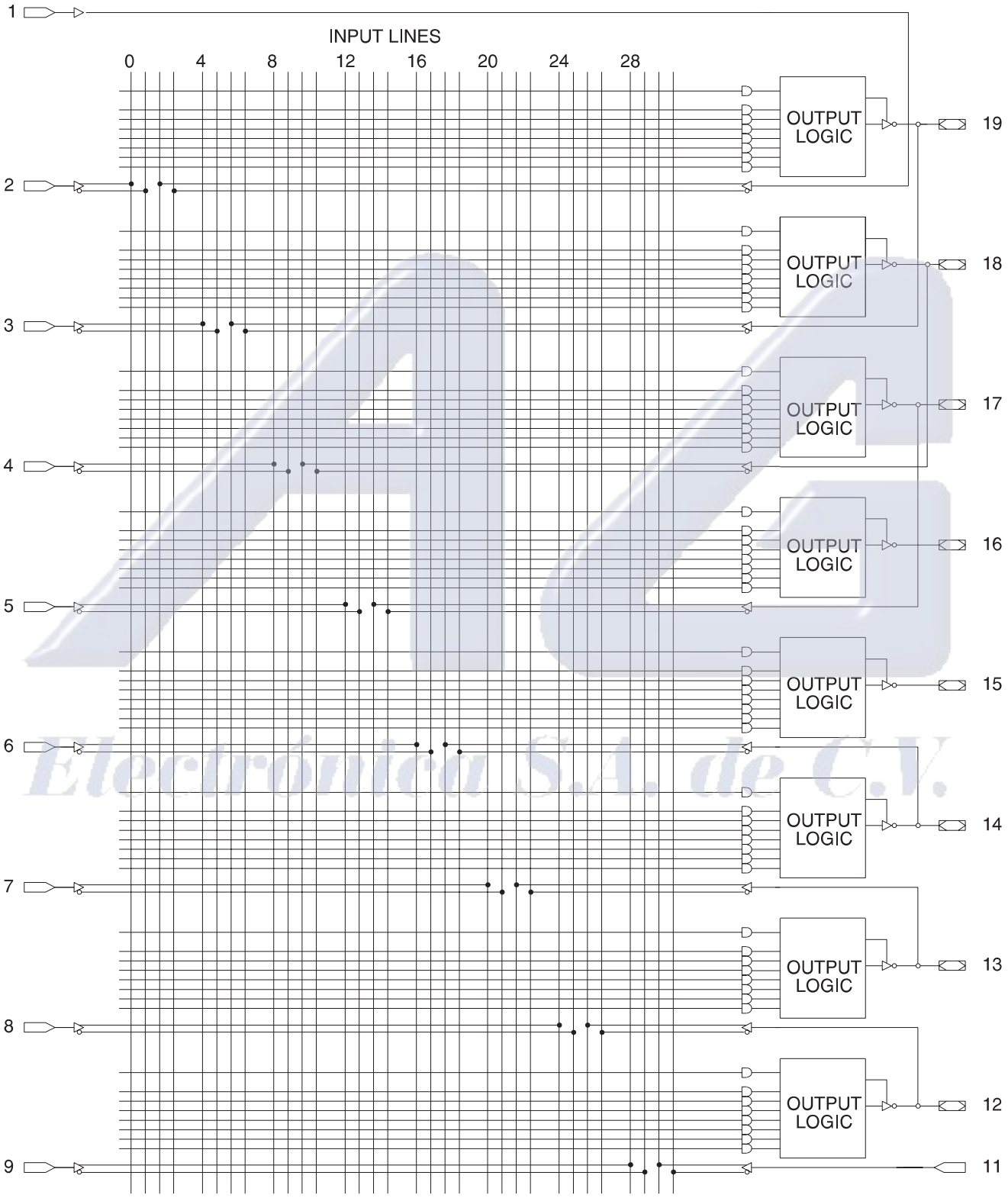
Simple Mode Logic Diagram



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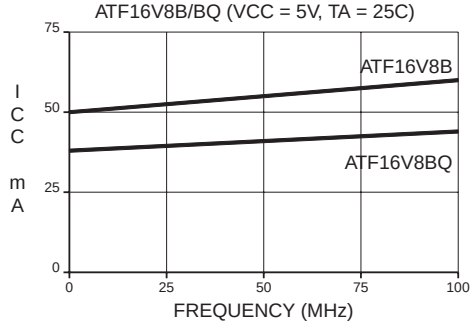
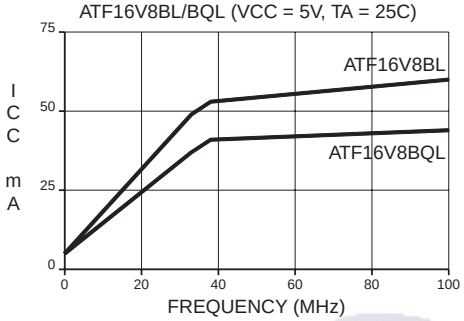
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8B/BQ (VCC = 5V, TA = 25C)



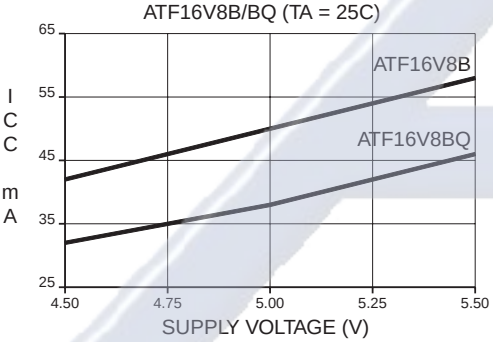
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8BL/BQL (VCC = 5V, TA = 25C)



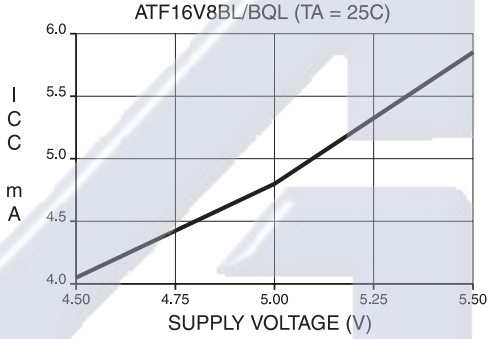
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8B/BQ (TA = 25C)



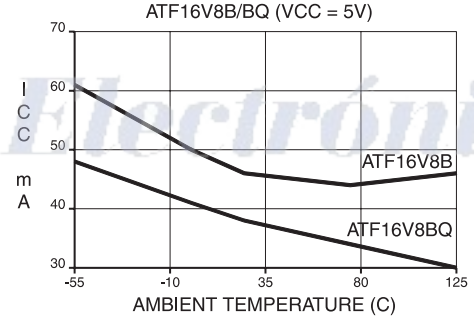
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8BL/BQL (TA = 25C)



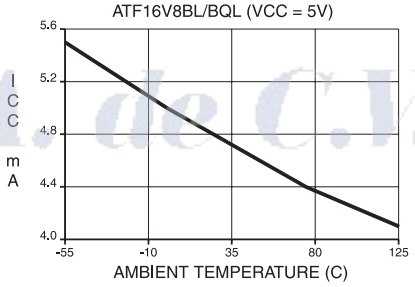
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8B/BQ (VCC = 5V)



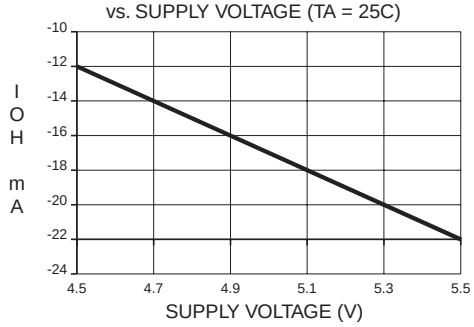
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8BL/BQL (VCC = 5V)



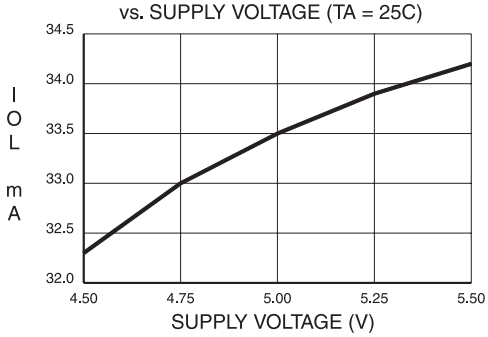
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



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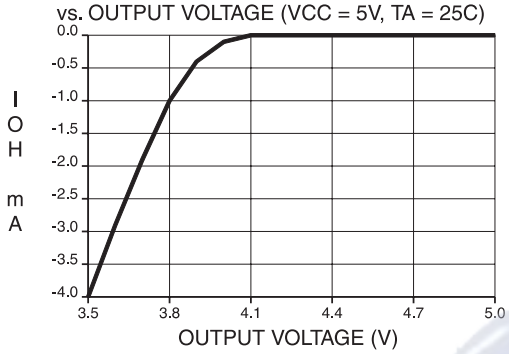
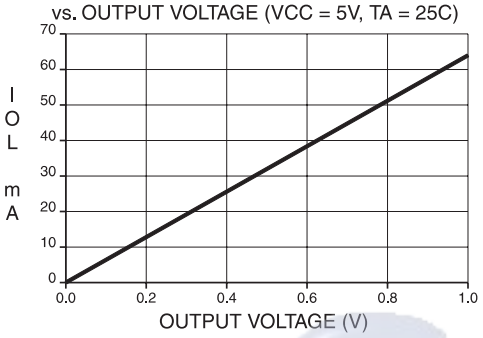
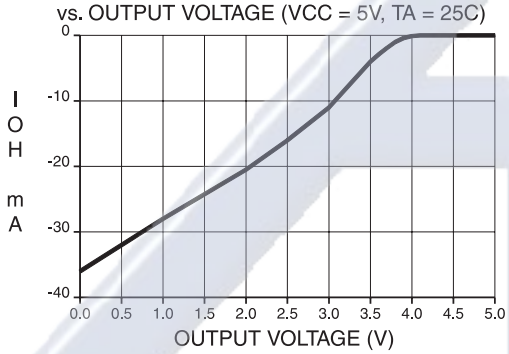
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



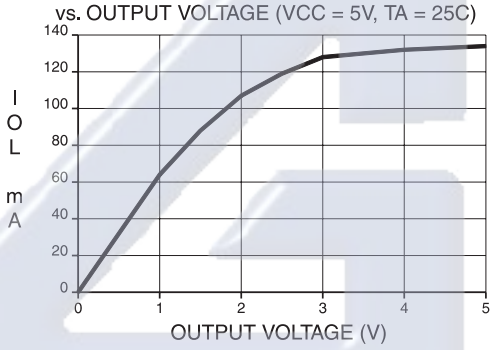
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



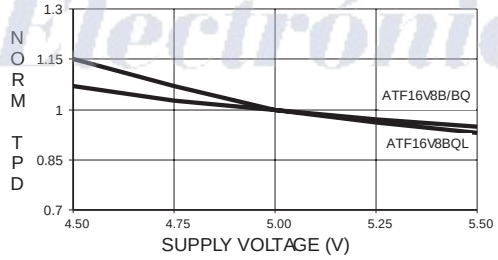
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



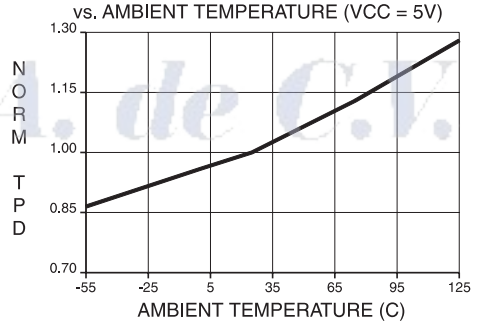
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



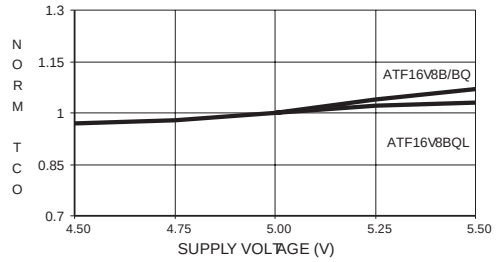
NORMALIZED TPD
vs. SUPPLY VOLTAGE (TA=25°C)



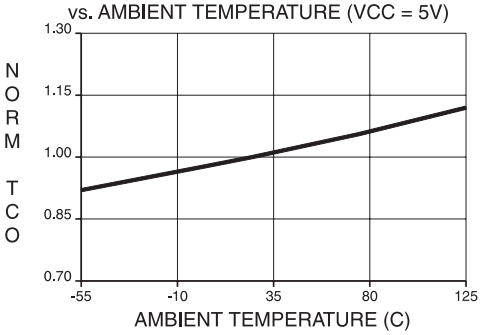
NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC = 5V)



NORMALIZED TCO
vs. SUPPLY VOLTAGE(TA=25°C)



NORMALIZED TCO
vs. AMBIENT TEMPERATURE (VCC = 5V)



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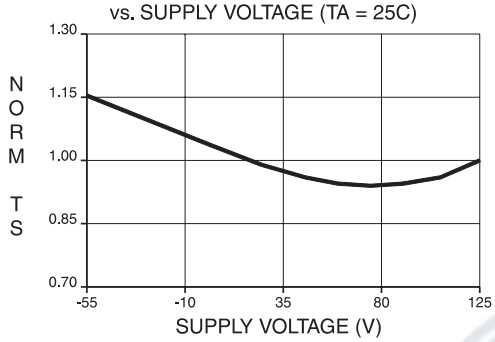
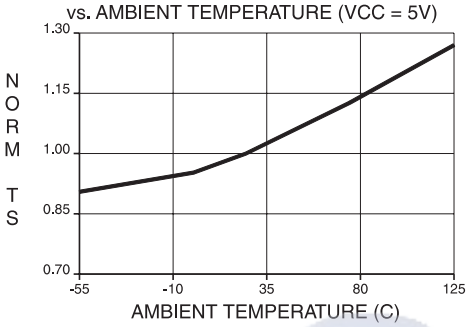
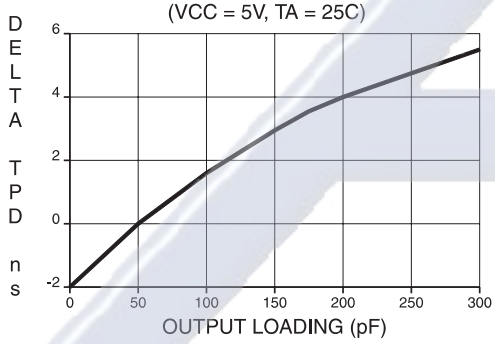
NORMALIZED TS
vs. SUPPLY VOLTAGE (TA = 25C)



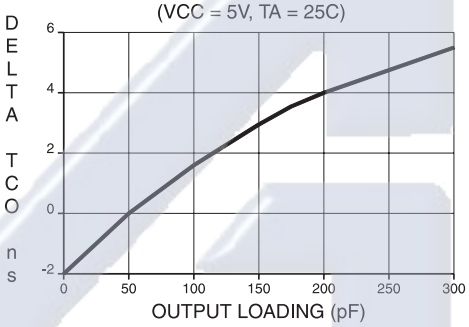
NORMALIZED TS
vs. AMBIENT TEMPERATURE (VCC = 5V)



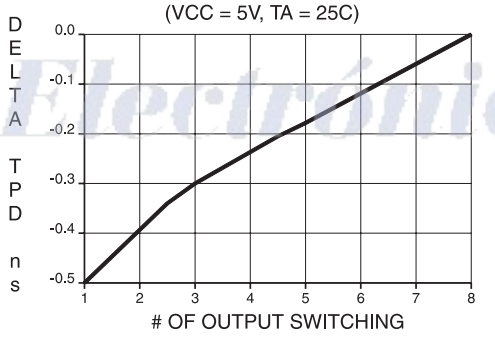
DELTA TPD vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



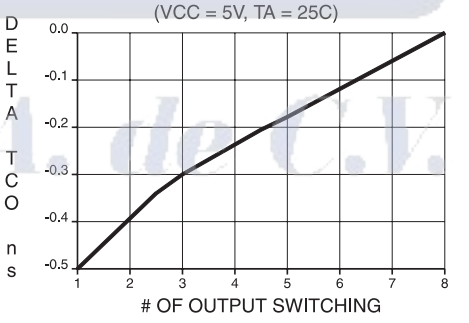
DELTA TCO vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



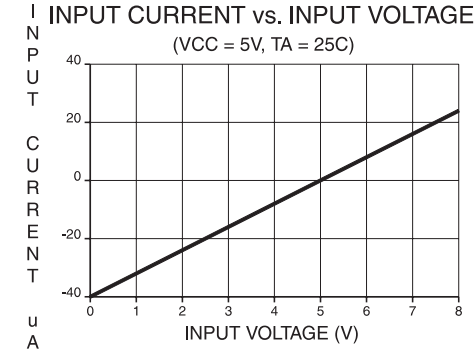
DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



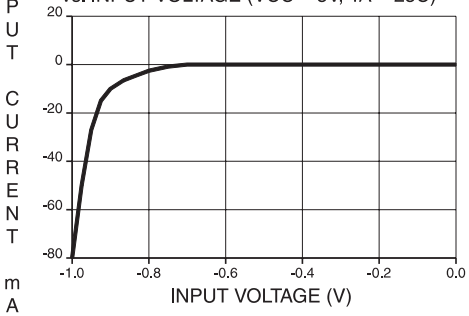
DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V, TA = 25C)



INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)



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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	5	5	ATF16V8B-7JC[1] ATF16V8B-7PC[1] ATF16V8B-7SC[1] ATF16V8B-7XC[1]	20J 20P3 20S 20X	Commercial (0°C to 70°C)
10	7.5	7	ATF16V8B-10JC ATF16V8B-10PC ATF16V8B-10SC ATF16V8B-10XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
			ATF16V8B-10JI ATF16V8B-10PI ATF16V8B-10SI ATF16V8B-10XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)
15	12	10	ATF16V8B-15JC ATF16V8B-15PC ATF16V8B-15SC ATF16V8B-15XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
			ATF16V8B-15JI ATF16V8B-15PI ATF16V8B-15SI ATF16V8B-15XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)
25	15	12	ATF16V8B-25JC ATF16V8B-25PC ATF16V8B-25SC ATF16V8B-25XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
			ATF16V8B-25JI ATF16V8B-25PI ATF16V8B-25SI ATF16V8B-25XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Note: 1. Recommend ATF16V8C-7.

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7.5	7	ATF16V8BQ-10JC ATF16V8BQ-10PC ATF16V8BQ-10SC ATF16V8BQ-10XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
15	12	10	ATF16V8BQL-15JC ATF16V8BQL-15PC ATF16V8BQL-15SC ATF16V8BQL-15XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
25	15	12	ATF16V8BQL-25JC ATF16V8BQL-25PC ATF16V8BQL-25SC ATF16V8BQL-25XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
			ATF16V8BQL-25JI ATF16V8BQL-25PI ATF16V8BQL-25SI ATF16V8BQL-25XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Package Type	
20J	20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
20P3	20-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
20X	20-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

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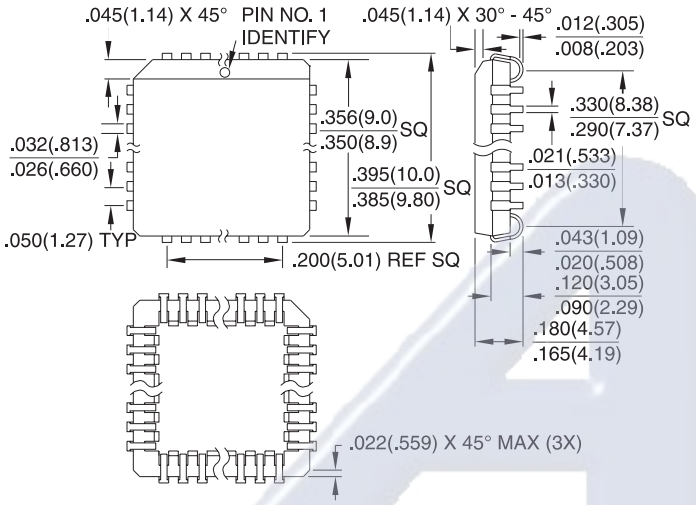
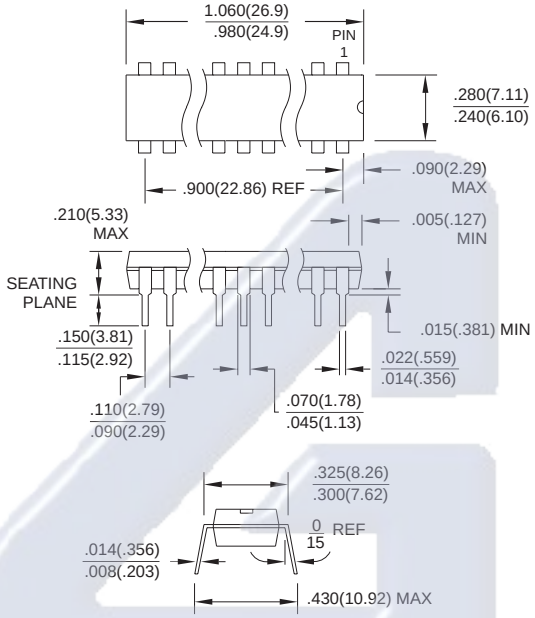
Packaging Information

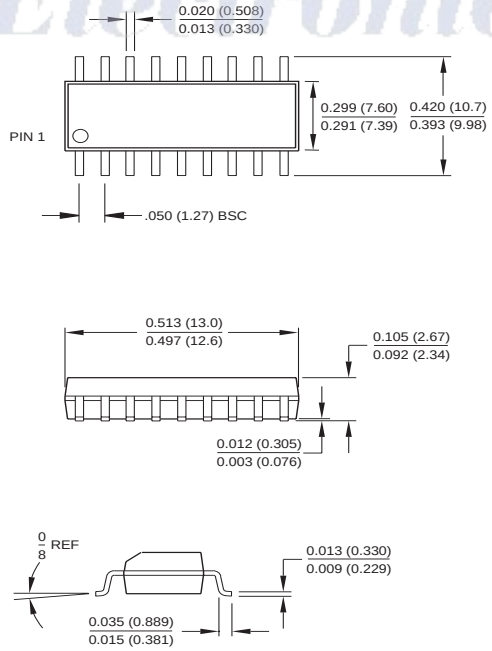
20J, 20-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



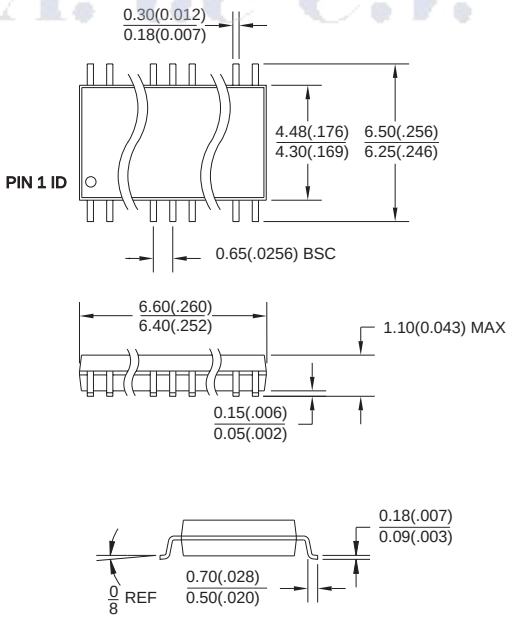
20P3, 20-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AD



20S, 20-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



20X, 20-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)
Dimensions in Millimeters and (Inches)



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