STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９８８３ＡＦ，ＢＤ９８８３ＦＶ**

FUNCTION
- 36V High voltage process
- 1ch control with Half-bridge
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Mode-selectable the operating or stand-by mode by stand-by pin

○Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	30	V
BST	BST	40	V
BST-ST Voltage Difference	BST-SW	15	V
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Power Dissipation	Pd	550*1 (BD9883AF)	mW
		650*2 (BD9883FV)	
Maximum Junction Temperature	Tjmax	+150	℃

*1 Pd derated at 4.4mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

*2 Pd derated at 5.2mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Recommended operating condition

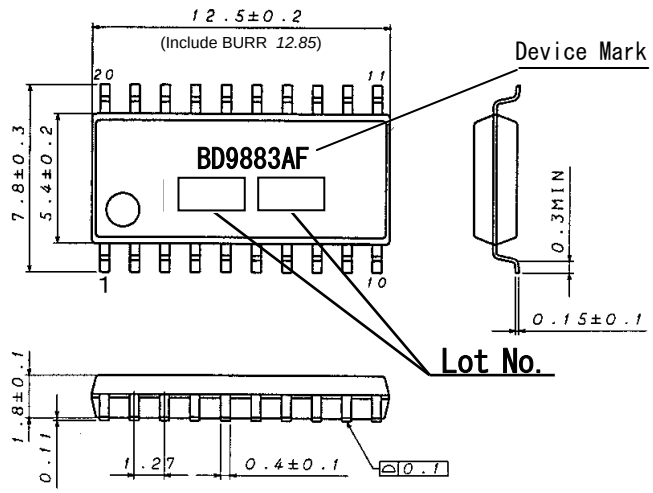
Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	6.0～22.0	V
CT oscillation frequency	f_{CT}	20～150	kHz
BST voltage	BST	4.0～34.0	V
BST-SW voltage difference	BST-SW	4.0～12.0	V
BCT oscillation frequency	f_{BCT}	0.10～0.50	kHz

○Electric Characteristics (Ta=25℃, VCC=12V)

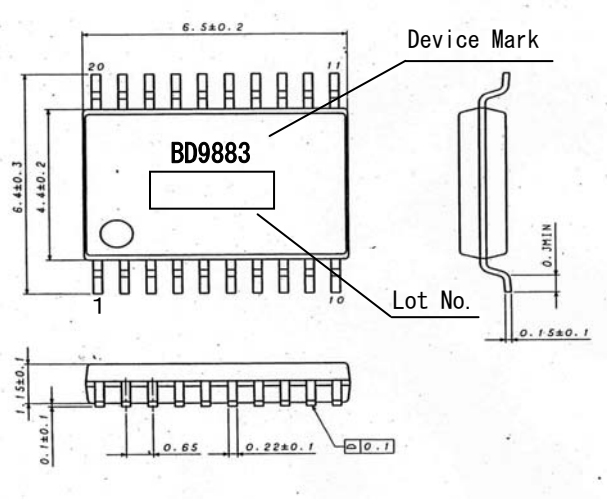
Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	Icc1	—	9.0	17.0	mA	fCT=100kHz
Stand-by current	Icc2	—	5.0	10.0	μA	
((STAND BY CONTROL))						
Stand-by voltage H	VstH	1.7	—	VCC	V	System ＯＮ
Stand-by voltage L	VstL	-0.3	—	0.7	V	System ＯＦＦ
Stand-by hysteresis	⊿Vst	0.05	0.20	0.35	V	
((UVLO BLOCK))						
Operating voltage	VuvloH	5.15	5.40	5.65	V	
Shut down voltage	VuvloL	4.90	5.15	5.40	V	
((REG BLOCK))						
REG output voltage	VREG	5.30	5.50	5.70	V	Vcc＞6.0V
REG source current	IREG	20.0	—	—	mA	
((OSC BLOCK))						
Active edge current	Iact	1.35/RT	1.5/RT	1.65/RT	A	
Negative edge current	Ineg	Iact×10	Iact×13	Iact×16	A	
OSC Max voltage	VoscH	1.8	2.0	2.2	V	fCT=50kHz, fCT=120kHz
OSC Min voltage①	VoscL1	0.2	0.4	0.6	V	fCT=50kHz
OSC Min voltage②	VoscL2	0.05	0.15	0.25	V	fCT=120kHz
Soft start current	Iss	0.50	1.00	1.50	μA	
SRT ON resistance	RSRT	—	150	300	Ω	
((BOSC BLOCK))						
BOSC Max voltage	VBCTH	1.920	2.000	2.080	V	fBCT=0.3kHz
BOSC Min Voltage	VBCTL	0.400	0.500	0.600	V	fBCT=0.3kHz
BOSC constant current	IBCT	1.35/BRT	1.5/BRT	1.65/BRT	A	VBCT=0.2V
((TIMER LATCH))						
Timer Latch voltage	Vscp	1.8	2.0	2.2	V	
Timer Latch current	Iscp	0.25	0.50	0.75	μA	
((FEED BACK BLOCK))						
IS threshold voltage	Vis	1.220	1.250	1.280	V	
VS threshold voltage	Vvs	1.220	1.250	1.280	V	
IS source current 1	Iis1	—	—	0.9	μA	DUTY=2.0V
IS source current 2	Iis2	12.0	20.0	28.0	μA	DUTY=0V、IS=0.5V
VS source current	Ivs	—	—	0.9	μA	
FB over voltage detect voltage	Vovf	2.2	2.5	2.8	V	
IS COMP detect Voltage	Visc	0.3	0.4	0.5	V	
((OUTPUT BLOCK))						
LN output sink current	RsinkLN	—	15	30	Ω	
LN output source current	RsourceLN	—	30	60	Ω	
HN output sink current	RsinkHN	—	15	30	Ω	VBST-VSW=5.0V
HN output source current	RsourceHN	—	30	60	Ω	VBST-VSW=5.0V

(This product is not designed for normal operation with in a radio active environment.)

○Package Dimensions

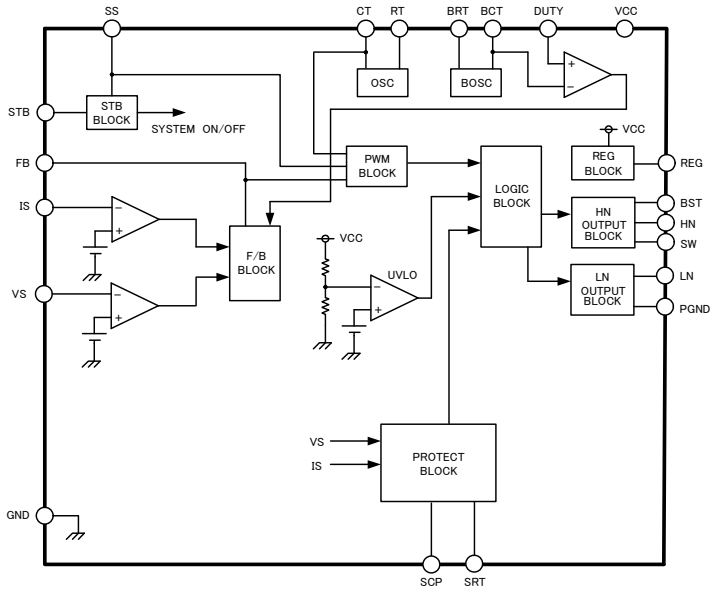


SOP20 (Unit:mm)



SSOP-B20 (Unit:mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Function
1	DUTY	Control PWM mode and BURST mode
2	BCT	External capacitor from BCT to GND for adjusting the BURST triangle oscillator
3	BRT	External resistor from BRT to GND for adjusting the BURST triangle oscillator
4	CT	External capacitor from CT to GND for adjusting the triangle oscillator
5	RT	External resistor from RT to GND for adjusting the triangle oscillator
6	SRT	External resistor from SRT to RT for adjusting the triangle oscillator
7	GND	GROUND
8	FB	Error amplifier output
9	IS	Error amplifier input①
10	VS	Error amplifier input②
11	STB	Stand-by switch
12	SCP	External capacitor from SCP to GND for Timer Latch
13	SS	External capacitor from SS to GND for Soft Start Control
14	PGND	Ground for FET drivers
15	LN	NMOS FET driver
16	HN	NMOS FET driver
17	SW	Low voltage for HN output
18	BST	Boot-Strap input for HN output
19	REG	Internal regulator output
20	VCC	Supply voltage input

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC.Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range

   The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.
3. Mounting Failures

   Mounting failures, such as misdirection or miscounts, may harm the device.
4. Electromagnetic Fields

   A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin
6. BD9883AF, BD9883FV has the short circuit protection with Thermal Shut Down System. When STB or Vcc pin re-supplied, They enables to cancel the latch. If It rise the temperature of the chip more than 170℃(TYP), It make the external FET OFF
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9883AF,BD9883FV is changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.7～1.7V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1)has P^+ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate)voltage to an input pin.

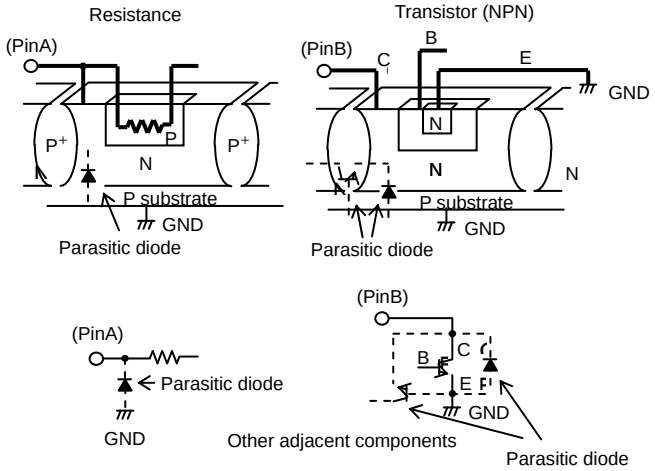


図-1 Simplified structure of a Bipolar IC

Notes

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