BUV22

SWITCHMODE™ Series NPN Silicon Power Transistor

This device is designed for high speed, high current, high power applications.

Features

- High DC Current Gain:
  h_{FE} min = 20 at I_C = 10 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$
  max = 1.0 V at I_C = 10 A
- Very Fast Switching Times:
  TF max = 0.35 μs at I_C = 20 A
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(SUS)}$	250	Vdc
Collector−Base Voltage	V_{CBO}	300	Vdc
Emitter−Base Voltage	V_{EBO}	7	Vdc
Collector−Emitter Voltage (V_{BE} = −1.5 V)	V_{CEX}	300	Vdc
Collector−Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	290	Vdc
Collector−Current − Continuous − Peak (PW ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base−Current Continuous	I_B	8	Adc
Total Device Dissipation @ T_C = 25°C	P_D	250	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	θ_{JC}	0.7	°C/W

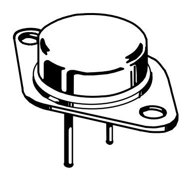
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

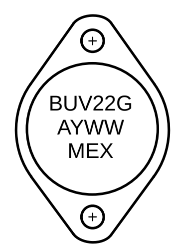
http://onsemi.com

40 AMPERES
NPN SILICON POWER
METAL TRANSISTOR
250 VOLTS − 250 WATTS



TO−204AE (TO−3)
CASE 197A

MARKING DIAGRAM



BUV22	= Device Code
G	= Pb−Free Package
A	= Assembly Location
Y	= Year
WW	= Work Week
MEX	= Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
BUV22	TO−204	100 Units / Tray
BUV22G	TO−204 (Pb−Free)	100 Units / Tray

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (Note 1)				
Collector−Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 300 V, V_{BE} = −1.5 V) (V_{CE} = 300 V, V_{BE} = −1.5 V, T_C = 125°C)	I_{CEX}		 3.0 12.0	mAdc
Collector−Emitter Cutoff Current (V_{CE} = 200 V)	I_{CEO}		3.0	mAdc
Emitter−Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter−Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	 12 0.15		Adc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 10 A, V_{CE} = 4 V) (I_C = 20 A, V_{CE} = 4 V)	h_{FE}	 20 10	 60	
Collector−Emitter Saturation Voltage (I_C = 10 A, I_B = 1 A) (I_C = 20 A, I_B = 2.5 A)	$V_{CE(sat)}$		 1.0 1.5	Vdc
Base−Emitter Saturation Voltage (I_C = 40 A, I_B = 4 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz

SWITCHING CHARACTERISTICS (Resistive Load)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn−on Time	(I_C = 20 A, I_{B1} = I_{B2} = 2.5 A, V_{CC} = 100 V, R_C = 5 Ω)	t_{on}		0.8	μs
Storage Time		t_s		2.0	
Fall Time		t_f		0.35	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

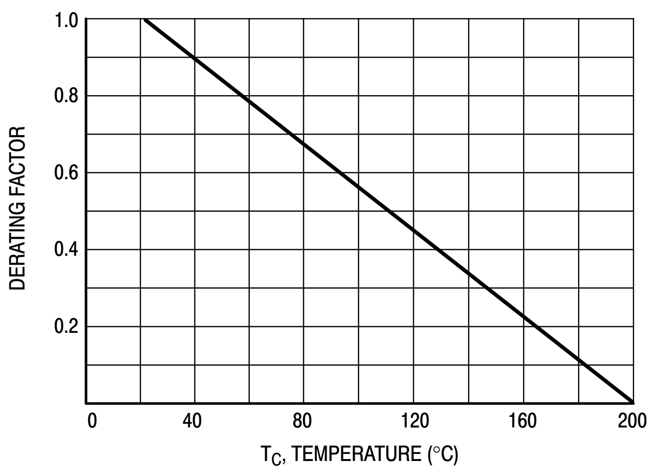


Figure 1. Power Derating

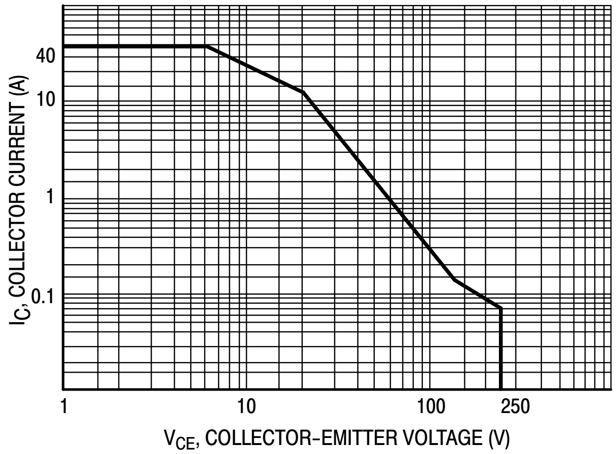


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

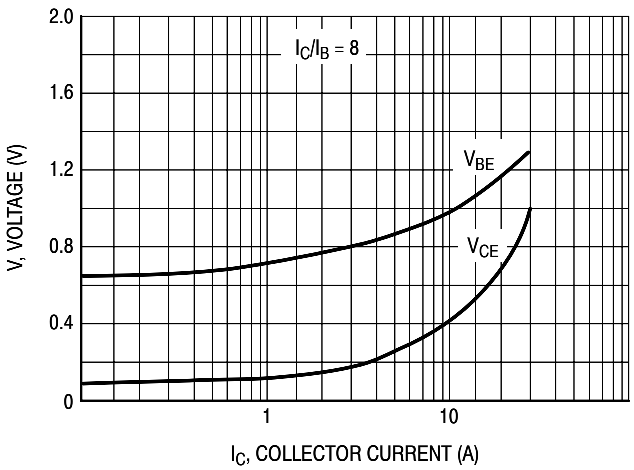


Figure 3. "On" Voltages

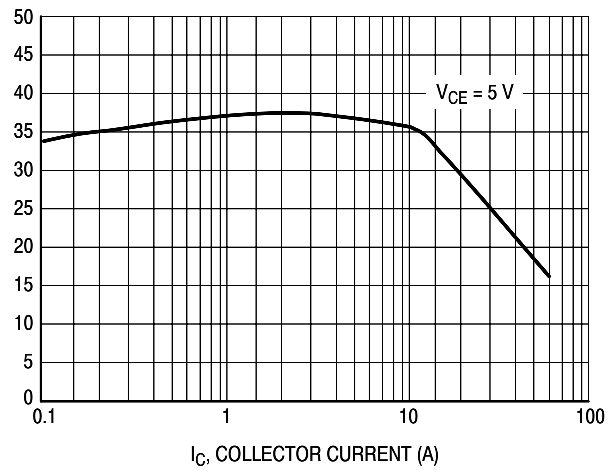


Figure 4. DC Current Gain

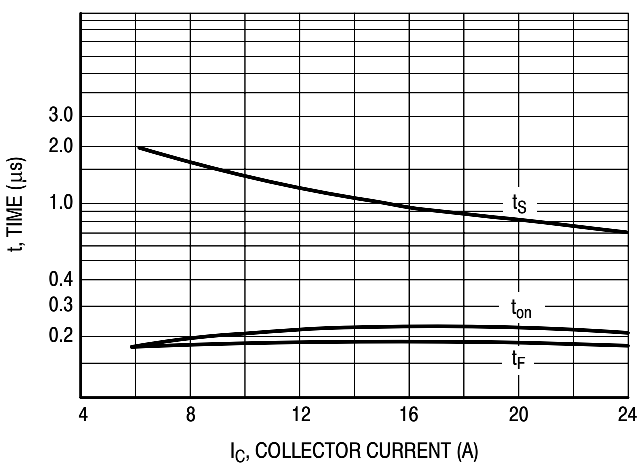


Figure 5. Resistive Switching Performance

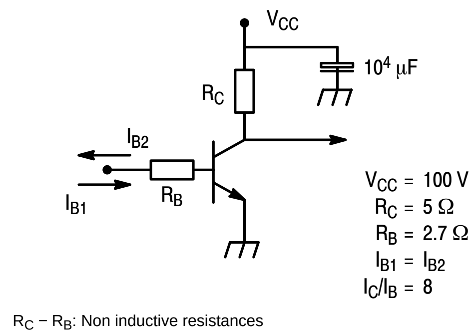
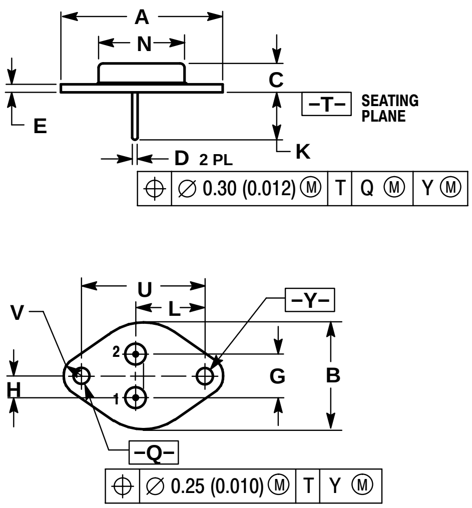


Figure 6. Switching Times Test Circuit

PACKAGE DIMENSIONS

TO−204 (TO−3)
CASE 197A−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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