Surface Mount Multilayer Ceramic Chip Capacitors (SMD MLCCs)

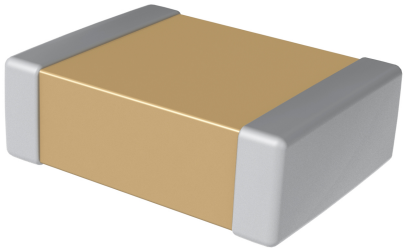
X7R Dielectric, 6.3 – 250 VDC (Commercial Grade)

Overview

KEMET's X7R dielectric features a 125°C maximum operating temperature and is considered temperature stable. The Electronics Components, Assemblies and Materials Association (EIA) characterizes X7R dielectric as a Class II material. Components of this classification are fixed, ceramic dielectric capacitors suited for bypass and decoupling applications or for frequency discriminating circuits where Q and stability of capacitance characteristics are not critical. X7R exhibits a predictable change in capacitance with respect to time and voltage, boasting a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to ±15% from −55°C to +125°C.

Benefits

- −55°C to +125°C operating temperature range
- Lead (Pb)-free, RoHS, and REACH Compliant
- Temperature stable dielectric
- EIA 0402, 0603, 0805, 1206, 1210, 1808, 1812, 1825, 2220, and 2225 case sizes
- DC voltage ratings of 6.3 V, 10 V, 16 V, 25 V, 35 V, 50 V, 100 V, 200 V, and 250 V
- Capacitance offerings ranging from 10 pF to 47 µF
- Available capacitance tolerances of ±5%, ±10% and ±20%
- Non-polar device, minimizing installation concerns
- 100% pure matte tin-plated termination finish allowing for excellent solderability
- SnPb termination finish option available upon request (5% Pb minimum)



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Applications

Typical applications include decoupling, bypass, filtering and transient voltage suppression.

Ordering Information

C	1206	C	106	M	4	R	A	C	TU
Ceramic	Case Size (L" x W")	Specification/ Series[1]	Capacitance Code (pF)	Capacitance Tolerance	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Termination Finish[2]	Packaging/ Grade (C-Spec)
	0402 0603 0805 1206 1210 1808 1812 1825 2220 2225	C = Standard	Two significant digits and number of zeros.	J = ±5% K = ±10% M = ±20%	9 = 6.3 8 = 10 4 = 16 3 = 25 6 = 35 5 = 50 1 = 100 2 = 200 A = 250	R = X7R	A = N/A	C = 100% Matte Sn	See "Packaging C-Spec Ordering Options Table"

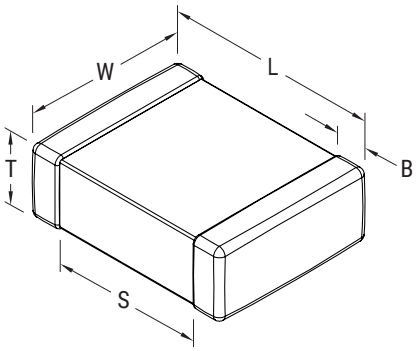
[1] Flexible termination option is available. Please see FT-CAP product bulletin C1013_X7R_FT-CAP_SMD.
[2] Additional termination finish options may be available. Contact KEMET for details.

Packaging C-Spec Ordering Options Table

Packaging Type[1]	Packaging/Grade Ordering Code (C-Spec)
Bulk Bag/Unmarked	Not required (Blank)
7" Reel/Unmarked	TU
13" Reel/Unmarked	7411 (EIA 0603 and smaller case sizes) 7210 (EIA 0805 and larger case sizes)
7" Reel/Marked	TM
13" Reel/Marked	7040 (EIA 0603 and smaller case sizes) 7215 (EIA 0805 and larger case sizes)
7" Reel/Unmarked/2 mm pitch[2]	7081
13" Reel/Unmarked/2 mm pitch[2]	7082

[1] Default packaging is "Bulk Bag." An ordering code C-Spec is not required for "Bulk Bag" packaging.
[1] The terms "Marked" and "Unmarked" pertain to laser marking option of capacitors. All packaging options labeled as "Unmarked" will contain capacitors that have not been laser marked. Please contact KEMET if you require a laser marked option. For more information see "Capacitor Marking."
[2] The 2 mm pitch option allows for double the packaging quantity of capacitors on a given reel size. This option is limited to EIA 0603 (1608 metric) case size devices. For more information regarding 2 mm pitch option see "Tape & Reel Packaging Information."

Dimensions – Millimeters (Inches)



EIA Size Code	Metric Size Code	L Length	W Width	T Thickness	B Bandwidth	S Separation Minimum	Mounting Technique
0402	1005	1.00 (0.040) ±0.05 (0.002)	0.50 (0.020) ±0.05 (0.002)	See Table 2 for Thickness	0.30 (0.012) ±0.10 (0.004)	0.30 (0.012)	Solder reflow only
0603	1608	1.60 (0.063) ±0.15 (0.006)	0.80 (0.032) ±0.15 (0.006)		0.35 (0.014) ±0.15 (0.006)	0.70 (0.028)	Solder wave or Solder reflow
0805	2012	2.00 (0.079) ±0.20 (0.008)	1.25 (0.049) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	0.75 (0.030)	
1206	3216	3.20 (0.126) ±0.20 (0.008)	1.60 (0.063) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	N/A	
1210[1]	3225	3.20 (0.126) ±0.20 (0.008)	2.50 (0.098) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)		Solder reflow only
1808	4520	4.70 (0.185) ±0.50 (0.020)	2.00 (0.079) ±0.20 (0.008)		0.60 (0.024) ±0.35 (0.014)		
1812	4532	4.50 (0.177) ±0.30 (0.012)	3.20 (0.126) ±0.30 (0.012)		0.60 (0.024) ±0.35 (0.014)		
1825	4564	4.50 (0.177) ±0.30 (0.012)	6.40 (0.252) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)		
2220	5650	5.70 (0.224) ±0.40 (0.016)	5.00 (0.197) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)		
2225	5664	5.60 (0.220) ±0.40 (0.016)	6.40 (0.248) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)		

[1] *For capacitance values ≥ 4.7 µF add 0.02 (0.001) to the width tolerance dimension and 0.10 (0.004) to the length tolerance dimension.*

Qualification/Certification

Commercial Grade products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 4, Performance & Reliability.

Environmental Compliance

Lead (Pb)-free, RoHS, and REACH compliant without exemptions.

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	−55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±15%
[1]Aging Rate (Maximum % Capacitance Loss/Decade Hour)	3.0%
[2]Dielectric Withstanding Voltage (DWV)	250% of rated voltage (5 ±1 seconds and charge/discharge not exceeding 50mA)
[3]Dissipation Factor (DF) Maximum Limit at 25°C	See Dissipation Factor Limit Table
[4]Insulation Resistance (IR) Minimum Limit at 25°C	See Insulation Resistance Limit Table (Rated voltage applied for 120 ±5 seconds at 25°C)

[1] Regarding Aging Rate: Capacitance measurements (including tolerance) are indexed to a referee time of 48 or 1,000 hours. Please refer to a part number specific datasheet for referee time details.

[2] DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the capacitor.

[3] Capacitance and dissipation factor (DF) measured under the following conditions:

1 kHz ±50 Hz and 1.0 ±0.2 V_{rms} if capacitance ≤ 10 µF

120 Hz ±10 Hz and 0.5 ±0.1 V_{rms} if capacitance > 10 µF

[4] To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Insulation Resistance Limit Table

EIA Case Size	Rated DC Voltage	1,000 megohm microfarads or 100 GΩ	500 megohm microfarads or 10 GΩ	100 megohm microfarads or 10 GΩ
0402	ALL	< 0.012 µF	≥ 0.012 µF	N/A
0603	≤ 200 V	< 0.047 µF	≥ 0.047 µf < 0.47 µf	≥ 0.47 µf
	250 V	N/A	N/A	ALL
0805	≤ 200 V	< 0.15 µF	≥ 0.15 µF < 2.2 µf	≥ 2.2 µf
	250 V	< .027 µF	N/A	≥ .027 µF
1206	≤ 200 V	< 0.47 µF	≥ 0.47 µF < 4.7 µf	≥ 4.7 µf
	250 V	< 0.12 µF	N/A	≥ 0.12 µF
1210	≤ 200 V	< 0.39 µF	≥ 0.39 µF < 10 µf	≥ 10 µf
	250 V	< 0.27 µF	N/A	≥ 0.27 µF
1808	ALL	ALL	N/A	N/A
1812	ALL	< 2.2 µF	≥ 2.2 µF	N/A
1825	ALL	ALL	N/A	N/A
2220	ALL	< 10 µF	≥ 10 µF	N/A
2225	ALL	ALL	N/A	N/A

Post Environmental Limits

High Temperature Life, Biased Humidity, Moisture Resistance						
Dielectric	Case Size	Rated DC Voltage	Capacitance Value	Dissipation Factor (Maximum %)	Capacitance Shift	Insulation Resistance
X7R	0402	< 16	All	7.5	± 20%	10% of Initial limit
		16/25		5.0		
		> 25		3.0		
	0603	< 16	< 1.0 µF	7.5		
		16/25		5.0		
		> 25		3.0		
		< 16	≥ 1.0 µF	20.0		
		16/25				
	0805	< 16	< 2.2 µF	7.5		
		16/25		5.0		
		> 25	< 1.0 µF	3.0		
		< 16	≥ 2.2 µF	20.0		
		16/25				
		> 25	≥ 1.0 µF			
	1206	< 16	< 10 µF	7.5		
		16/25		5.0		
		> 25		3.0		
		35/50	≥ 2.2 µF	20.0		
		< 16	≥ 10 µF			
		16/25				
	1210	< 16	< 22 µF	7.5		
		16/25		5.0		
		> 25		3.0		
		< 16	≥ 22 µF	20.0		
		16/25				
	1808-2225	< 16	All	7.5		
		16/25		5.0		
		> 25		3.5		

Dissipation Factor (DF) Limit Table

EIA Case Size	Rated DC Voltage	Capacitance	Dissipation Factor (Maximum %)
0402	< 16	All	5.0
	16		3.5
	25	< 0.1 µF	3.5
	25	≥ 0.1 µF	10.0
	> 25	All	2.5
0603	< 16	< 1.0 µF	5.0
	16/25		3.5
	> 25		2.5
	< 16	≥ 1.0 µF	10.0
	16/25		
0805	< 16	< 2.2 µF	5.0
	16/25		3.5
	> 25	< 1.0 µF	2.5
	< 16	≥ 2.2 µF	10.0
	16/25		
	> 25	≥ 1.0 µF	
1206	< 16	< 10 µF	5.0
	16/25		3.5
	> 25		2.5
	35/50	≥ 2.2 µF	10.0
	< 16	≥ 10 µF	10.0
	16/25		
1210	< 16	< 22 µF	5.0
	16/25		3.5
	> 25		2.5
	< 16	≥ 22 µF	10.0
	16/25		
1808–2225	< 16	All	5.0
	16/25		3.5
	> 25		2.5

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC–7351

EIA Size Code	Metric Size Code	Density Level A: Maximum (Most) Land Protrusion (mm)					Density Level B: Median (Nominal) Land Protrusion (mm)					Density Level C: Minimum (Least) Land Protrusion (mm)				
		C	Y	X	V1	V2	C	Y	X	V1	V2	C	Y	X	V1	V2
0402	1005	0.50	0.72	0.72	2.20	1.20	0.45	0.62	0.62	1.90	1.00	0.40	0.52	0.52	1.60	0.80
0603	1608	0.90	1.15	1.10	4.00	2.10	0.80	0.95	1.00	3.10	1.50	0.60	0.75	0.90	2.40	1.20
0805	2012	1.00	1.35	1.55	4.40	2.60	0.90	1.15	1.45	3.50	2.00	0.75	0.95	1.35	2.80	1.70
1206	3216	1.60	1.35	1.90	5.60	2.90	1.50	1.15	1.80	4.70	2.30	1.40	0.95	1.70	4.00	2.00
1210	3225	1.60	1.35	2.80	5.65	3.80	1.50	1.15	2.70	4.70	3.20	1.40	0.95	2.60	4.00	2.90
1210[1]	3225	1.50	1.60	2.90	5.60	3.90	1.40	1.40	2.80	4.70	3.30	1.30	1.20	2.70	4.00	3.00
1808	4520	2.30	1.75	2.30	7.40	3.30	2.20	1.55	2.20	6.50	2.70	2.10	1.35	2.10	5.80	2.40
1812	4532	2.15	1.60	3.60	6.90	4.60	2.05	1.40	3.50	6.00	4.00	1.95	1.20	3.40	5.30	3.70
1825	4564	2.15	1.60	6.90	6.90	7.90	2.05	1.40	6.80	6.00	7.30	1.95	1.20	6.70	5.30	7.00
2220	5650	2.75	1.70	5.50	8.20	6.50	2.65	1.50	5.40	7.30	5.90	2.55	1.30	5.30	6.60	5.60
2225	5664	2.70	1.70	6.90	8.10	7.90	2.60	1.50	6.80	7.20	7.30	2.50	1.30	6.70	6.50	7.00

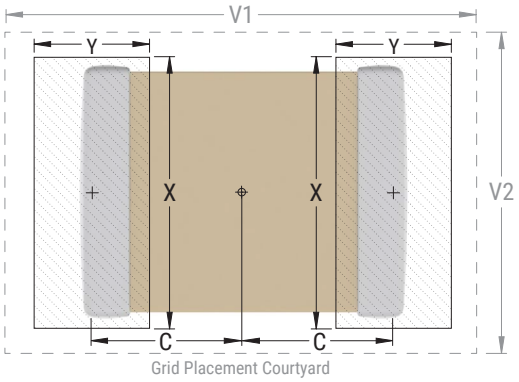
[1] *Only for capacitance values ≥ 22 µF*

Density Level A: *For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes. KEMET only recommends wave soldering of EIA 0603, 0805, and 1206 case sizes.*

Density Level B: *For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.*

Density Level C: *For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC Standard 7351 (IPC–7351).*

Image below based on Density Level B for an EIA 1210 case size.



Soldering Process

Recommended Soldering Technique:

- Solder wave or solder reflow for EIA case sizes 0603, 0805 and 1206
- All other EIA case sizes are limited to solder reflow only

Recommended Reflow Soldering Profile:

KEMET's families of surface mount multilayer ceramic capacitors (SMD MLCCs) are compatible with wave (single or dual), convection, IR or vapor phase reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for convection and IR reflow reflect the profile conditions of the IPC/J-STD-020 standard for moisture sensitivity testing. These devices can safely withstand a maximum of three reflow passes at these conditions.

Profile Feature	Termination Finish	
	SnPb	100% Matte Sn
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_S) from T_{Smin} to T_{Smax}	60 – 120 seconds	60 – 120 seconds
Ramp-Up Rate (T_L to T_P)	3°C/second maximum	3°C/second maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_P)	235°C	260°C
Time Within 5°C of Maximum Peak Temperature (t_P)	20 seconds maximum	30 seconds maximum
Ramp-Down Rate (T_P to T_L)	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Note 1: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

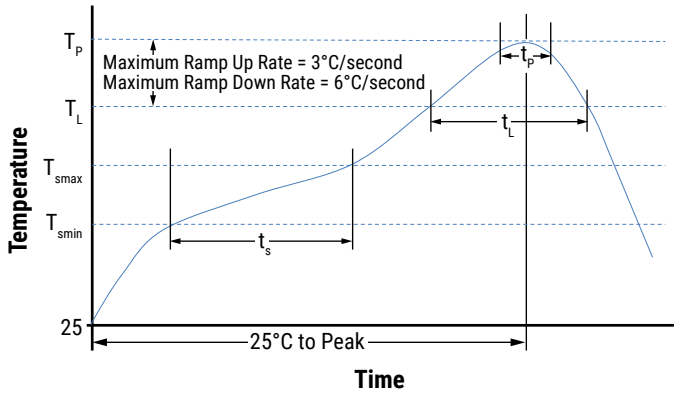


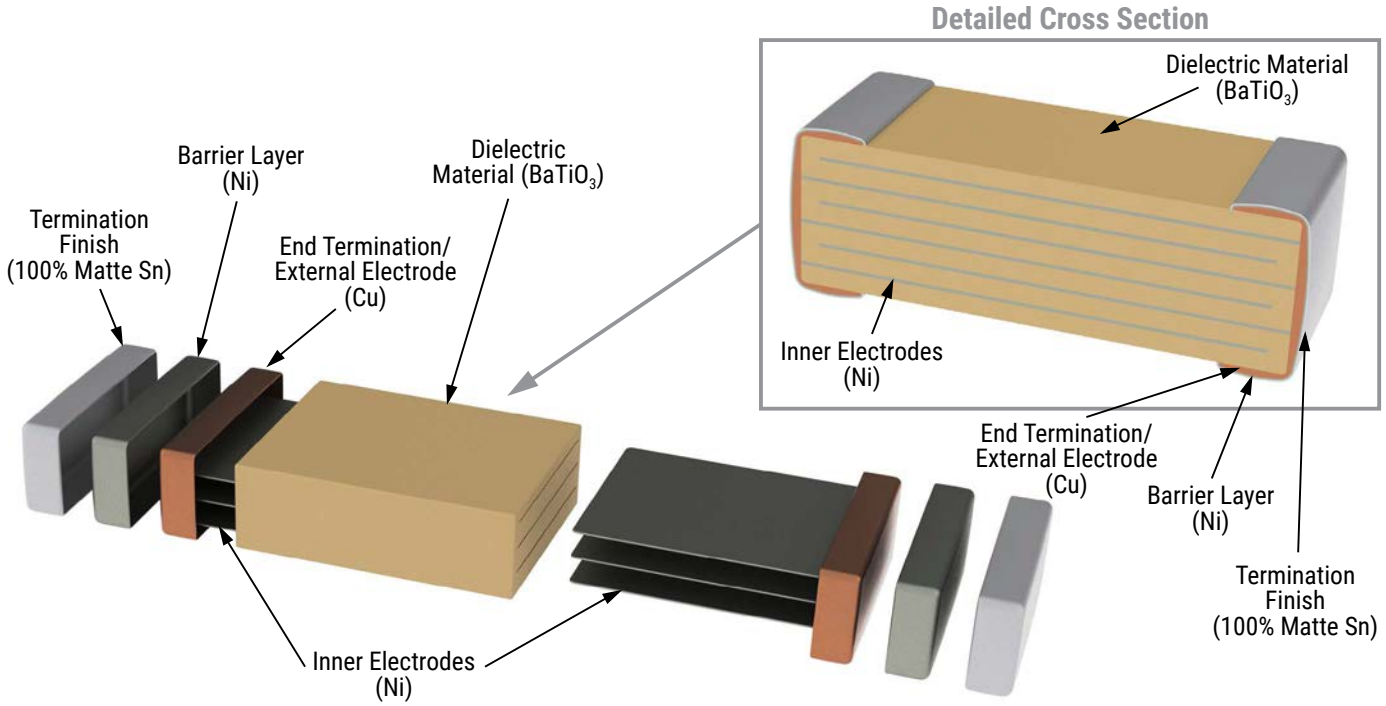
Table 4 – Performance & Reliability: Test Methods and Conditions

<table>
<tr><th>Stress</th><th>Reference</th><th>Test or Inspection Method</th></tr>
<tr><td>Terminal Strength</td><td>JIS–C–6429</td><td>Appendix 1, Note: Force of 1.8 kg for 60 seconds.</td></tr>
<tr><td>Board Flex</td><td>JIS–C–6429</td><td>Appendix 2, Note: Standard termination system – 2.0 mm (minimum) for all except 3 mm for C0G. Flexible termination system – 3.0 mm (minimum).</td></tr>
<tr><td rowspan="4">Solderability</td><td rowspan="4">J–STD–002</td><td>Magnification 50 X. Conditions:</td></tr>
<tr><td>a) Method B, 4 hours at 155°C, dry heat at 235°C</td></tr>
<tr><td>b) Method B, category 3 at 215°C</td></tr>
<tr><td>c) Method D, category 3 at 260°C</td></tr>
<tr><td>Temperature Cycling</td><td>JESD22 Method JA–104</td><td>1,000 Cycles (–55°C to +125°C). Measurement at 24 hours ±4 hours after test conclusion.</td></tr>
<tr><td rowspan="2">Biased Humidity</td><td rowspan="2">MIL–STD–202
Method 103</td><td>Load Humidity: 1,000 hours 85°C/85% RH and rated voltage. Add 100 K ohm resistor. Measurement at 24 hours ±4 hours after test conclusion.</td></tr>
<tr><td>Low Volt Humidity: 1,000 hours 85°C/85% RH and 1.5 V. Add 100 K ohm resistor. Measurement at 24 hours ±4 hours after test conclusion.</td></tr>
<tr><td>Moisture Resistance</td><td>MIL–STD–202
Method 106</td><td>t = 24 hours/cycle. Steps 7a and 7b not required.
Measurement at 24 hours ±4 hours after test conclusion.</td></tr>
<tr><td>Thermal Shock</td><td>MIL–STD–202
Method 107</td><td>–55°C/+125°C. Note: Number of cycles required – 300. Maximum transfer time – 20 seconds. Dwell time – 15 minutes. Air – air.</td></tr>
<tr><td>High Temperature Life</td><td>MIL–STD–202
Method 108/EIA–198</td><td>1,000 hours at 125°C with 2 X rated voltage applied excluding the following:
<table>
<tr><th>Case Size</th><th>Capacitance</th><th>Applied Voltage</th></tr>
<tr><td>0603 & 0805</td><td>≥ 1.0 µF</td><td rowspan="2">1.5 X</td></tr>
<tr><td>1206 & 1210</td><td>≥ 10 µF</td></tr>
</table></td></tr>
<tr><td>Storage Life</td><td>MIL–STD–202
Method 108</td><td>150°C, 0 VDC for 1,000 hours.</td></tr>
<tr><td>Vibration</td><td>MIL–STD–202
Method 204</td><td>5 g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8" X 5" PCB 0.031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10 – 2,000 Hz</td></tr>
<tr><td>Mechanical Shock</td><td>MIL–STD–202
Method 213</td><td>Figure 1 of Method 213, Condition F.</td></tr>
<tr><td>Resistance to Solvents</td><td>MIL–STD–202
Method 215</td><td>Add aqueous wash chemical, OKEM Clean or equivalent.</td></tr>
</table>

Storage & Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature – reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction (Typical)



Capacitor Marking (Optional):

These surface mount multilayer ceramic capacitors are normally supplied unmarked. If required, they can be marked as an extra cost option. Marking is available on most KEMET devices, but must be requested using the correct ordering code identifier(s). If this option is requested, two sides of the ceramic body will be laser marked with a "K" to identify KEMET, followed by two characters (per EIA–198 - see table below) to identify the capacitance value. EIA 0603 case size devices are limited to the "K" character only.

Laser marking option is not available on:

- C0G, ultra stable X8R and Y5V dielectric devices.
- EIA 0402 case size devices.
- EIA 0603 case size devices with flexible termination option.
- KPS commercial and automotive grade stacked devices.
- X7R dielectric products in capacitance values outlined below.

EIA Case Size	Metric Size Code	Capacitance
0603	1608	≤ 170 pF
0805	2012	≤ 150 pF
1206	3216	≤ 910 pF
1210	3225	≤ 2,000 pF
1808	4520	≤ 3,900 pF
1812	4532	≤ 6,700 pF
1825	4564	≤ 0.018 µF
2220	5650	≤ 0.027 µF
2225	5664	≤ 0.033 µF

Marking appears in legible contrast. Illustrated below is an example of an MLCC with laser marking of "KA8", which designates a KEMET device with rated capacitance of 100 µF. Orientation of marking is vendor optional.