



Data sheet acquired from Harris Semiconductor
SCHS031B - Revised July 2003

CD4026B, CD4033B Types

CMOS Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)
With Decoded 7-Segment Display Outputs and:
Display Enable - CD4026B
Ripple Blanking - CD4033B

■ CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven

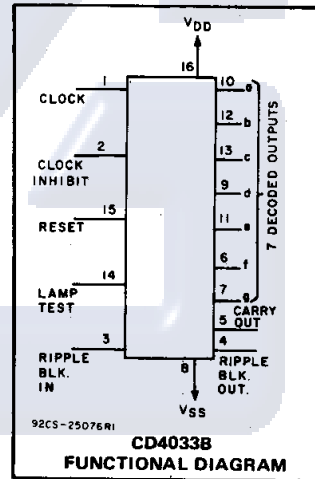
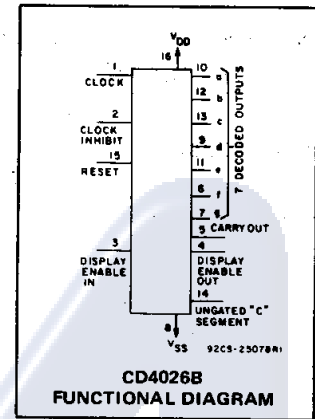
Features:

- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 6 MHz (typ.) at V_{DD}=10 V
- Ideal for low-power displays
- Display enable output (CD4026B)
- "Ripple blanking" and lamp test (CD4033B)
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Schmitt-triggered clock inputs
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

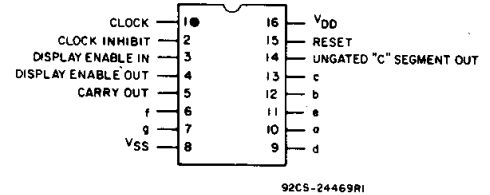
- Decade counting 7-segment decimal display
- Frequency division 7-segment decimal displays
- Clocks, watches, timers (e.g. ÷60, ÷60, ÷12 counter/display)
- Counter/display driver for meter applications

segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.



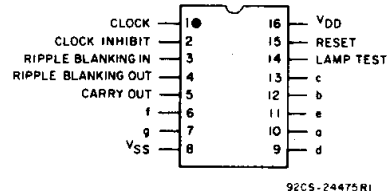
TERMINAL DIAGRAMS

Top View



CD4026B

Top View



CD4033B

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

CD4026B, CD4033B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | VDD (V) | LIMITS | | UNITS |
|---|------------|--------|-----------|-------|
| | | MIN. | MAX. | |
| Supply-Voltage Range (For T_A = Full Package Temperature Range) | | 3 | 18 | V |
| Clock Input Frequency, f_{CL} | 5 | — | 2.5 | MHz |
| | 10 | — | 5.5 | |
| | 15 | — | 8 | |
| Clock Pulse Width, t_{WCL} | 5 | 220 | — | ns |
| | 10 | 100 | — | |
| | 15 | 80 | — | |
| Clock Rise and Fall Time, t_{rCL}, t_{fCL} | 5 | — | Unlimited | ns |
| | 10 | — | — | |
| | 15 | — | — | |
| Clock Inhibit Set Up Time, t_{SU} | 5 | 200 | — | ns |
| | 10 | 50 | — | |
| | 15 | 30 | — | |
| Reset Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 50 | — | |
| Reset Removal Time | 5 | 30 | — | ns |
| | 10 | 15 | — | |
| | 15 | 10 | — | |

CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero \rightarrow 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|-----------------------|------------------------|------------------------|---------------------------------------|-----------|---------|---------|-------|---------------|-----------|---------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I_{DD} Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0.04 | 5 | μ A |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0.04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0.08 | 100 | |
| Output Low (Sink) Current I_{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High (Source) Current, I_{OH} Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| Output Voltage: Low-Level, V_{OL} Max. | — | 0,5 | 5 | 0.05 | | | | — | 0 | 0.05 | V |
| | — | 0,10 | 10 | 0.05 | | | | — | 0 | 0.05 | |
| | — | 0,15 | 15 | 0.05 | | | | — | 0 | 0.05 | |
| Output Voltage: High-Level, V_{OH} Min. | — | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | — | V |
| | — | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | — | |
| | — | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | — | |
| Input Low Voltage, V_{IL} Max. | 0.5, 4.5 | — | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1, 9 | — | 10 | 3 | | | | — | — | 3 | |
| | 1.5, 13.5 | — | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, V_{IH} Min. | 0.5, 4.5 | — | 5 | 3.5 | | | | 3.5 | — | — | V |
| | 1, 9 | — | 10 | 7 | | | | 7 | — | — | |
| | 1.5, 13.5 | — | 15 | 11 | | | | 11 | — | — | |
| Input Current I_{IN} Max. | — | 0,18 | 18 | ± 0.1 | ± 0.1 | ± 1 | ± 1 | — | $\pm 10^{-5}$ | ± 0.1 | μ A |

CD4026B, CD4033B Types

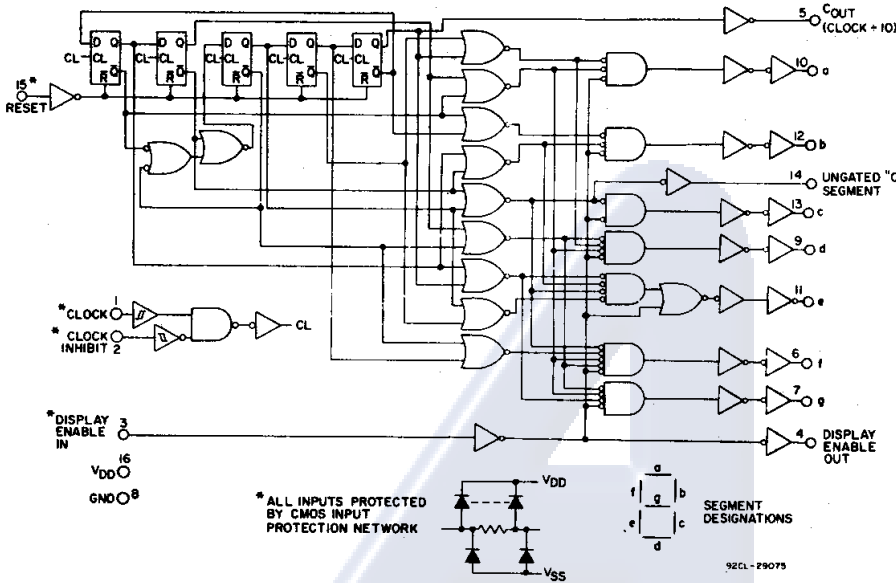


Fig. 1 - CD4026B logic diagram.

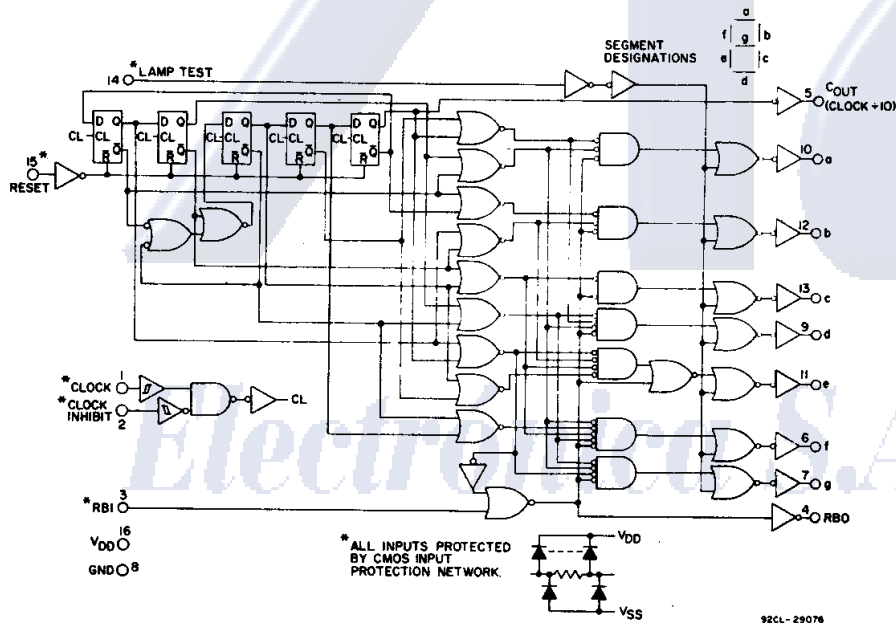


Fig. 2 - CD4033B logic diagram.

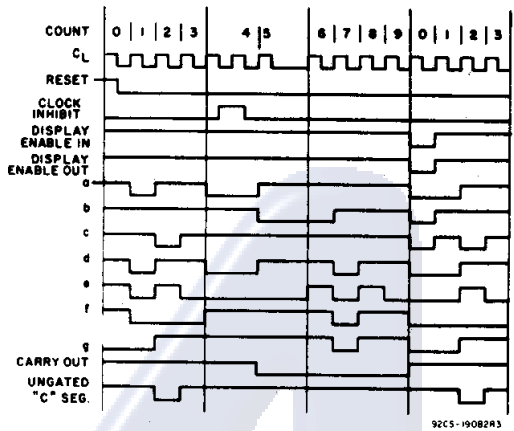


Fig. 3 - CD4026B timing diagram.

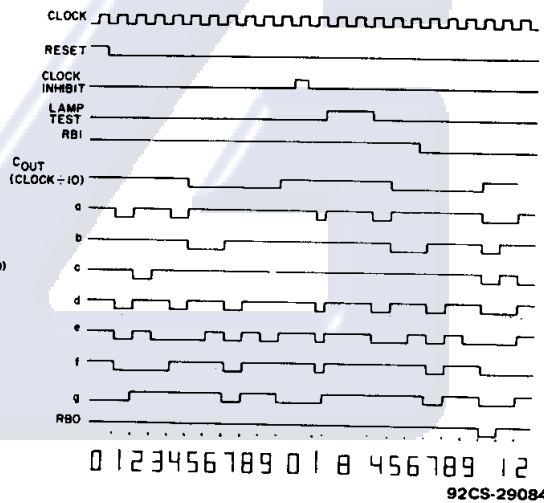


Fig. 4 - CD4033B timing diagram.

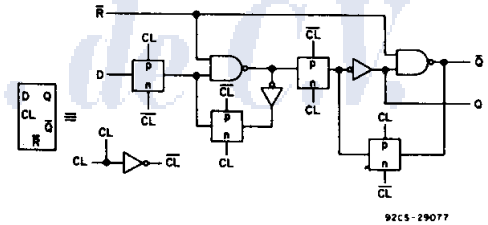


Fig. 5 - Detail of typical flip-flop stage for both types.

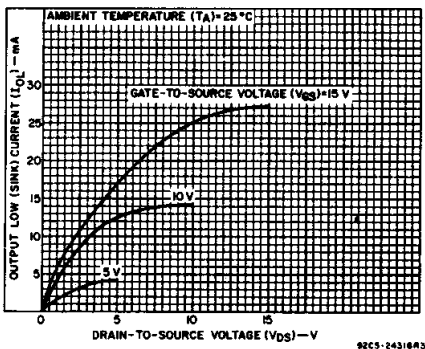


Fig. 6 - Typical n-channel output low (sink) current characteristics.

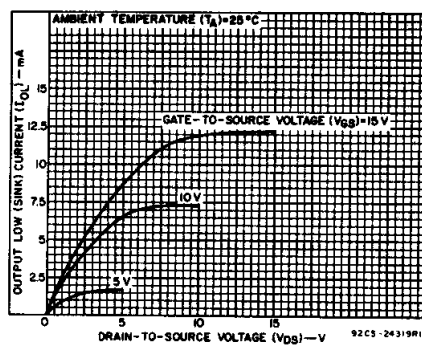


Fig. 7 - Minimum n-channel output low (sink) current characteristics.

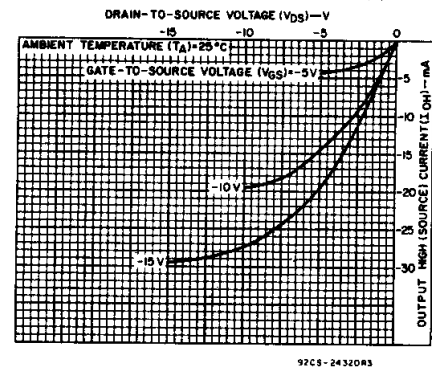


Fig. 8 - Typical p-channel output high (source) current characteristics.

CD4026B, CD4033B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|--|-----------------|---------|-----------|------|-------|------|
| | | VDD (V) | Min. | Typ. | | Max. |
| CLOCKED OPERATION | | | | | | |
| Propagation Delay Time; Carry-Out Line t_{PLH}, t_{PHL} | | 5 | - | 250 | 500 | ns |
| | | 10 | - | 100 | 200 | |
| | | 15 | - | 75 | 150 | |
| Decode Outlines | | 5 | - | 350 | 700 | ns |
| | | 10 | - | 125 | 250 | |
| | | 15 | - | 90 | 180 | |
| Transition Time; Carry-Out Line t_{THL}, t_{TLH} | | 5 | - | 100 | 200 | ns |
| | | 10 | - | 50 | 100 | |
| | | 15 | - | 25 | 50 | |
| Maximum Clock Input Frequency, f_{CL}^{Δ} | | 5 | 2.5 | 5 | - | MHz |
| | | 10 | 5.5 | 11 | - | |
| | | 15 | 8 | 16 | - | |
| Min. Clock Pulse Width, t_W | | 5 | - | 110 | 220 | ns |
| | | 10 | - | 50 | 100 | |
| | | 15 | - | 40 | 80 | |
| Clock and Clock Inhibit Rise or Fall Time; t_{rCL}, t_{fCL} | | 5 | Unlimited | | ns | |
| | | 10 | Unlimited | | | |
| | | 15 | Unlimited | | | |
| Average Input Capacitance, C_{IN} | Any Input | - | 5 | 7 | pF | |
| RESET OPERATION | | | | | | |
| Propagation Delay Time; To Carry-Out Line, t_{PLH} | | 5 | - | 275 | 550 | ns |
| | | 10 | - | 120 | 240 | |
| | | 15 | - | 80 | 160 | |
| To Decode Out Lines, t_{PHL}, t_{PLH} | | 5 | - | 300 | 600 | ns |
| | | 10 | - | 125 | 250 | |
| | | 15 | - | 90 | 180 | |
| Min. Reset Pulse Width, t_W | | 5 | - | 100 | 120 | ns |
| | | 10 | - | 50 | 100 | |
| | | 15 | - | 25 | 50 | |
| Min. Reset Removal Time | | 5 | - | 0 | 30 | ns |
| | | 10 | - | 0 | 15 | |
| | | 15 | - | 0 | 10 | |

Δ Measured with respect to carry-out line.

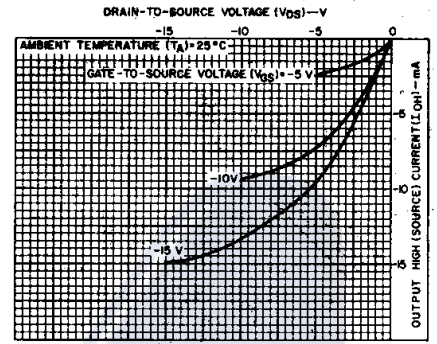


Fig. 9 - Minimum p-channel output high (source) current characteristics.

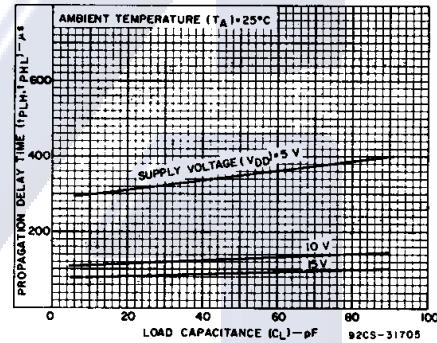


Fig. 10 - Typical propagation delay time as a function of load capacitance for decoded outputs.

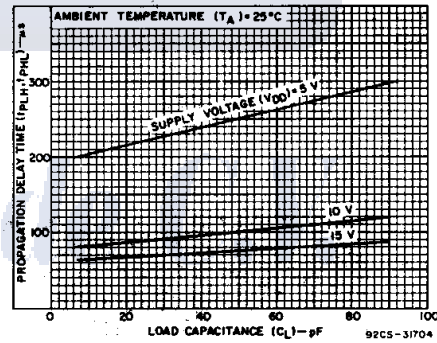


Fig. 11 - Typical propagation delay time as a function of load capacitance for carry-out outputs.

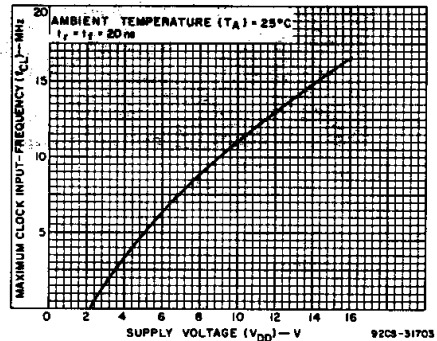


Fig. 12 - Typical maximum clock input-frequency as a function of supply voltage.

3
**COMMERCIAL CMOS
 HIGH VOLTAGE ICs**

CD4026B, CD4033B Types

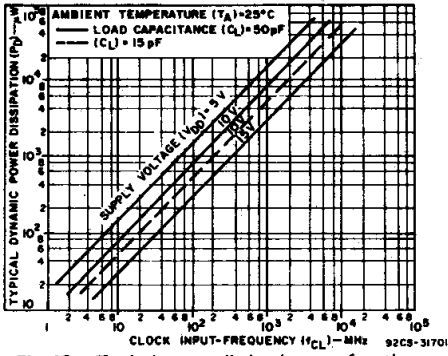


Fig. 13 - Typical power dissipation as a function of clock input frequency.

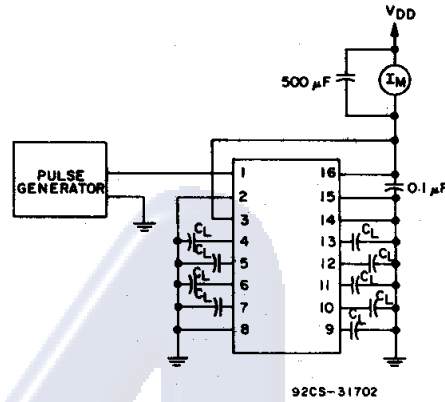


Fig. 14 - Dynamic power dissipation test circuit for CD4033B.

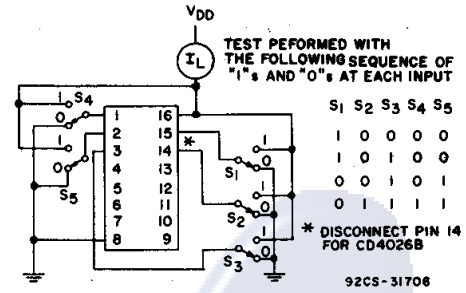
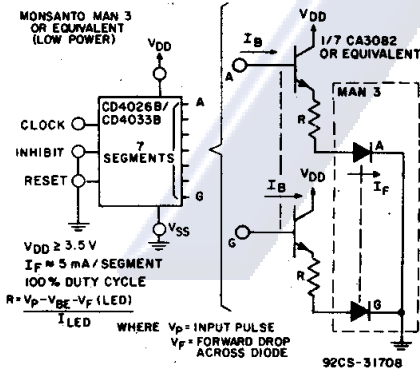
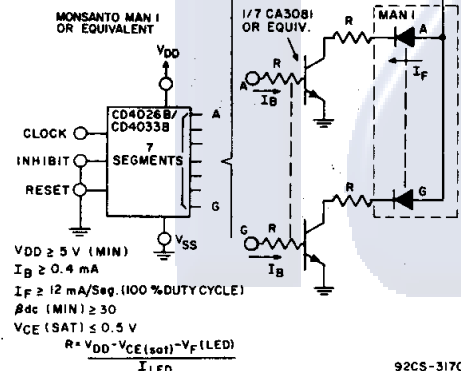


Fig. 15 - Quiescent device current.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALY AVAILABLE LIGHT EMITTING DIODE DISPLAYS



92CS-31708



92CS-31709

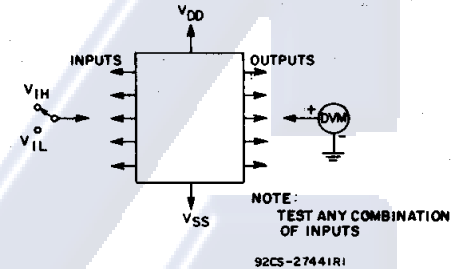


Fig. 16 - Input voltage.

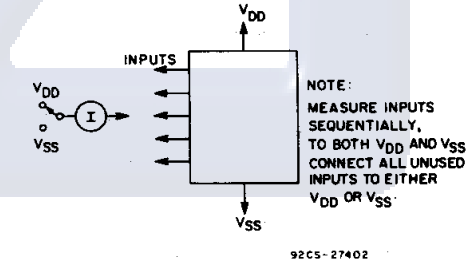
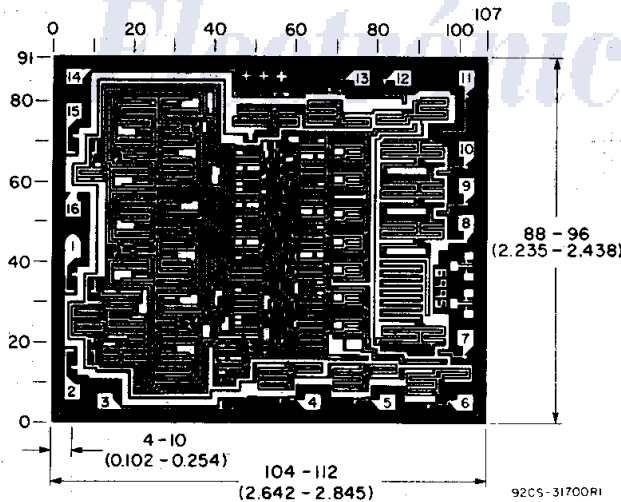
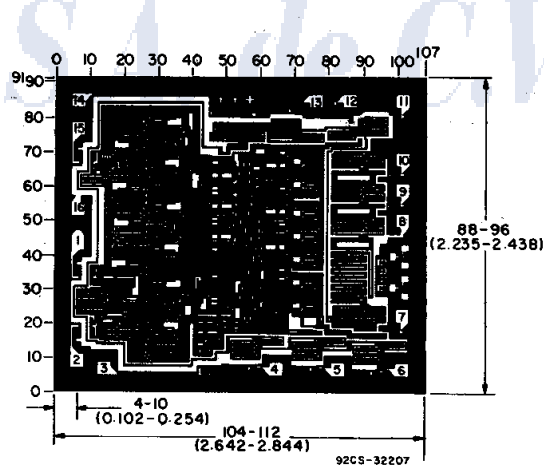


Fig. 17 - Input current.



Chip dimensions and pad layout for CD4026B

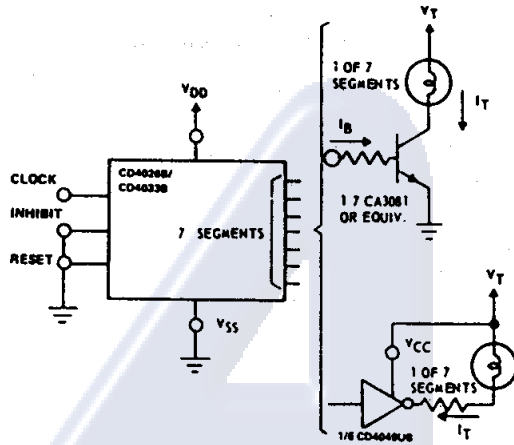
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).



Chip dimensions and pad layout for CD4033B

CD4026B, CD4033B Types

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALY AVAILABLE 7-SEGMENT DISPLAY DEVICES*



INCANDESCENT READOUTS
 RCA Numitron DR2000 Series
TUBE REQUIREMENTS
 $V_T = 3.5-5V$
 $I_T = 24 \text{ mA Segment}$

ASSUMED TRANSISTOR CHARACTERISTICS @ $V_{CC} = 10V \text{ (min.)}$
 $\beta_{dc} \text{ (min.)} \geq 25$
 $V_{CE(sat.)} \leq 0.5V$
 $V_{DD} = 8V \text{ (min.)}$
 $I_B = 1 \text{ mA (min.)}$
 $I_T = 24 \text{ mA (min.)}$

COMMON
 $V_{CC} = 10V \text{ (min.)}$
 $V_{CE} \leq 2V$
 $I_T = 8 \text{ mA (min.)}$
 $V_T = 3.5V \text{ TO } 6V$

COMMON
 @ $V_{CC} = 10V \text{ (min.)}$
 $V_{CE} \leq 0.6V$
 $I_T = 8 \text{ mA (min.)}$

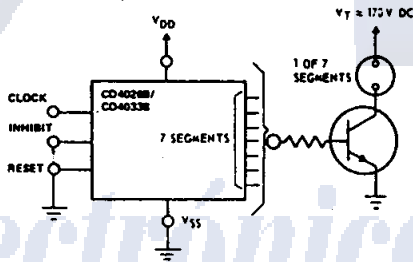
LOW-POWER INCANDESCENT READOUTS
 PINLITES INC-Series O and R

| TUBE REQUIREMENTS | $V_T \text{ (V)}$ | mA/Segment |
|-------------------|-------------------|---------------------|
| O-03-15 | 1.5 | 8 |
| O-04-30 | 3 | 8 |
| O-06-30 | 3 | 8 |
| R-R3-20 | 2 | 4.3 |
| R-R4-30 | 3 | 4.3 |

ASSUMED TRANSISTOR CHARACTERISTICS
 $\beta_{dc} \text{ (min.)} \geq 30$
 $V_{CE(sat.)} \leq 0.5V$
 $V_{CC} \geq 3.5V \text{ (min.)}$
 $I_B \geq 0.25 \text{ mA (min.)}$
 $I_T \leq 7.5 \text{ mA (min.)}$

92CM-31707

* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10 V.



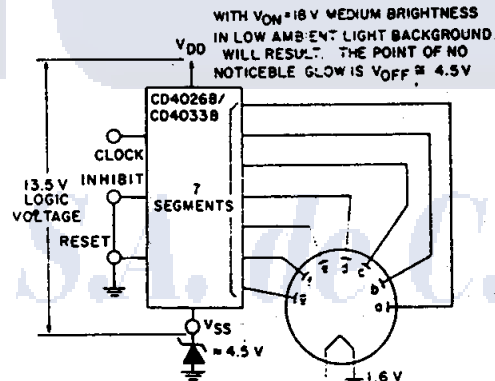
NEON READOUT (NIXIE TUBE*)

- Alco Electronics - MG19
- Burroughs - B5971, B7971, B8971

| TUBE REQUIREMENTS | $V_T \text{ (Vdc)}$ | mA Segment |
|------------------------|---------------------|---------------------|
| Alco MG19 | 180 | 0.5 |
| Burroughs B5971 | 170 | 3 |
| Burroughs B7971, B8971 | 170 | 6 |

▲ (Trademark) Burroughs Corp.
TRANSISTOR CHARACTERISTICS
 Leakage with transistor cutoff - 0.05 mA
 $V_{(BR)CER} > V_T$
 $\beta_{dc} \text{ (min.)} > 30$

92CS-31710



LOW VOLTAGE VACUUM FLUORESCENT READOUTS

- Tung-Sol DIGIVAC S/G ; Type DT1704A or DT1705C
 - Nippon Electric (NEC); Type DG12E or LD91S
- TUBE REQUIREMENTS:** 100 to 300 μA /segment at tube voltages of 12 V to 25 V depending on required brightness Filament requirement 45 mA at 1.6 V, ac or dc.

▲ (Trademark) Wagner Electric Co.

92CS-31711

3
 COMMERCIAL CMOS
 HIGH VOLTAGE ICs

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4026BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4026BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4026BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4026BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4026BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4026BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4026BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4026BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4033BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4033BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4033BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4033BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4033BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4033BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4033BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4033BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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AG

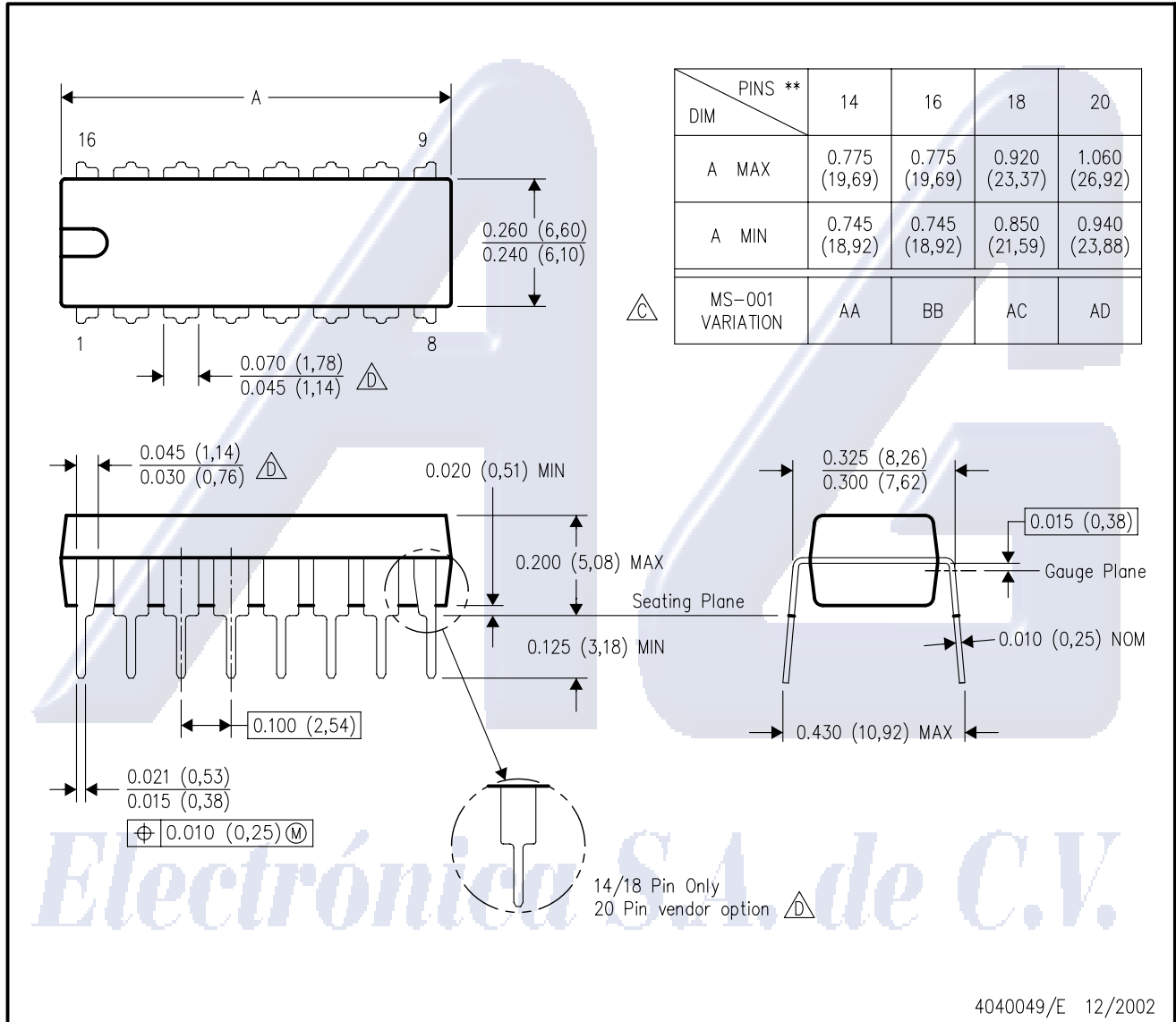
Electrónica S.A. de C.V.

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



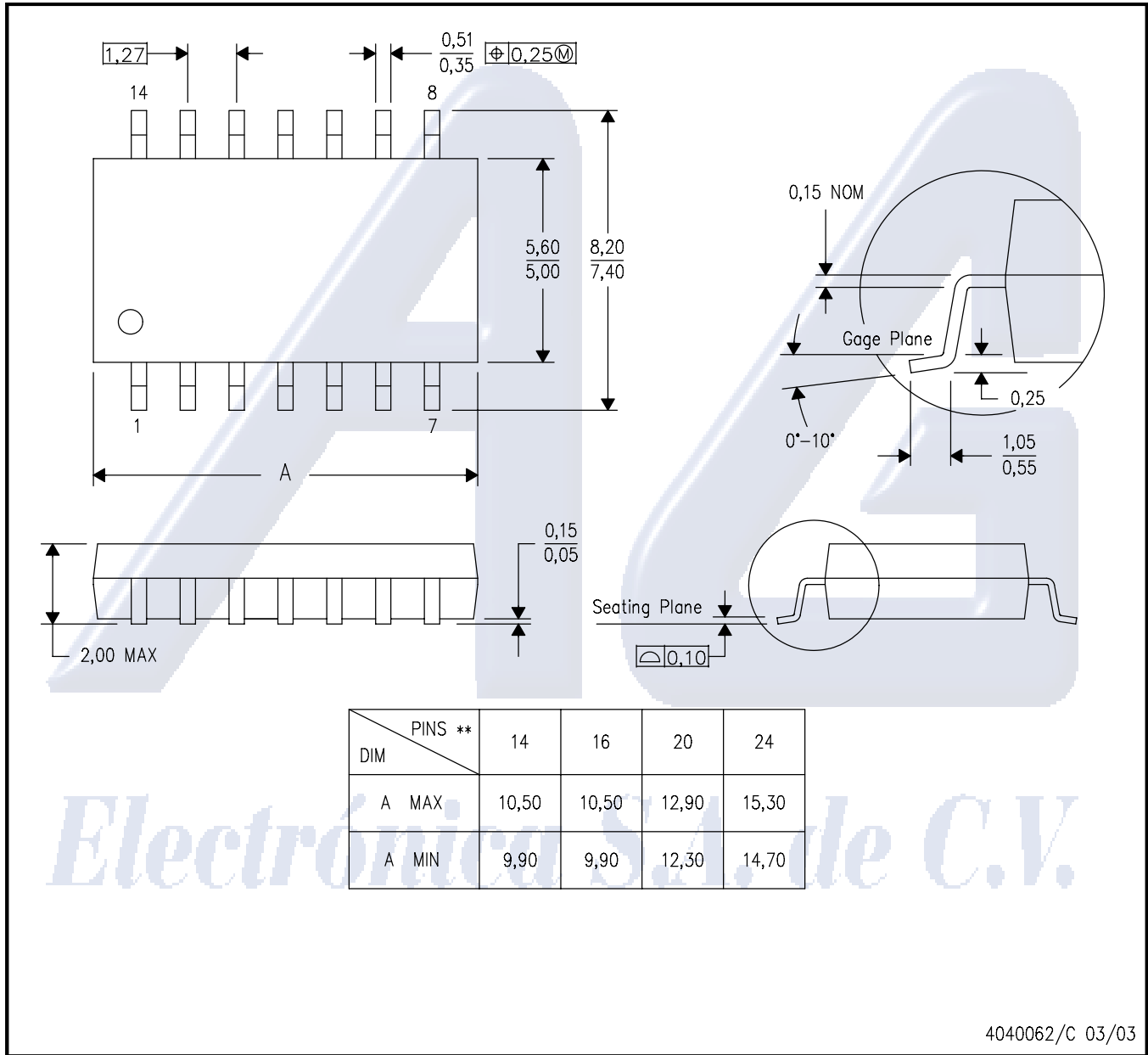
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

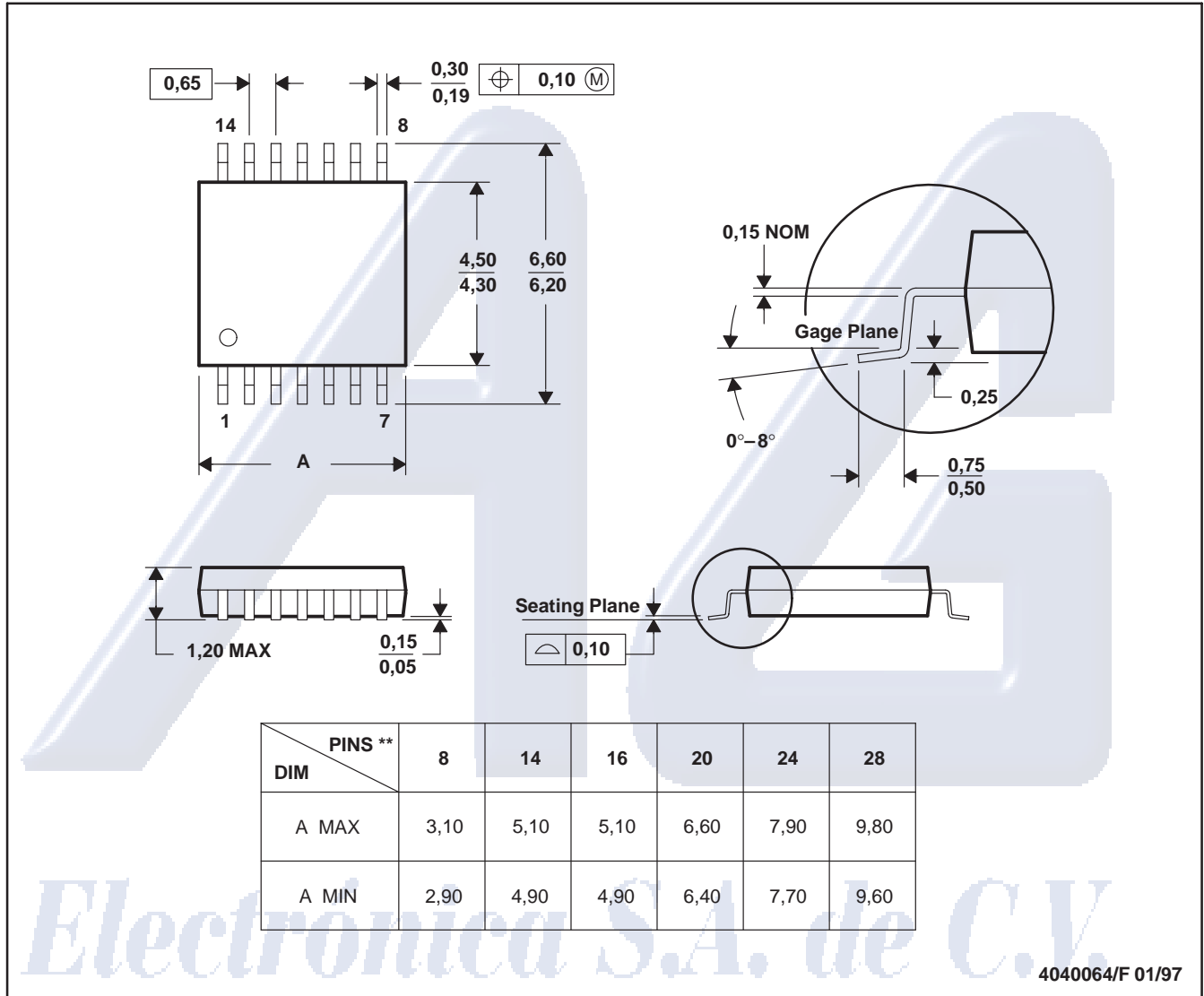
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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