

## CMOS

### Quad Clocked "D" Latch

High-Voltage Types (20-Volt Rating)

■ CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical. Information present at the data input is transferred to outputs Q and  $\bar{Q}$  during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (D, DR, DT, DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

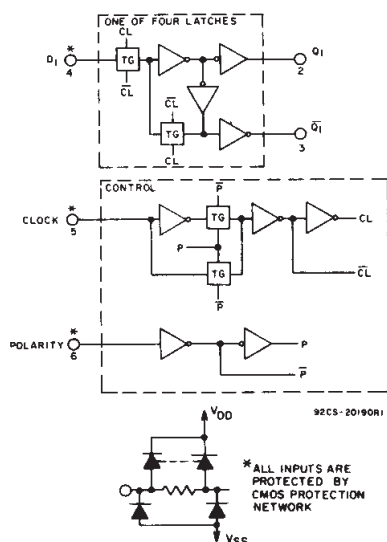


Fig. 1 – Logic block diagram and truth table.

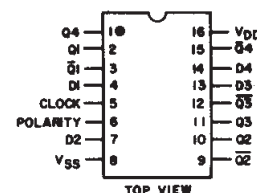
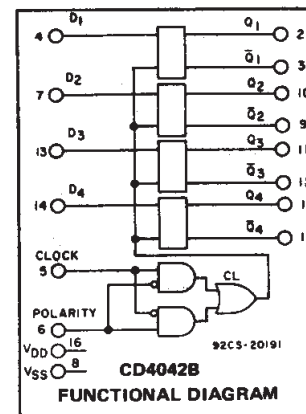
#### Features:

- Clock polarity control
- Q and  $\bar{Q}$  outputs
- Common clock
- Low power TTL compatible
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### Applications:

- Buffer storage
- Holding register
- General digital logic

## CD4042B Types



92CS-20756R1

#### TERMINAL ASSIGNMENT

#### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I <sub>DD</sub> Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output High (Source) Current, I <sub>OH</sub> Min.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

## CD4042B Types

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal)

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD}$  +0.5V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$ mA

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12mW/ $^\circ\text{C}$  to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$ )	—	3	18	V
Clock Pulse Width, $t_W$	5	200	—	ns
	10	100	—	
	15	60	—	
Setup Time, $t_S$	5	50	—	ns
	10	30	—	
	15	25	—	
Hold Time, $t_H$	5	120	—	ns
	10	60	—	
	15	50	—	
Clock Rise or Fall Time: $t_r, t_f$	5, 10, 15	Not rise or fall time sensitive.		$\mu\text{s}$

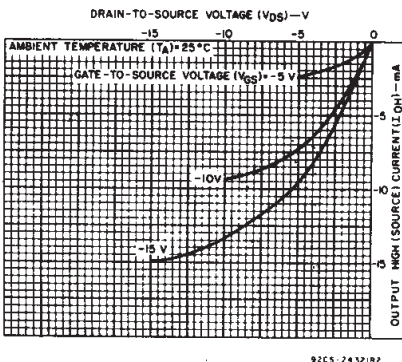


Fig. 5 — Minimum output high (source) current characteristics.

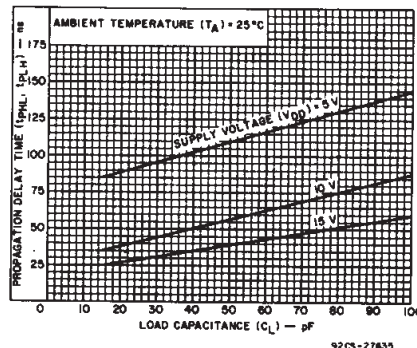


Fig. 6 — Typical propagation delay time vs. load capacitance—data to Q.

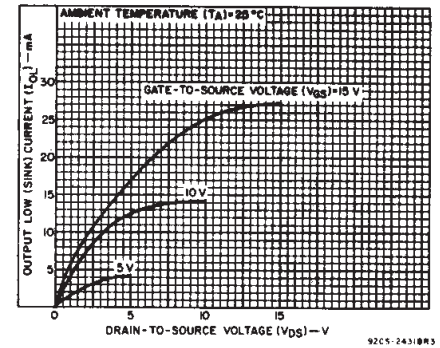


Fig. 2 — Typical output low (sink) current characteristics.

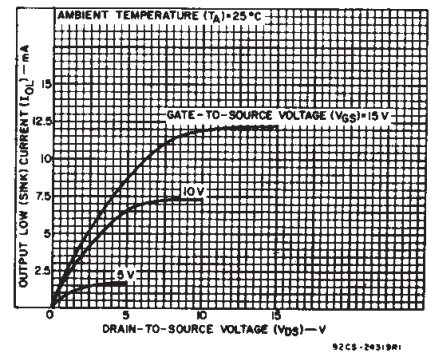


Fig. 3 — Minimum output low (sink) current characteristics.

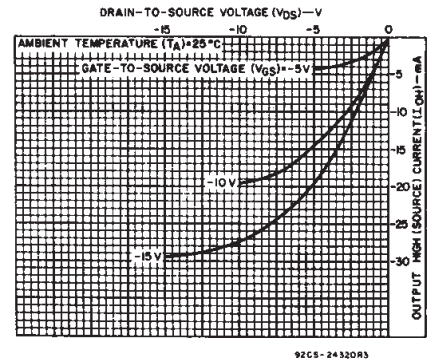


Fig. 4 — Typical output high (source) current characteristics.

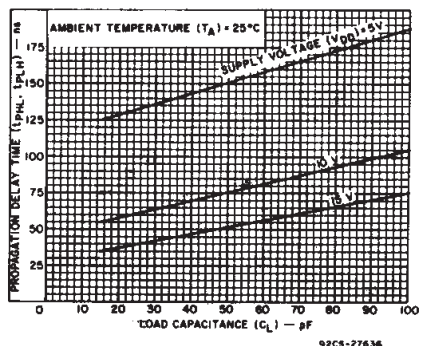


Fig. 7 — Typical propagation delay time vs. load capacitance—data to  $\bar{Q}$ .

# CD4042B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  
 $R_L = 200\text{ K}\Omega$

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time: $t_{PHL}, t_{PLH}$ Data In to Q	5 10 15	110 55 40	220 110 80	ns
Data In to $\bar{Q}$	5 10 15	150 75 50	300 150 100	ns
Clock to Q	5 10 15	225 100 80	450 200 160	ns
Clock to $\bar{Q}$	5 10 15	250 115 90	500 230 180	ns
Transition Time: $t_{THL}, t_{TLH}$	5 10 15	100 50 40	200 100 80	ns
Minimum Clock Pulse Width, $t_W$	5 10 15	100 50 30	200 100 60	ns
Minimum Hold Time, $t_H$	5 10 15	60 30 25	120 60 50	ns
Minimum Setup Time, $t_S$	5 10 15	0 0 0	50 30 25	ns
Clock Input Rise or Fall Time: $t_r, t_f$	5, 10 15	Not rise or fall time sensitive.		$\mu\text{s}$
Input Capacitance, $C_{IN}$ Polarity Input	—	5	7.5	pF
All Other Inputs	—	7.5	15	pF

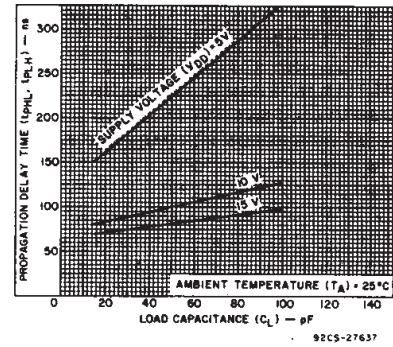


Fig. 8 — Typical propagation delay time vs. load capacitance—clock to Q

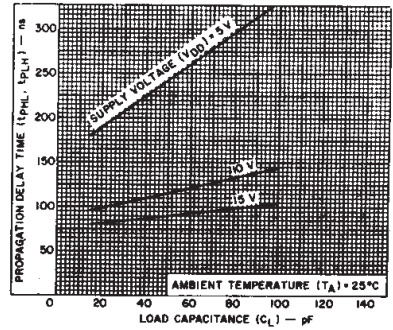
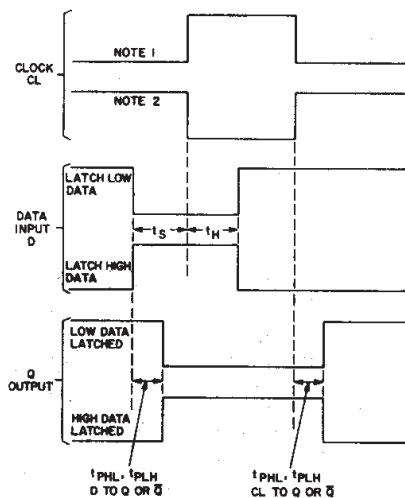


Fig. 9 — Typical propagation delay time vs. load capacitance—clock to  $\bar{Q}$ .



NOTES:  
 1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.  
 2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

92CS-27630

Fig. 12 — Dynamic test parameters.

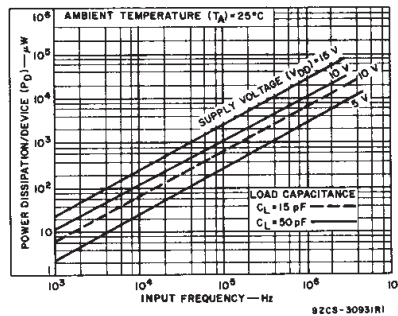


Fig. 10 — Typical power dissipation vs. frequency.

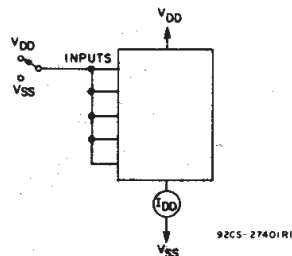


Fig. 13 — Quiescent device current test circuit.

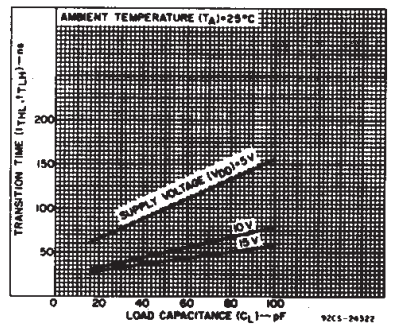


Fig. 11 — Typical transition time vs. load capacitance.

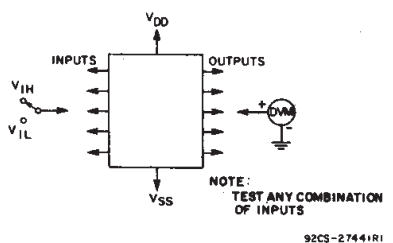


Fig. 14 — Input voltage test circuit.

## CD4042B Types

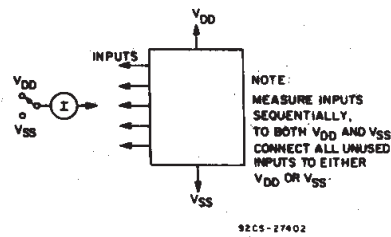
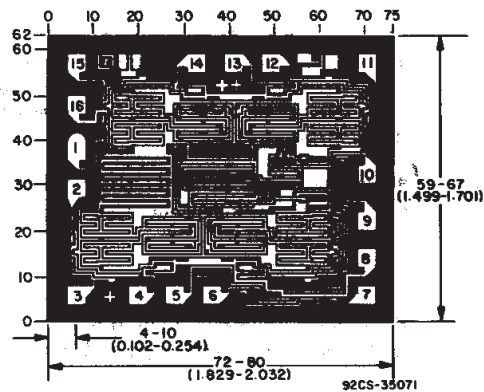


Fig. 15 - Input current test circuit.

### Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

3

COMMERCIAL CMOS  
HIGH VOLTAGE ICs

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4042BD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4042BDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4042BDT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4042BDW	ACTIVE	SOIC	DW	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD4042BDWR	ACTIVE	SOIC	DW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD4042BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4042BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4042BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4042BM	OBSOLETE	SOIC	D	16		None	Call TI	Call TI
CD4042BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4042BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4042BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

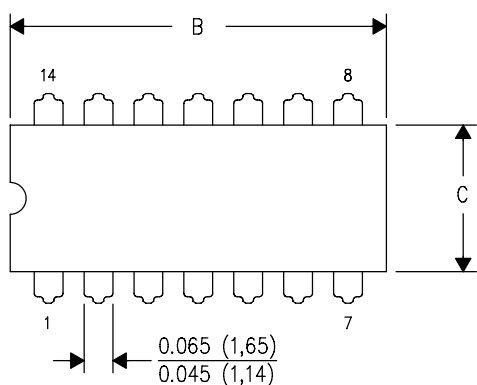
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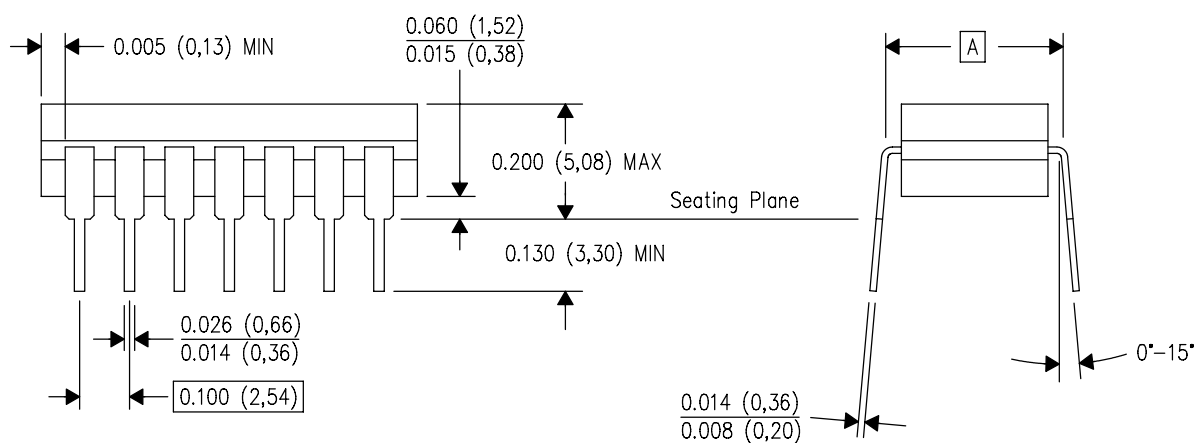
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



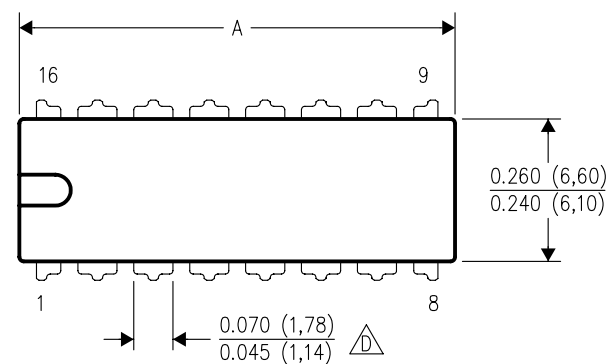
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

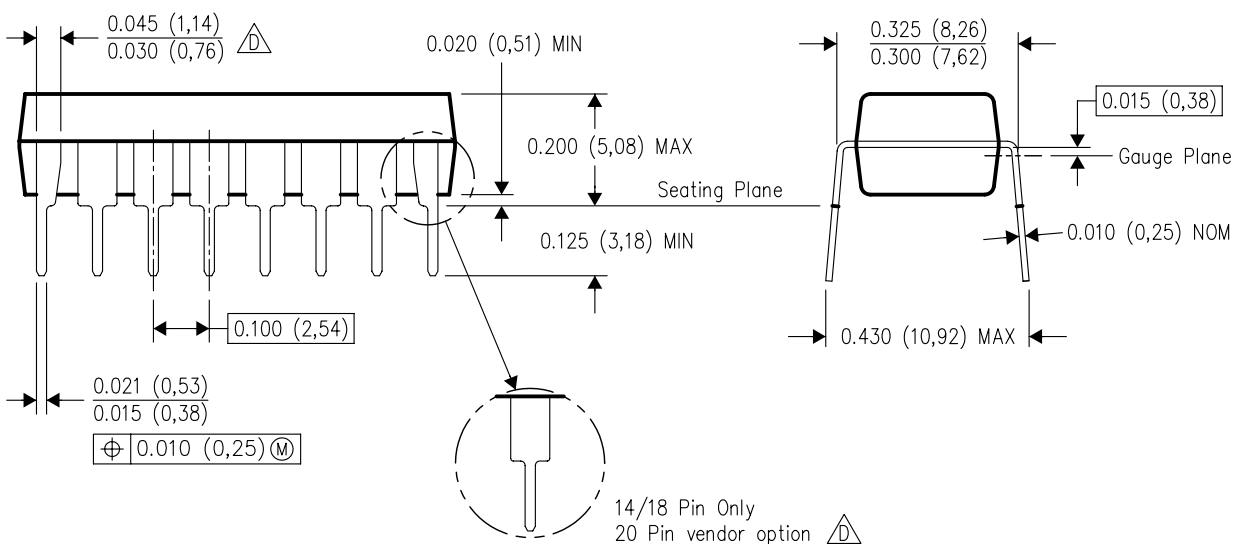
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



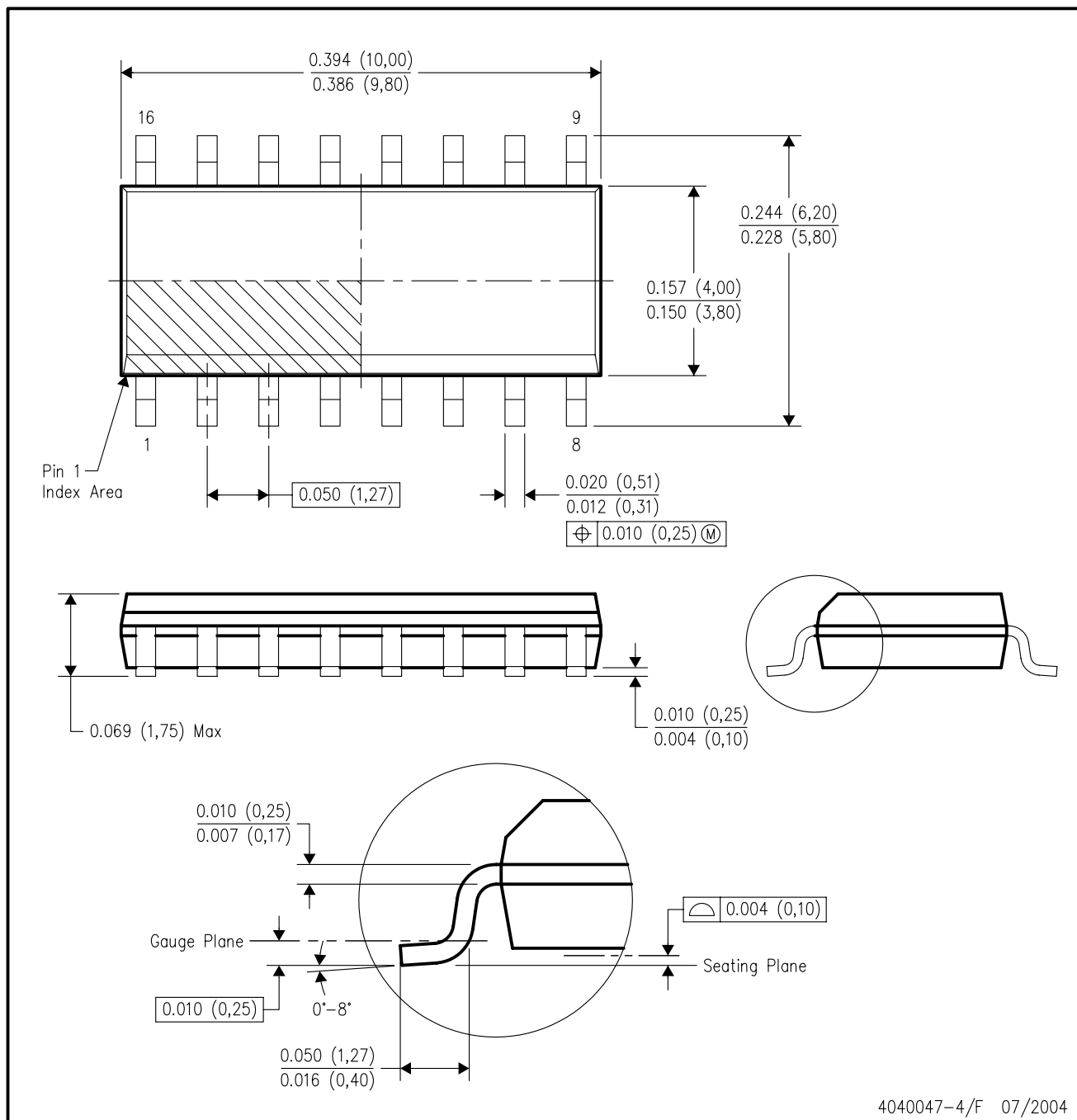
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE

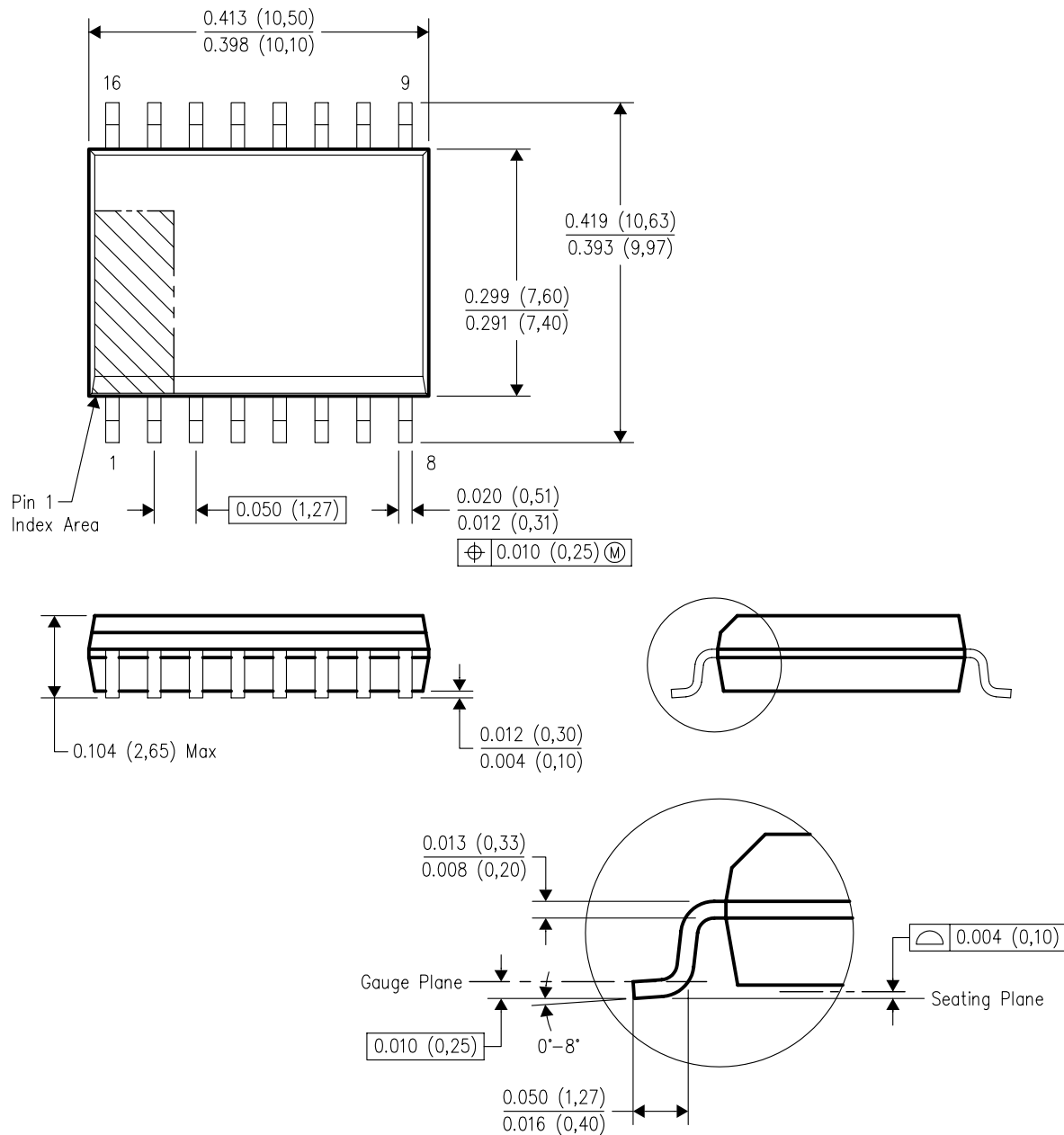


4040047-4/F 07/2004



## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

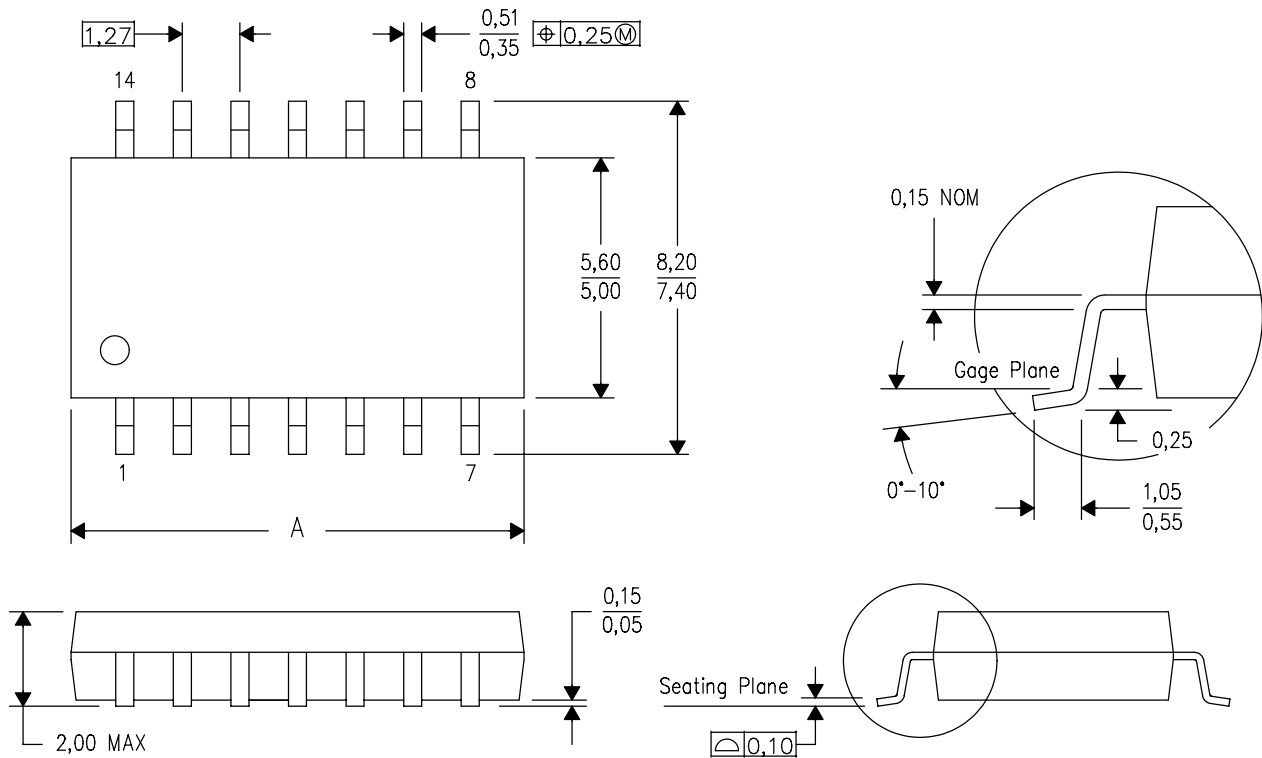
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed  $0.006 (0,15)$ .
  - Falls within JEDEC MS-013 variation AA.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

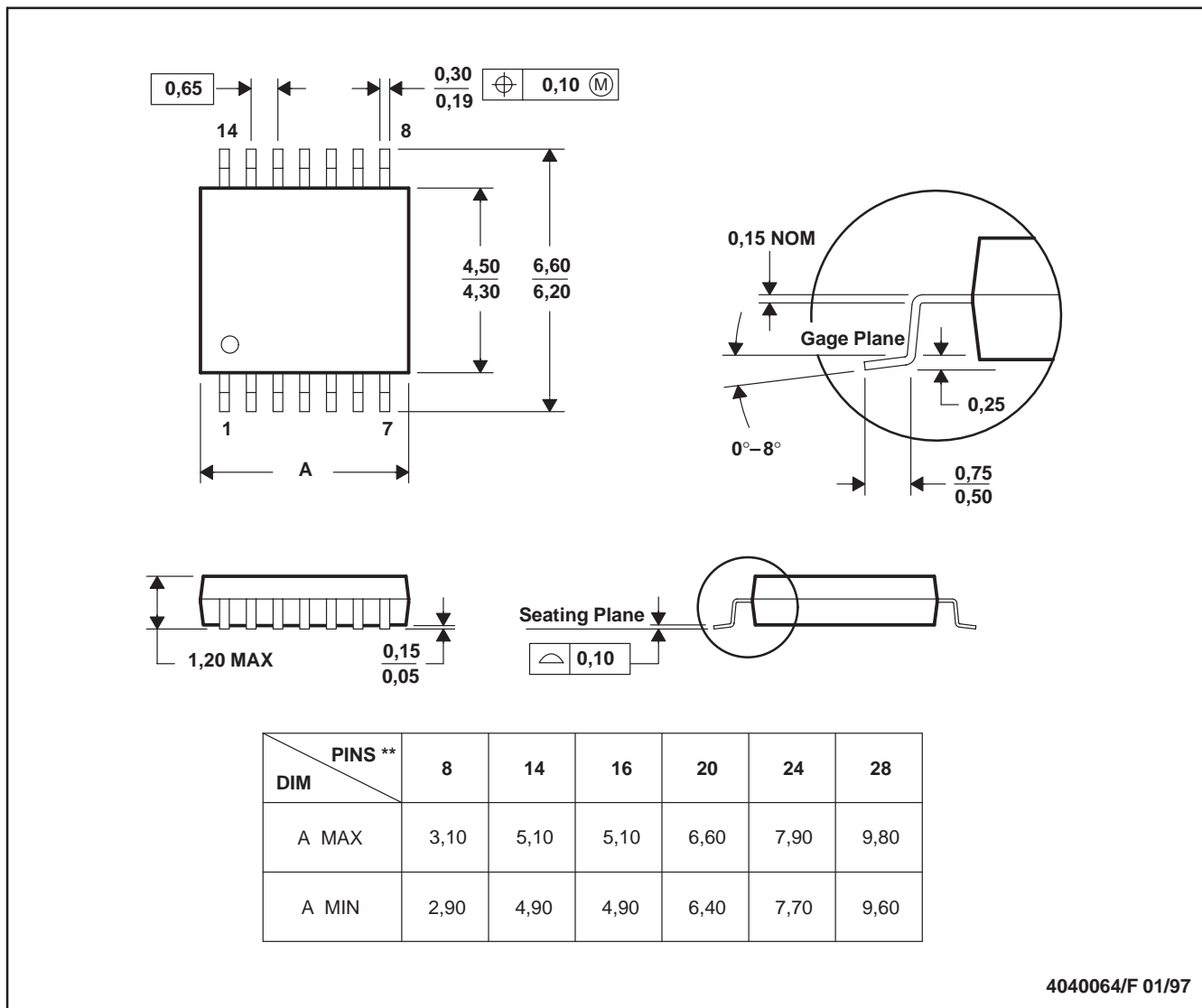
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - Falls within JEDEC MO-153

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