TEXAS INSTRUMENTS

CD4508B Types

CMOS Dual 4-Bit Latch

High-Voltage Types (20-Volt Rating)

■ CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (PW and PWR suffixes).

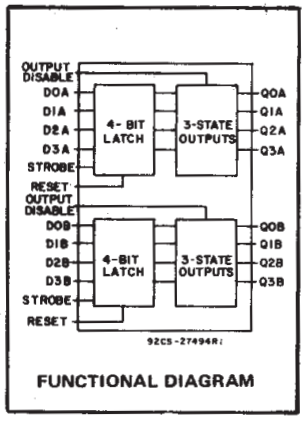
The CD4508B is similar to industry type MC14508.

Features:

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PHL} = t_{PLH} = 70$ ns (typ.) at $V_{DD} = 10$ V and $C_L = 50$ pF
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Buffer storage
- Holding registers
- Data storage and multiplexing



FUNCTIONAL DIAGRAM

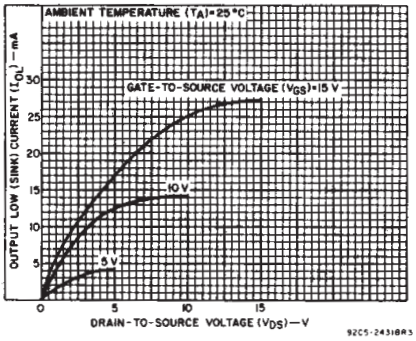


Fig.2 – Typical output low (sink) current characteristics.

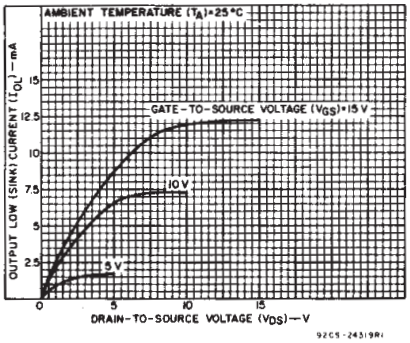


Fig.3 – Minimum output low (sink) current characteristics.

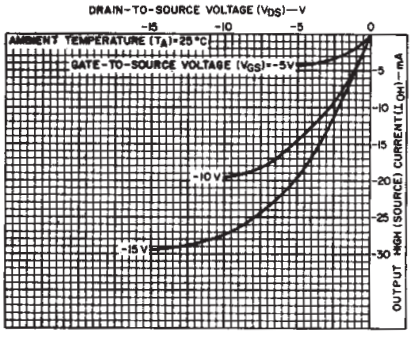


Fig.4 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

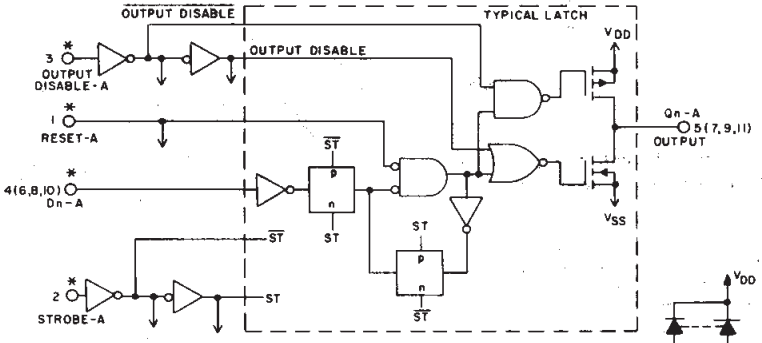
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Reset Pulse Width, $t_{W(R)}$	5	200	–	ns
	10	140	–	
	15	100	–	
Strobe Pulse Width, $t_{W(st)}$	5	140	–	
	10	80	–	
	15	70	–	
Setup Time, t_{SU}	5	50	–	
	10	30	–	
	15	20	–	
Hold Time, t_H	5	0	–	
	10	0	–	
	15	0	–	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$±10^{-4}$	±0.4	μA



TRUTH TABLE

RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL X = DON'T CARE
0 = LOW LEVEL Z = HIGH IMPEDANCE

Fig. 7 — Logic diagram (A-Section), 1 of 4 identical latches with common output disable, reset, and strobe.

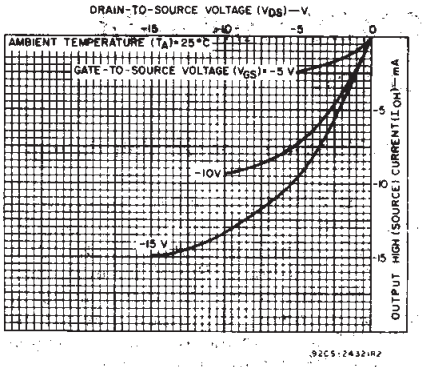


Fig. 4 — Minimum output high (source) current characteristics.

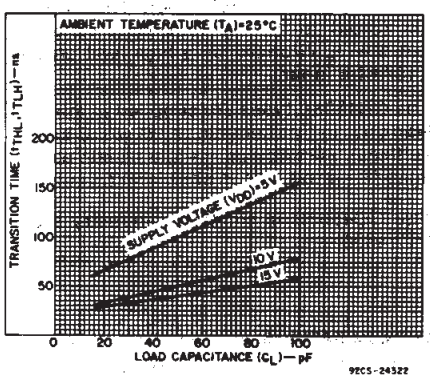


Fig. 5 — Typical transition time as a function of load capacitance.

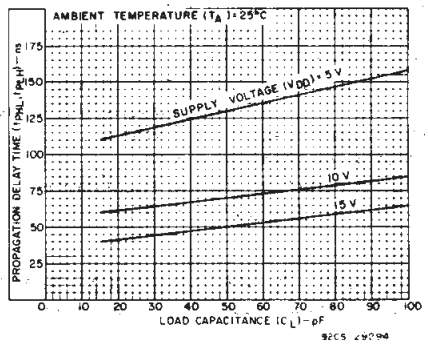


Fig. 6 — Typical propagation delay time as a function of load capacitance (strobe to data out).

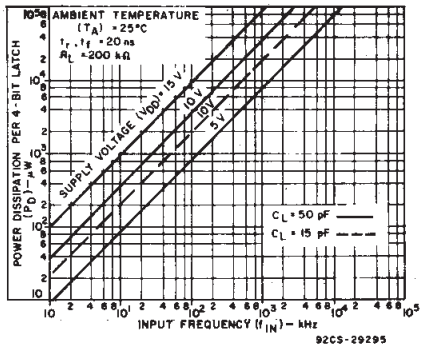


Fig. 8 — Typical power dissipation as a function of frequency.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	V_{DD}	LIMITS Typ.	LIMITS Max.	UNITS
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Reset Pulse Width, $t_{W(R)}$		5	100	200	
		10	70	140	
		15	50	100	
Minimum Strobe Pulse Width, $t_{W(st)}$		5	70	140	
		10	40	80	
		15	35	70	
Minimum Setup Time, t_{SU}		5	25	50	
		10	15	30	
		15	10	20	
Minimum Hold Time, t_H		5	0	0	
		10	0	0	
		15	0	0	
Propagation Delay Times: t_{PHL}, t_{PLH} Strobe to Data Out		5	130	260	
		10	70	140	
		15	50	100	
Data In to Data Out		5	105	210	
		10	60	120	
		15	45	90	
Reset to Data Out		5	90	180	
		10	50	100	
		15	40	80	
3-State Propagation Delay Times: Output High to High Impedance, t_{PHZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output High, t_{PZH}		5	90	180	
		10	50	100	
		15	35	70	
Output Low to High Impedance, t_{PLZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output Low, t_{PZL}		5	90	180	
		10	50	100	
		15	35	70	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF

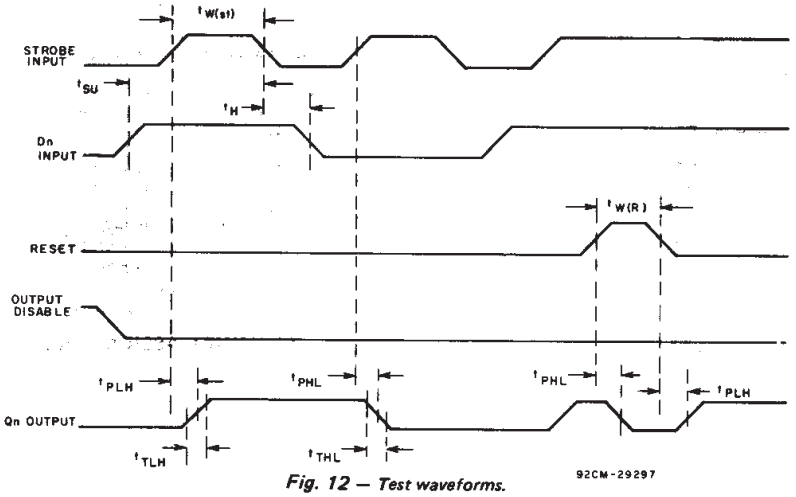


Fig. 12 – Test waveforms.

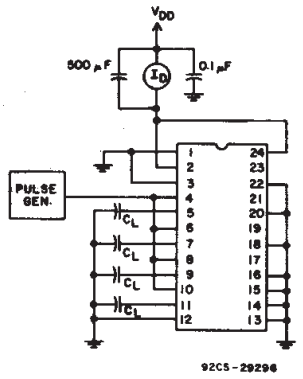


Fig.9 – Power dissipation test circuit.

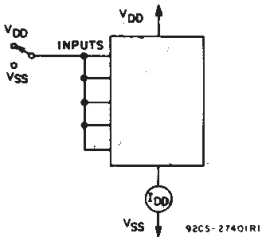


Fig.10 – Quiescent device current test circuit.

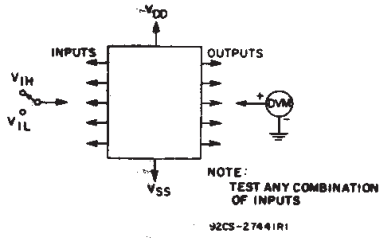


Fig.11 – Input voltage test circuit.

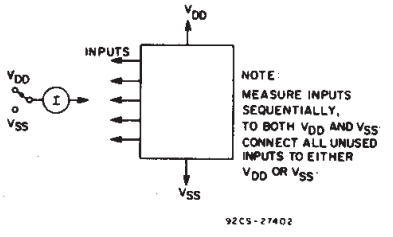


Fig. 13 – Input current test circuit.

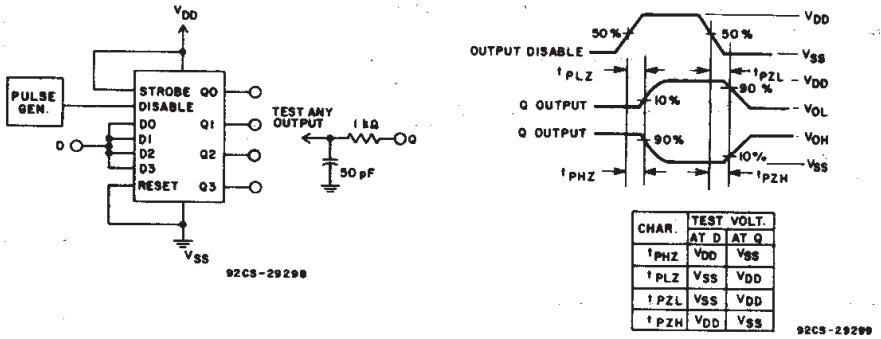


Fig. 14 – Output disable test circuit and waveforms.

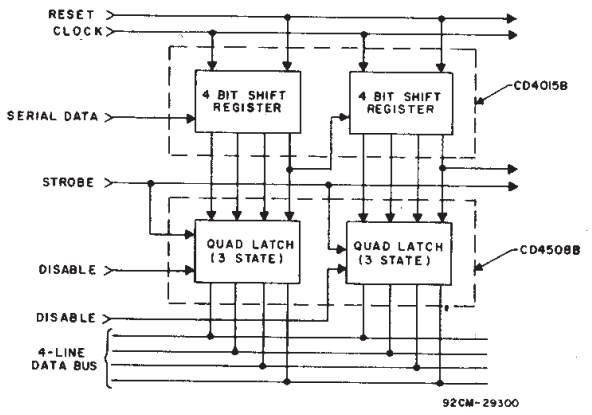


Fig. 15 – Bus register.

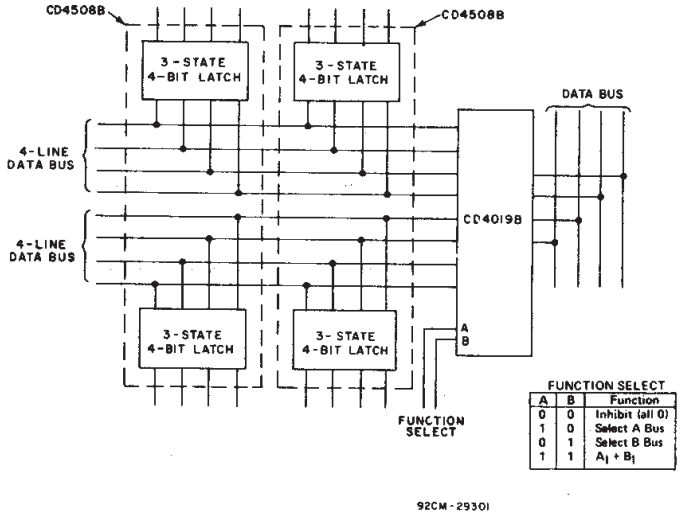
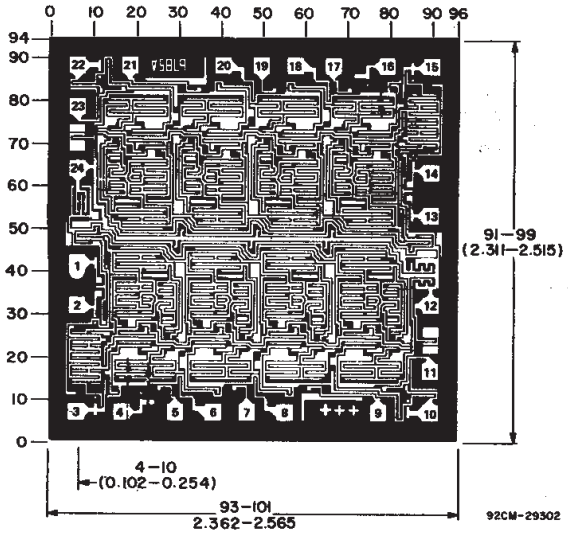
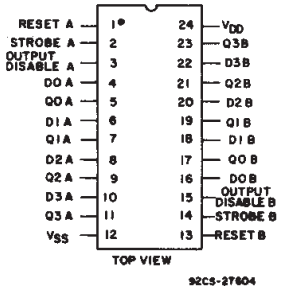


Fig. 16 – Dual multiplexed bus register with function select.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Chip dimensions and pad layout for CD4508B.



TERMINAL ASSIGNMENT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4508BD3	ACTIVE	CDIP SB	JD	24	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	CD4508BD/3	Samples
CD4508BF3A	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4508BF3A	Samples
CD4508BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508BM	Samples
CD4508BM96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508BM	Samples
CD4508BME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508BM	Samples
CD4508BNSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4508B	Samples
CD4508BPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM508B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD4508B, CD4508B-MIL :

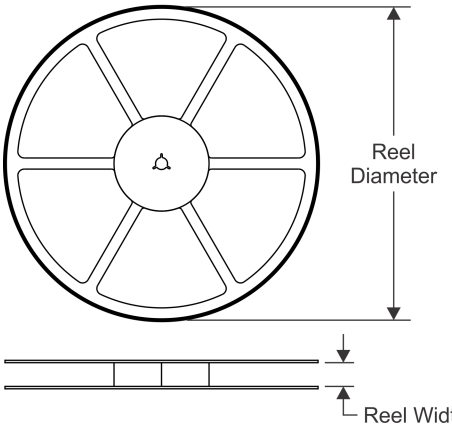
- Catalog: CD4508B
- Military: CD4508B-MIL

NOTE: Qualified Version Definitions:

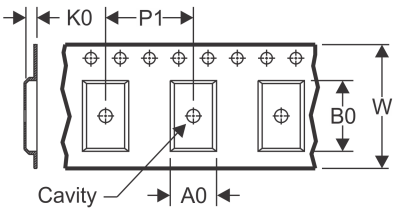
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

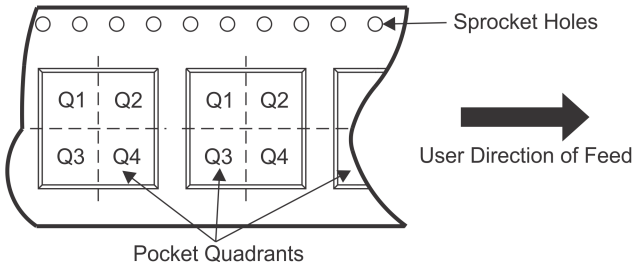


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

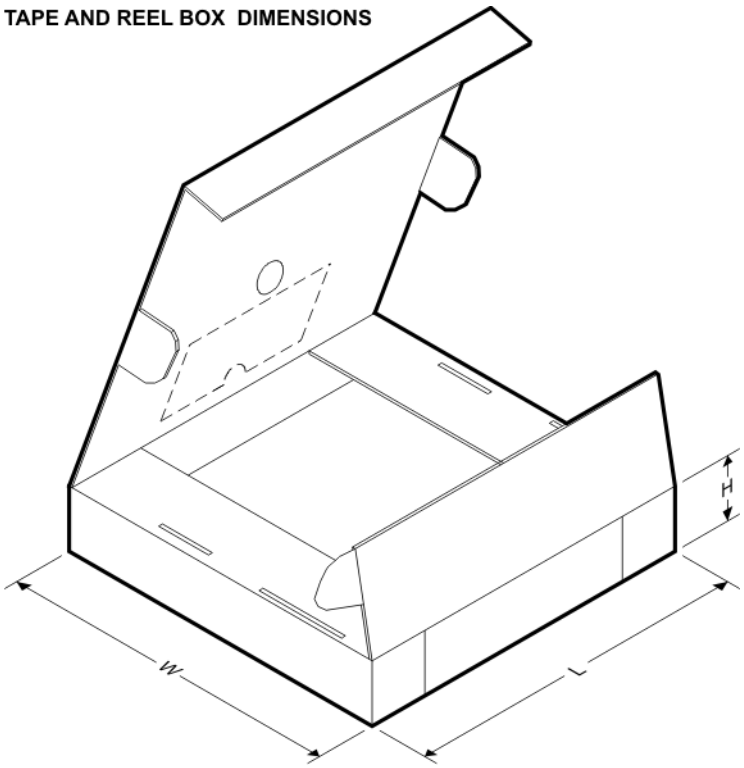
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4508BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4508BNSR	SO	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

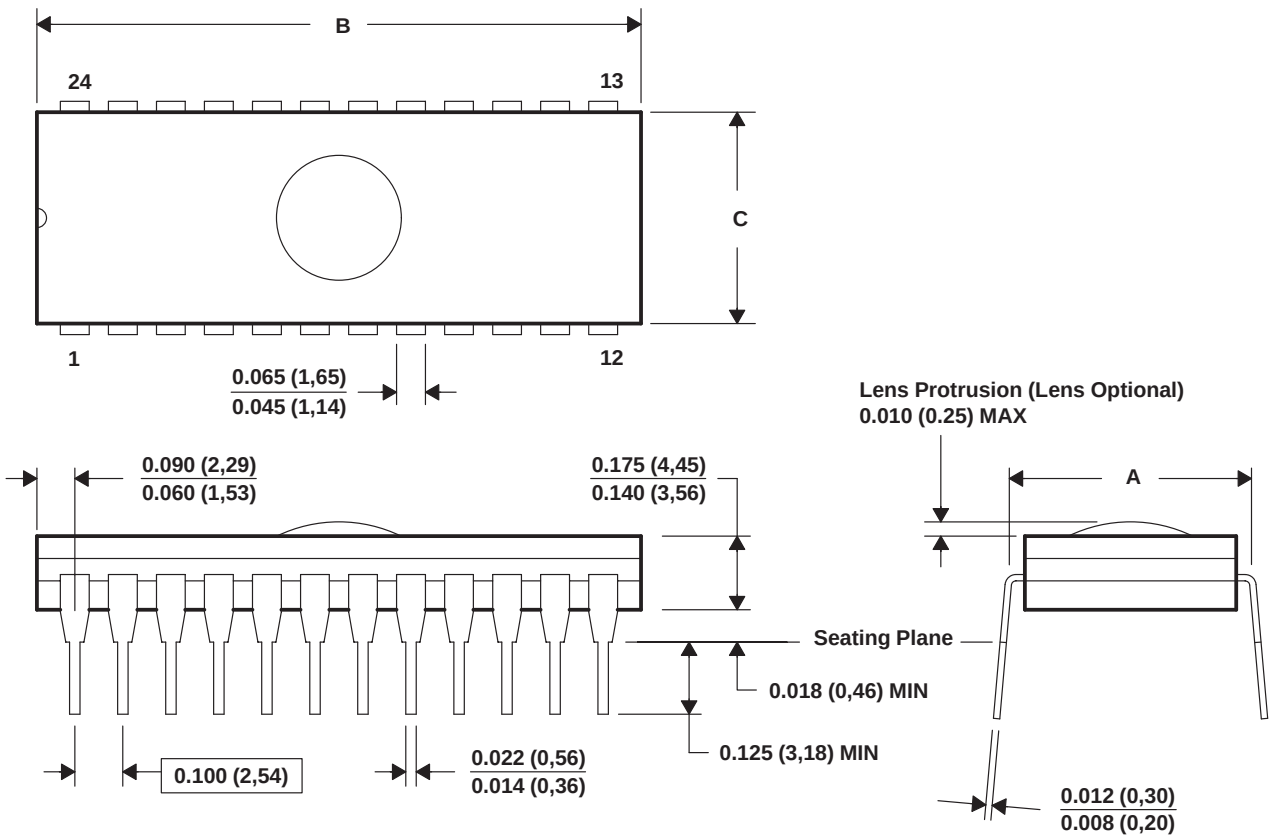


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4508BM96	SOIC	DW	24	2000	367.0	367.0	45.0
CD4508BNSR	SO	NS	24	2000	367.0	367.0	45.0

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

24 PINS SHOWN



DIM	PINS **	24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
"A"	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
"B"	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
"C"	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

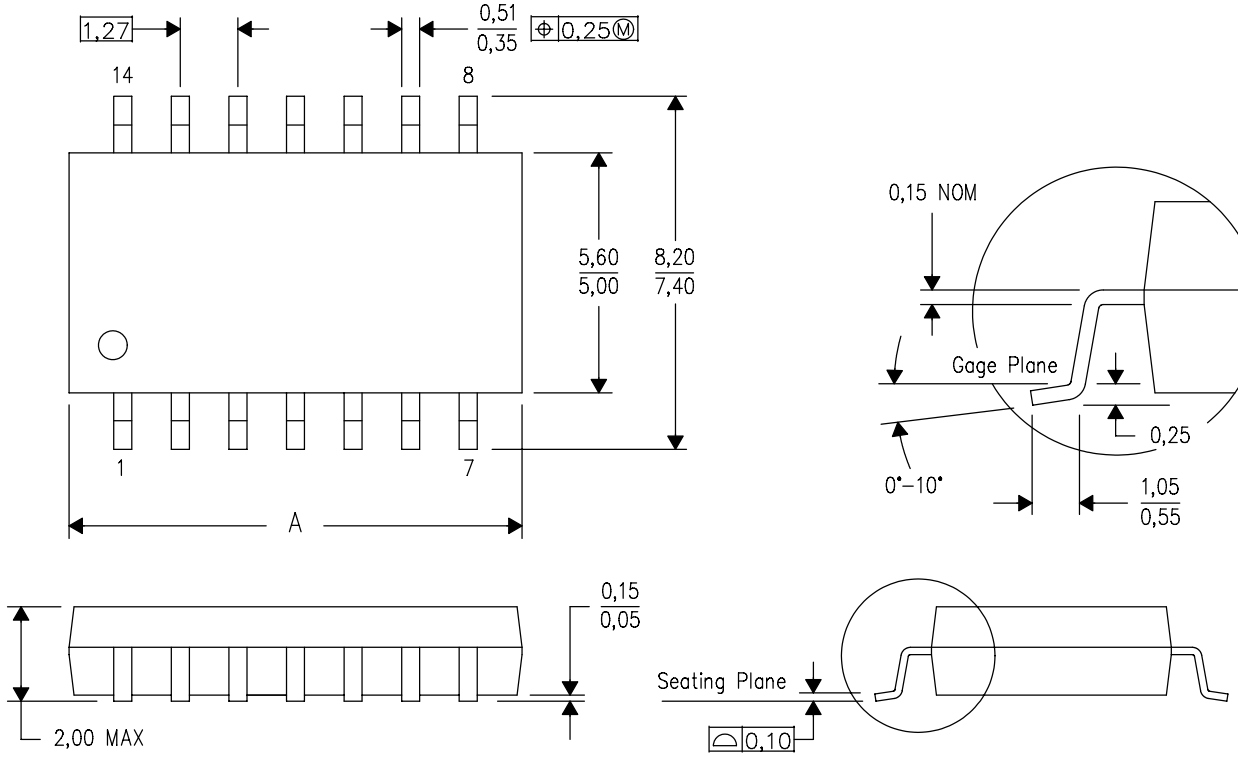
4040084/C 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



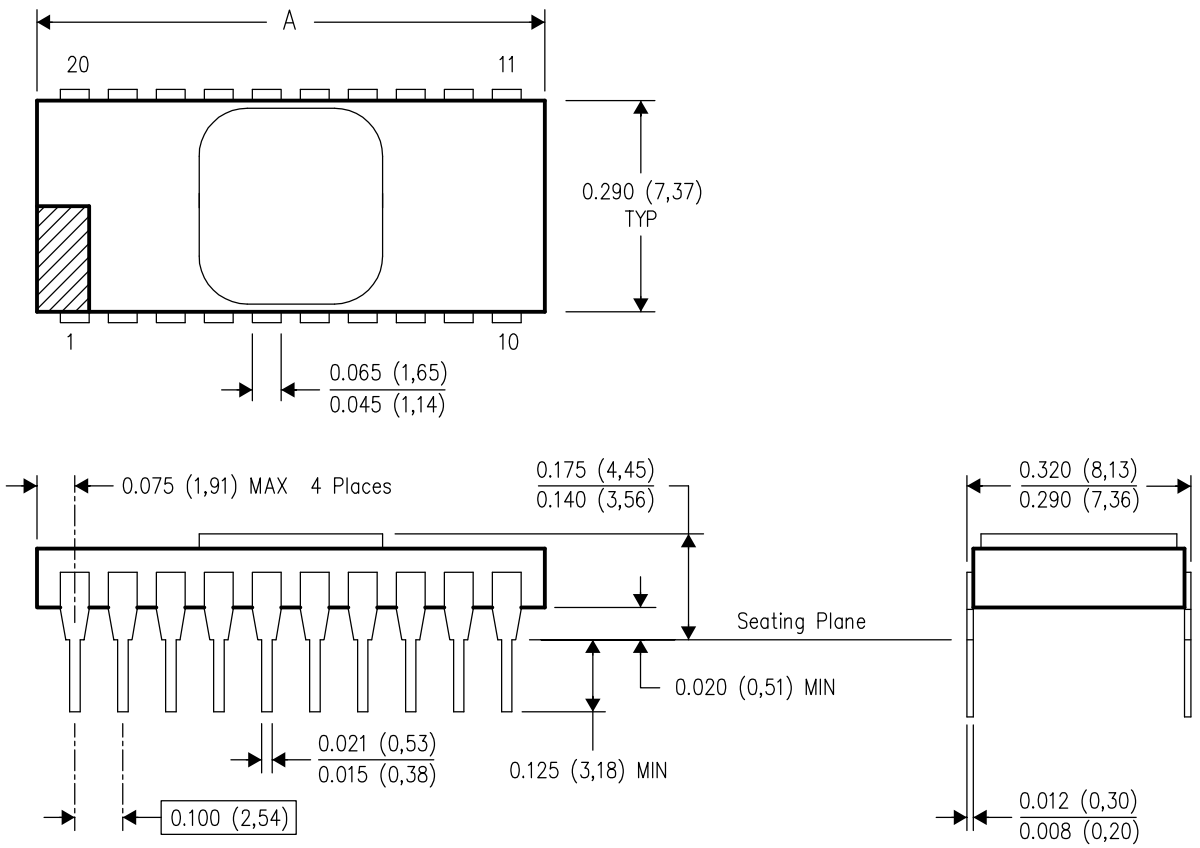
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN

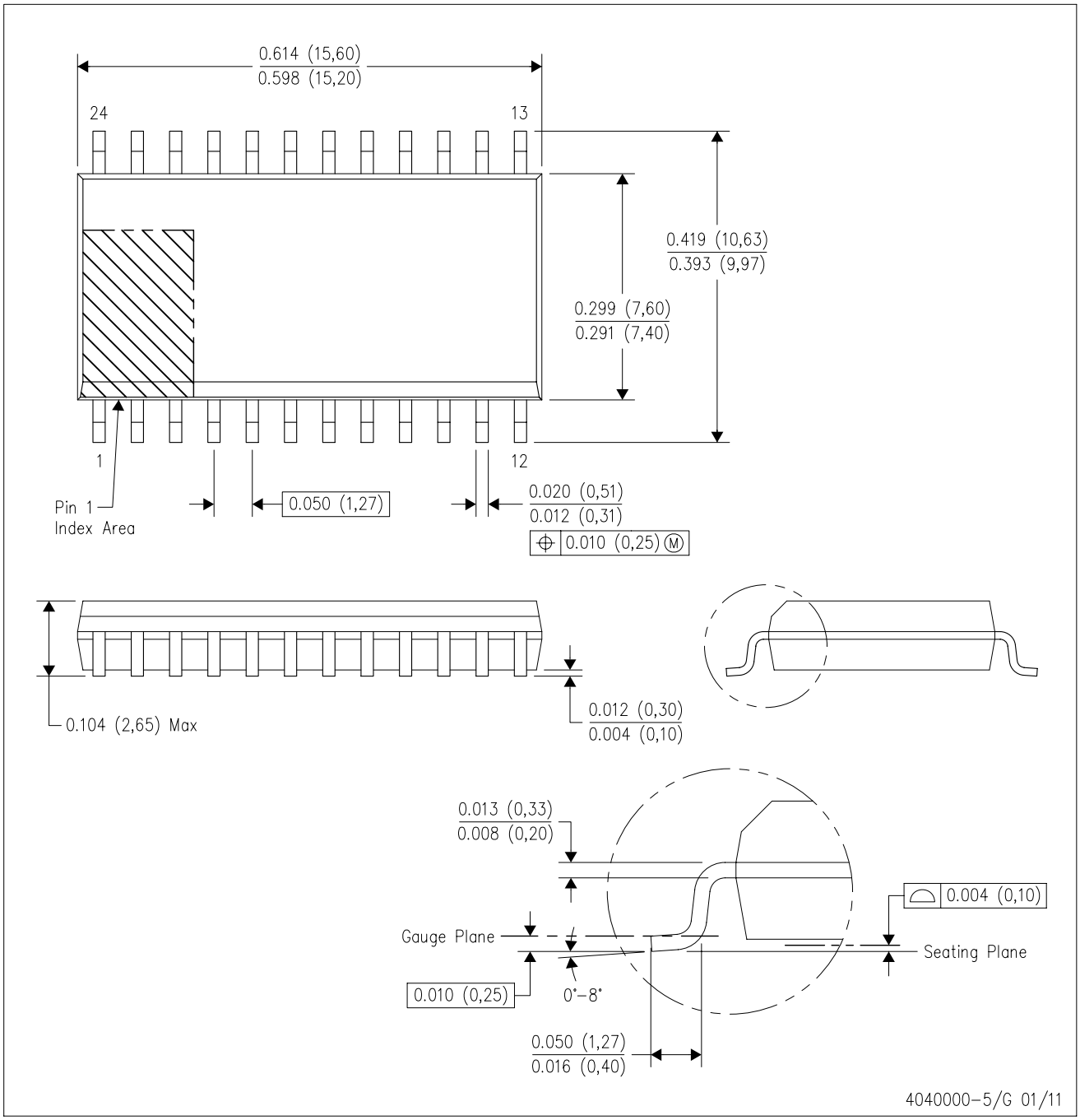


DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

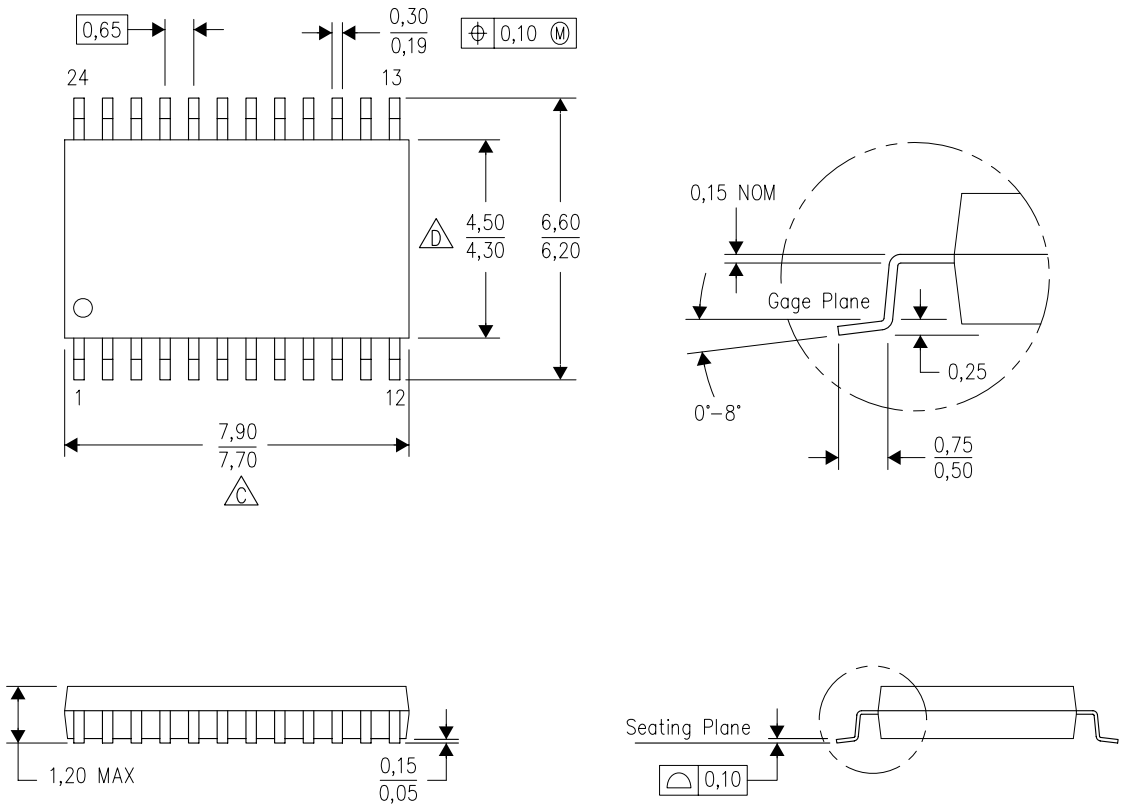
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

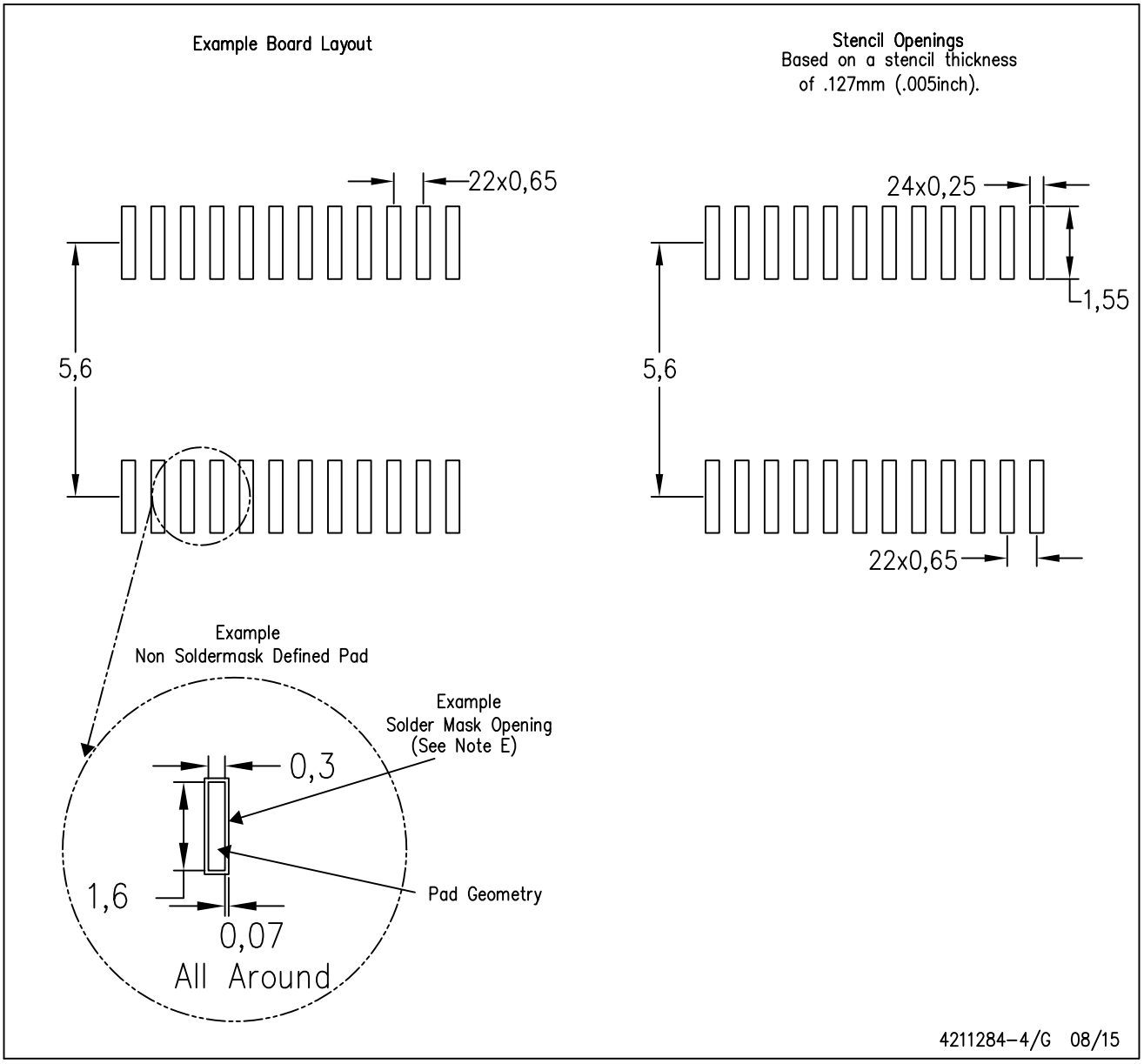
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.