FAIRCHILD
SEMICONDUCTOR

FDD5N50

N-Channel UniFET^{TM} II MOSFET

500 V, 4 A, 1.4 Ω

Features

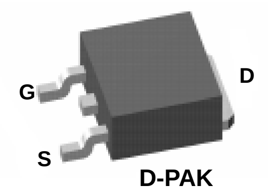
- $R_{DS(on)}$ = 1.15 Ω (Typ.) @ V_{GS} = 10 V, I_D = 2 A
- Low Gate Charge (Typ. 11 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- RoHS Compliant

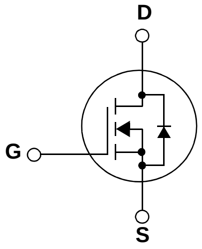
Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFET^{TM} MOSFET is Fairchild Semiconductor$^{®}$'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FDD5N50	Unit
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)	4	A
		- Continuous (T_C = 100°C)	2.4	
I_{DM}	Drain Current	- Pulsed (Note 1)	16	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		256	mJ
I_{AR}	Avalanche Current (Note 1)		4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	40	W
		- Derate above 25°C	0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FDD5N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5N50	FDD5N50TM	D-PAK	380mm	16mm	2500
FDD5N50	FDD5N50TM_WS	D-PAK	380mm	16mm	2500
FDD5N50	FDD5N50TF	D-PAK	380mm	16mm	2000

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.6	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 400V$, $T_C = 125^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V$, $V_{DS} = 0V$	-	-	±100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 2A$	-	1.15	1.4	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20V$, $I_D = 2A$	-	4.3	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	480	640	pF
C_{oss}	Output Capacitance		-	66	88	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400V$, $I_D = 5A$ $V_{GS} = 10V$ (Note 4)	-	11	15	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	5	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V$, $I_D = 5A$ $R_G = 25\Omega$ (Note 4)	-	13	36	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	28	66	ns
t_f	Turn-Off Fall Time		-	20	50	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	16	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 4A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 5A$ $dI_F/dt = 100A/\mu s$	-	300	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.8	-	μC

Notes:

1: Repetitive Rating: Pulse width limited by maximum junction temperature

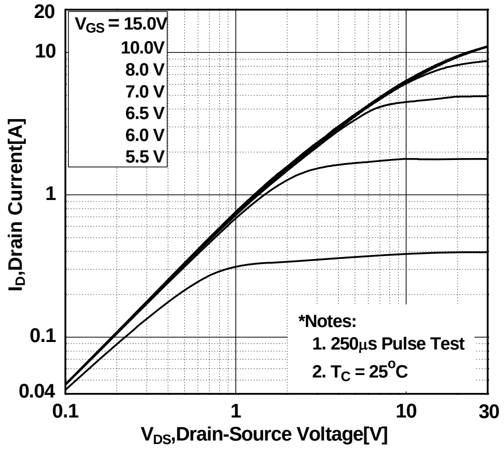
2: $L = 32mH$, $I_{AS} = 4A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$

3: $I_{SD} \leq 4A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$

4: Essentially Independent of Operating Temperature Typical Characteristics

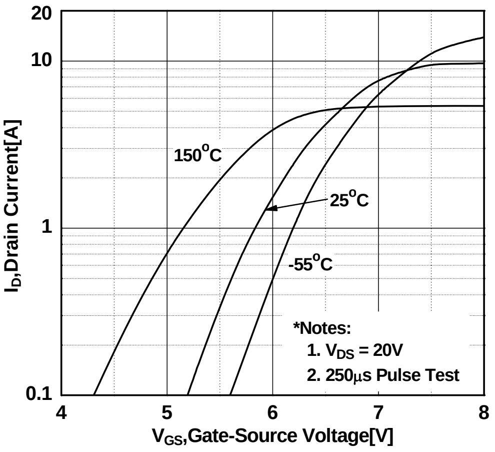
Typical Performance Characteristics

Figure 1. On-Region Characteristics



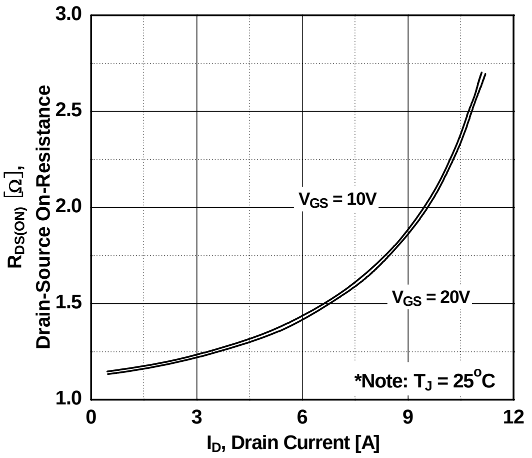
*Notes:
1. 250μs Pulse Test
2. T_C = 25°C

Figure 2. Transfer Characteristics



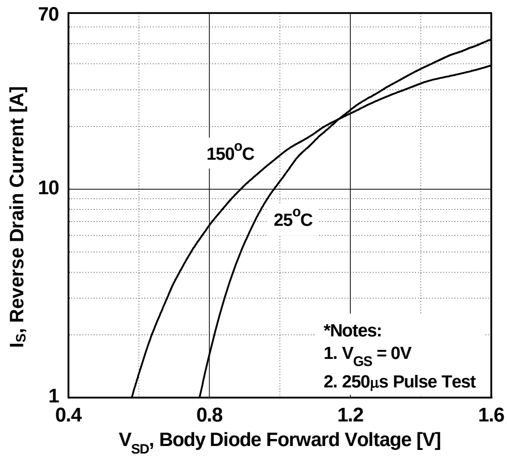
*Notes:
1. V_{DS} = 20V
2. 250μs Pulse Test

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage



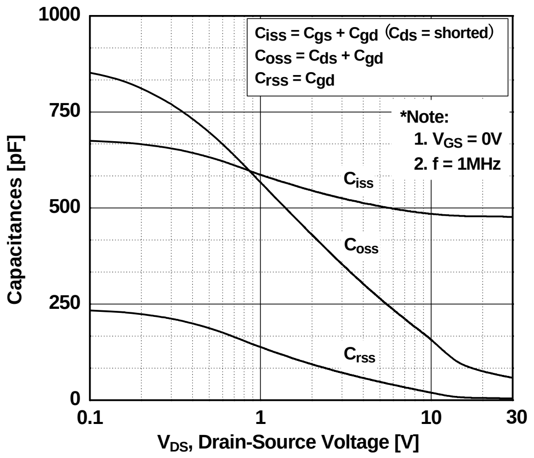
*Note: T_J = 25°C

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



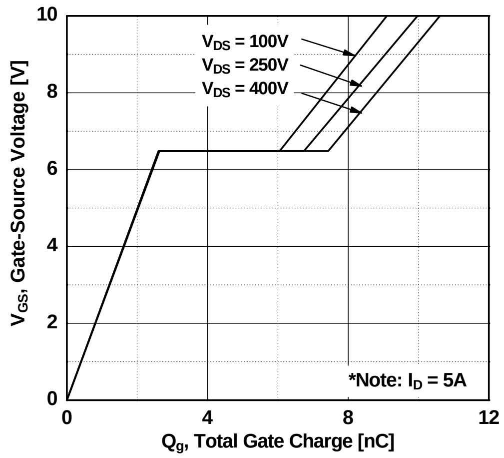
*Notes:
1. V_{GS} = 0V
2. 250μs Pulse Test

Figure 5. Capacitance Characteristics



*Note:
1. V_{GS} = 0V
2. f = 1MHz

Figure 6. Gate Charge Characteristics



*Note: I_D = 5A

Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

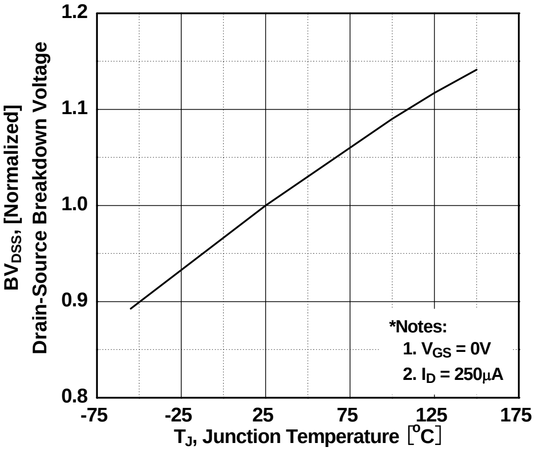


Figure 8. On-Resistance Variation vs. Temperature

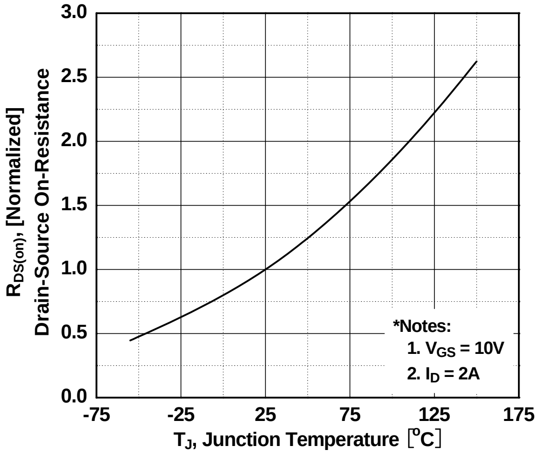


Figure 9. Maximum Safe Operating Area

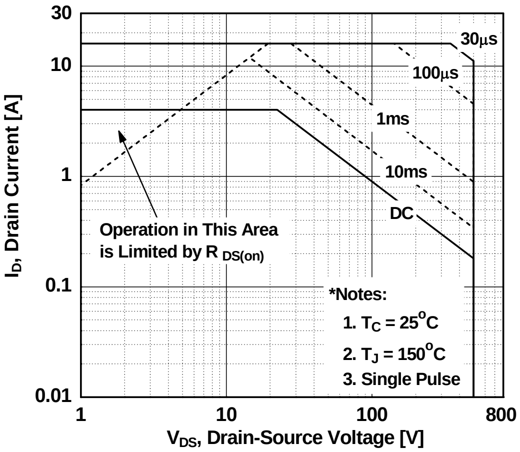


Figure 10. Maximum Drain Current vs. Case Temperature

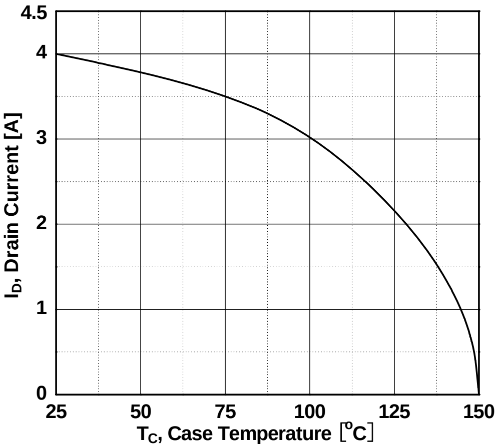
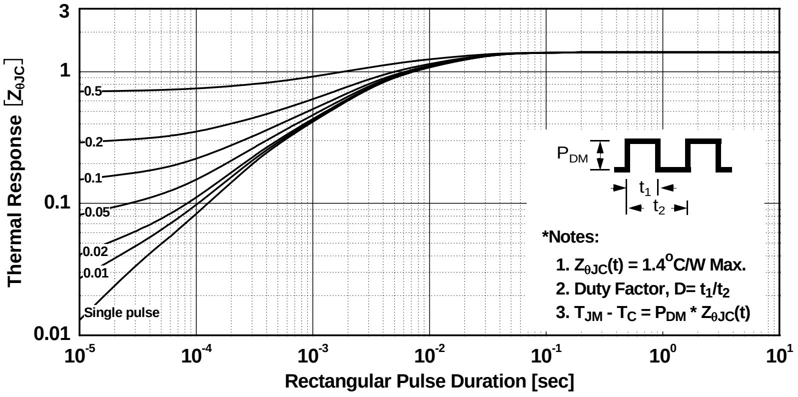
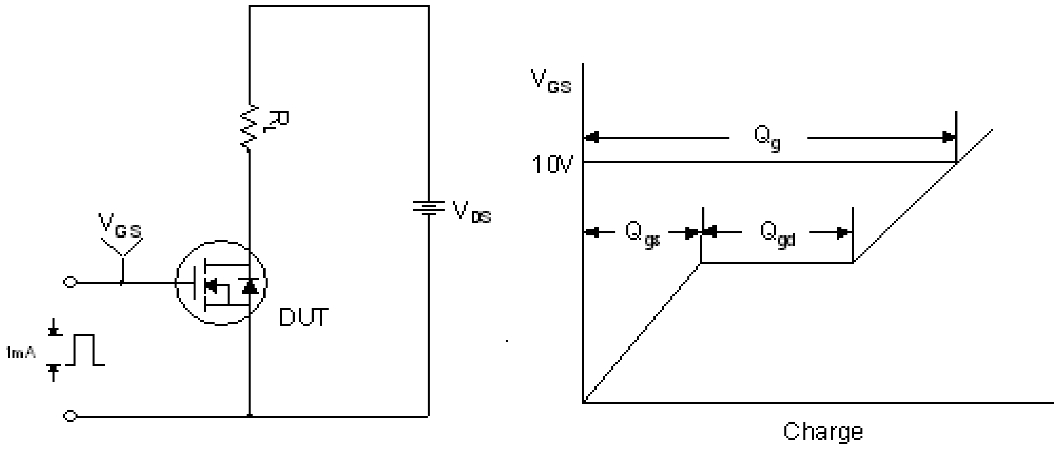


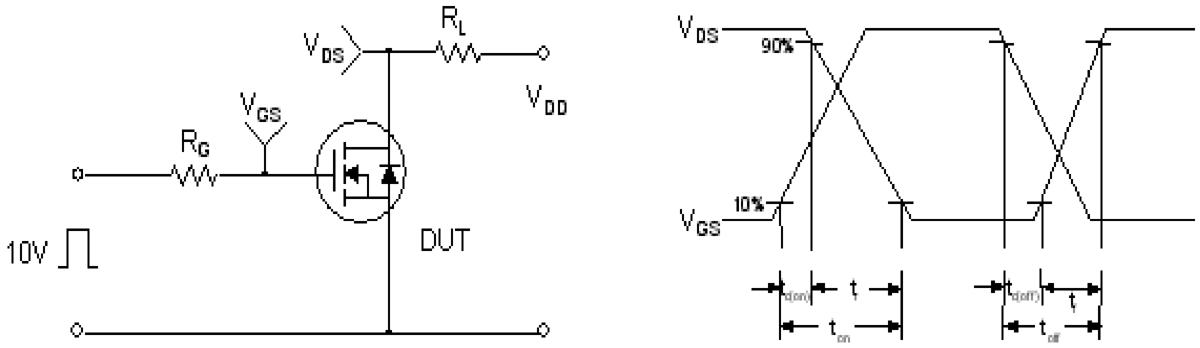
Figure 11. Transient Thermal Response Curve



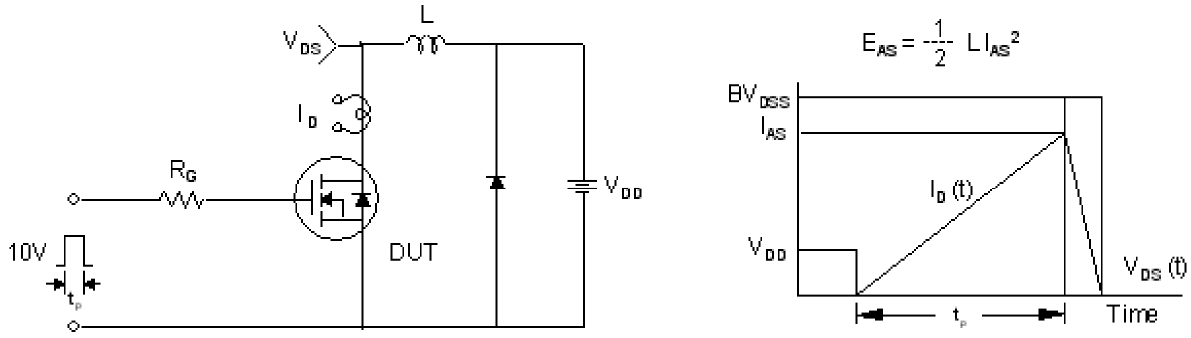
Gate Charge Test Circuit & Waveform



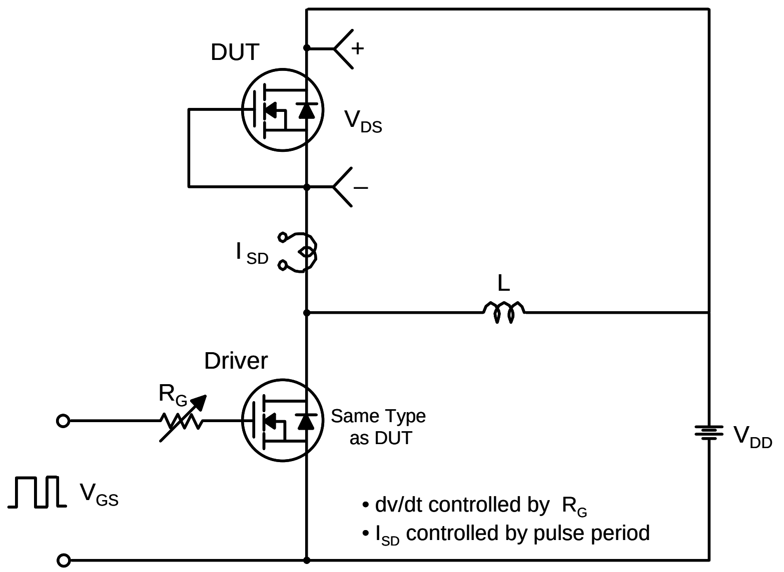
Resistive Switching Test Circuit & Waveforms

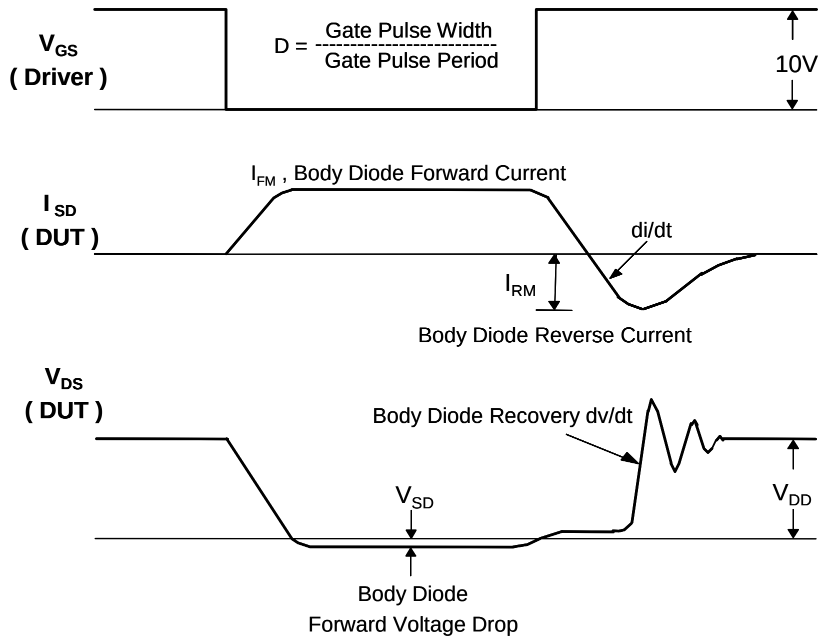


Unclamped Inductive Switching Test Circuit & Waveforms



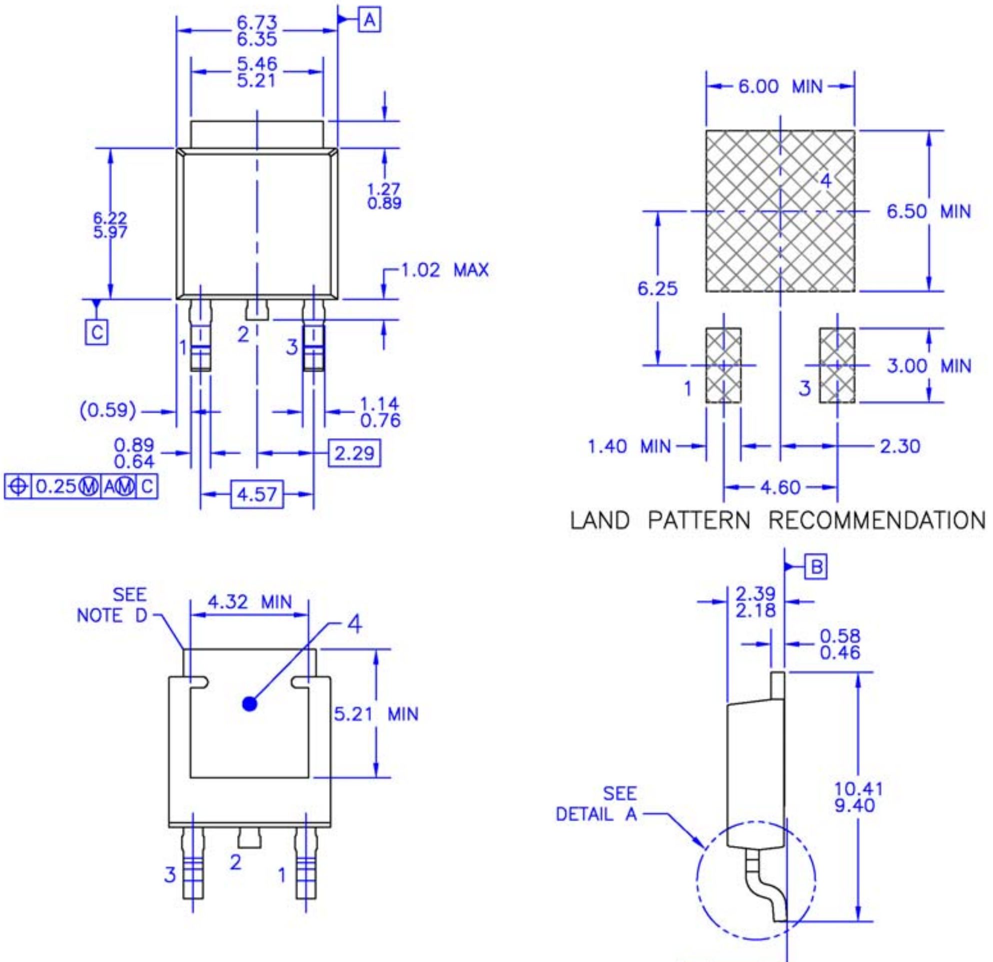
Peak Diode Recovery dv/dt Test Circuit & Waveforms





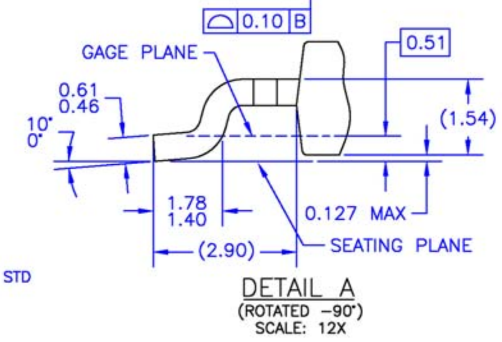
Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8



Dimensions in Millimeters