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DS36C279 Low Power EIA-RS-485 Transceiver with Sleep Mode

Check for Samples: DS36C279

FEATURES

- **100% RS-485 Compliant**
  - **Specified RS-485 Device Interoperation**
- **Low Power CMOS Design: I_{CC} 500 µA Max**
- **Automatic Sensing Sleep Mode**
  - **Reduces I_{CC} to 10 µA Maximum**
- **Built-in Power Up/Down Glitch-Free Circuitry**
  - **Permits Live Transceiver Intersection/Displacement**
- **SOIC Packages**
- **Industrial Temperature Range: −40°C to +85°C**
- **On-Board Thermal Shutdown Circuitry**
  - **Prevents Damage to the Device in the Event of Excessive Power Dissipation**
- **Wide Common Mode Range: −7V to +12V**
- **Receive Open Input Fail-Safe(1)**
- **¼ Unit Load (DS36C279): ≥ 128 Nodes**
- **½ Unit Load (DS36C279T): ≥ 64 Nodes**
- **ESD (Human Body Model): ≥ 2 kV**
- **Drop-In Replacement for:**
  - **LTC485 MAX485 DS75176 DS3695**

(1) Non-terminated, open input only

DESCRIPTION

The DS36C279 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition it is compatible with TIA/EIA-422-B.

The sleep mode feature automatically puts the device in a power saving mode when both the driver and receiver are disabled.(2) The device is ideal for use in power conscious applications where the device may be disabled for extended periods of time.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into a high impedance state.

The receiver incorporates a fail safe circuit which ensures a high output state when the inputs are left open.(3)

The DS36C279T is fully specified over the industrial temperature range (−40°C to +85°C).

(2) Device enters sleep mode if enable conditions are held > 600 ns

(3) Non-terminated, open input only

Connection and Logic Diagram

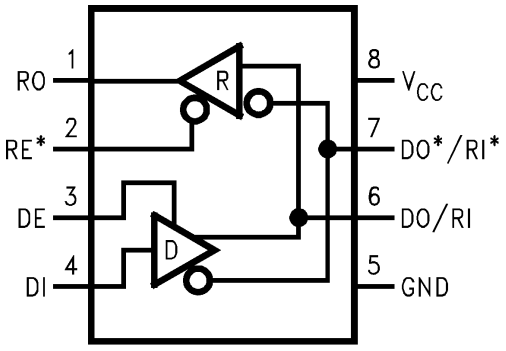

Figure 1. See Package Number D

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TRUTH TABLE

DRIVER SECTION				
RE*	**DE**	**DI**	**DO/RI**	**DO*/RI***
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE*	**DE**	**RI-RI***		**RO**
L	L	≥+0.2V		H
L	L	≤−0.2V		L
H	L	X		Z (1)
L	L	OPEN (2)		H

(1) Device enters sleep mode if enable conditions are held > 600 ns
(2) Non-terminated, open input only

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})		+12V
Input Voltage (DE, RE*, & DI)		−0.5V to (V_{CC} +0.5V)
Common Mode (V_{CM})	Driver Output/Receiver Input	±15V
Input Voltage (DO/RI, DO*/RI*)		±14V
Receiver Output Voltage		−0.5V to (V_{CC} +0.5V)
Maximum Package Power Dissipation	@ +25°C	
	D Package 1190 mW, derate	9.5 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature	(Soldering 4 sec)	+260°C

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

		Min	Typ	Max	Units
Supply Voltage (V_{CC})		+4.75	+5.0	+5.25	V
Bus Voltage		−7		+12	V
Operating Free Air Temperature (T_A)	DS36C279T	−40	+25	+85	°C
	DS36C279	0	+25	+70	°C

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ELECTRICAL CHARACTERISTICS[1][2]

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Reference		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS									
V_{OD1}	Differential Output Voltage	I_O = 0 mA (No Load)		(422) (485)		1.5		5.0	V
V_{OD0}	Output Voltage	I_O = 0 mA (Output to GND)				0		5.0	V
V_{OD0*}	Output Voltage					0		5.0	V
V_{OD2}	Differential Output Voltage (Termination Load)	R_L = 50Ω		(422)	See Figure 2	2.0	2.8		V
		R_L = 27Ω		(485)		1.5	2.3	5.0	V
ΔV_{OD2}	Balance of V_{OD2} $\lvert V_{OD2} - V_{OD2*}\rvert$	R_L = 27Ω or 50Ω		See[3] (422, 485)		−0.2	0.1	+0.2	V
V_{OD3}	Differential Output Voltage (Full Load)	R1 = 54Ω, R2 = 375Ω V_{TEST} = −7V to +12V		See Figure 3		1.5	2.0	5.0	V
V_{OC}	Driver Common Mode Output Voltage	R_L = 27Ω		(485)	See Figure 2	0		3.0	V
		R_L = 50Ω		(422)		0		3.0	V
ΔV_{OC}	Balance of V_{OC} $\lvert V_{OC} - V_{OC*}\rvert$	R_L = 27Ω or R_L = 50Ω		See[3] (422, 485)		−0.2		+0.2	V
I_{OSD}	Driver Output Short-Circuit Current	V_O = +12V		(485) See Figure 5			200	+250	mA
		V_O = −7V		(485)			−190	−250	mA
RECEIVER CHARACTERISTICS									
V_{TH}	Differential Input High Threshold Voltage	$V_O = V_{OH}$, I_O = −0.4 mA −7V ≤ V_{CM} ≤ +12V		See[4] (422, 485)			+0.035	+0.2	V
V_{TL}	Differential Input Low Threshold Voltage	$V_O = V_{OL}$, I_O = 0.4 mA −7V ≤ V_{CM} ≤ +12V				−0.2	−0.035		V
V_{HST}	Hysteresis	V_{CM} = 0V		See[5]			70		mV
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V	DS36C279T			24	68		kΩ
			DS36C279			48	68		kΩ
I_{IN}	Line Input Current See[6]	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}, V_{CC} = 4.75 to 5.25 or 0V	DS36C279	V_{IN} = +12V		0	0.19	0.25	mA
				V_{IN} = −7V		0	−0.1	−0.2	mA
			DS36C279T	V_{IN} = +12V		0	0.19	0.5	mA
				V_{IN} = −7V		0	−0.1	−0.4	mA
I_{ING}	Line Input Current Glitch See[6]	Other Input = 0V, DE = V_{IL}, RE* = V_{IL},	DS36C279	V_{IN} = +12V		0	0.19	0.25	mA
				V_{IN} = −7V		0	−0.1	−0.2	mA
		V_{CC} = +3.0V or 0V, T_A = 25°C	DS36C279T	V_{IN} = +12V		0	0.19	0.5	mA
				V_{IN} = −7V		0	−0.1	−0.4	mA
I_B	Input Balance Test	RS = 500Ω		(422) See[7]				±400	mV
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA, V_{ID} = +0.2V		RO See Figure 12		3.5	4.6		V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA, V_{ID} = −0.2V					0.3	0.5	V
I_{OSR}	Short Circuit Current	V_O = GND		RO		7	35	85	mA
I_{OZR}	TRI-STATE Leakage Current	V_O = 0.4V to 2.4V						±1	µA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD1} and V_{OD2}.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.
(3) Delta $\lvert V_{OD2}\rvert$ and Delta $\lvert V_{OC}\rvert$ are changes in magnitude of V_{OD2} and V_{OC} , respectively, that occur when input changes state.
(4) Threshold parameter limits specified as an algebraic value rather than by magnitude.
(5) Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.
(6) I_{IN} includes the receiver input current and driver TRI-STATE leakage current.
(7) For complete details of test, see RS-485.

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ELECTRICAL CHARACTERISTICS[1][2] (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Reference	Min	Typ	Max	Units
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE, RE*, DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$					2	µA
I_{IL}	Low Level Input Current	V_{CC} = 5V	V_{IL} = 0V				−2	µA
		V_{CC} = +3.0V					−2	µA
I_{CC}	Power Supply Current (No Load)	Driver and Receiver ON		V_{CC}		200	500	µA
I_{CCR}		Driver OFF, Receiver ON				200	500	µA
I_{CCD}		Driver ON, Receiver OFF				200	500	µA
I_{CCX}		Sleep Mode				0.2	10	µA

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SWITCHING CHARACTERISTICS(1)(2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 54Ω, C_L = 100 pF	See Figure 6 and Figure 7	10	39	80	ns
t_{PLHD}	Differential Propagation Delay Low to High			10	40	80	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$			0	1	10	ns
t_r	Rise Time			3	25	50	ns
t_f	Fall Time			3	25	50	ns
t_{PHZ}	Disable Time High to Z	C_L = 15 pF RE* = L	See Figure 8 and Figure 9		80	200	ns
t_{PLZ}	Disable Time Low to Z		See Figure 10 and Figure 11		80	200	ns
t_{PZH}	Enable Time Z to High	C_L = 100 pF RE* = L	See Figure 8 and Figure 9		50	200	ns
t_{PZL}	Enable Time Z to Low		See Figure 10 and Figure 11		65	200	ns
t_{PSH}	Driver Enable from Sleep Mode to Output High	C_L = 100 pF See(3)	See Figure 8 and Figure 9	70	98	250	ns
t_{PSL}	Driver Enble from Sleep Mode to Output Low	C_L = 100 pF See(3)	See Figure 10 and Figure 11	70	98	250	ns
RECEIVER CHARACTERISTICS							
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF	See Figure 13 and Figure 14	30	210	400	ns
t_{PLH}	Propagation Delay Low to High			30	190	400	ns
t_{SK}	Skew, $\|t_{PHL} - t_{PLH}\|$			0	20	50	ns
t_{PLZ}	Output Disable Time	C_L = 15 pF DE = H	See Figure 15, Figure 16 and Figure 17		50	150	ns
t_{PHZ}					55	150	ns
t_{PZL}	Output Enable Time				40	150	ns
t_{PZH}					45	150	ns
t_{PSH}	Receiver Enable from Sleep Mode to Output High	C_L = 15 pF See(3)	See Figure 15 and Figure 17	70	97	250	ns
t_{PSL}	Receiver Enable from Sleep Mode to Output Low	C_L = 15 pF See(3)	See Figure 15 and Figure 16	70	95	250	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.
(2) C_L includes probe and jig capacitance.
(3) For enable from sleep mode delays DE = L and RE* = H for greater than 600 ns prior to test (device is in sleep mode).

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PARAMETER MEASUREMENT INFORMATION

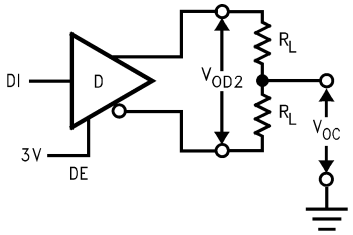

Figure 2. Driver V_{OD2} and V_{OC}

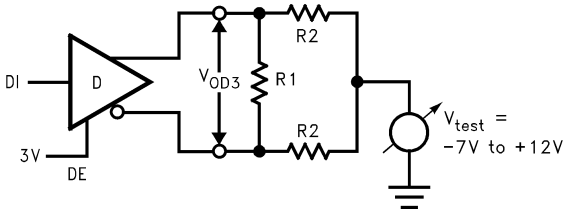

Figure 3. Driver V_{OD3}

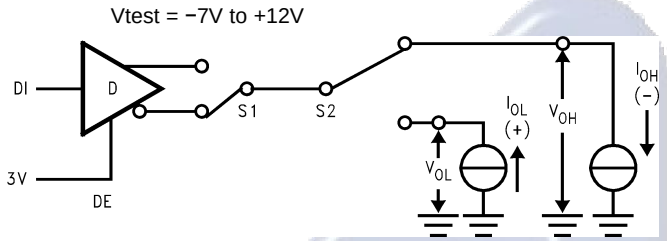

Figure 4. Driver V_{OH} and V_{OL}

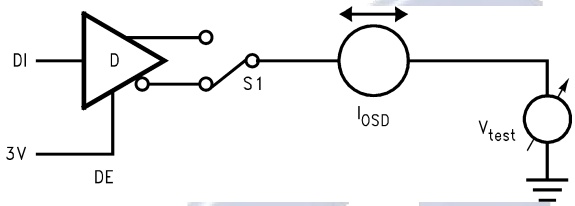

Figure 5. Driver I_{OSD}

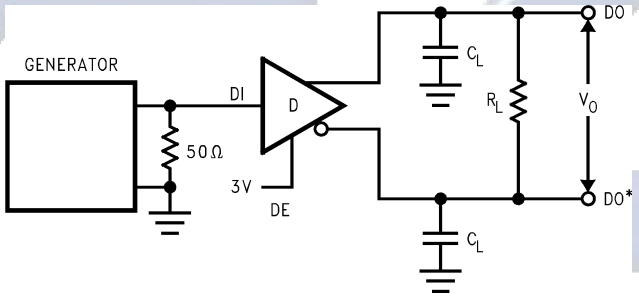

Figure 6. Driver Differential Propagation Delay Test Circuit

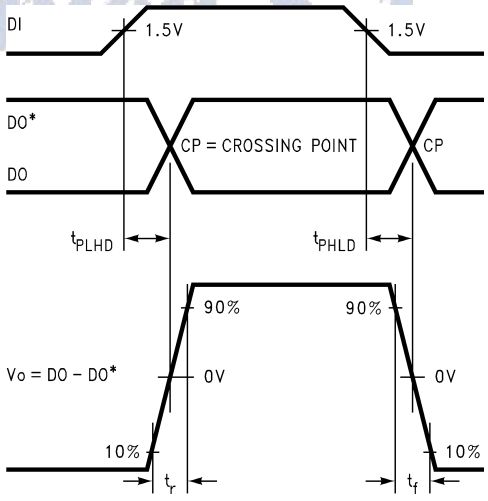

Figure 7. Driver Differential Propagation Delays and Differential Rise and Fall Times

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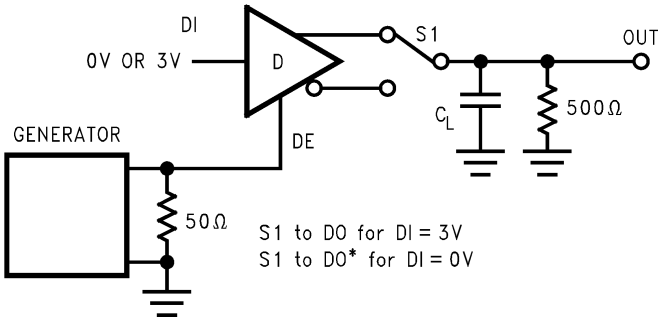

Figure 8. TRI-STATE and Sleep Mode Test Circuit (t_{PZH}, (t_{PSH}), t_{PHZ})

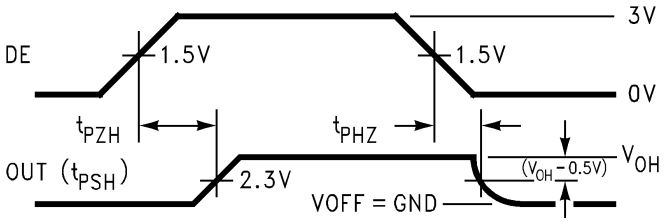

Figure 9. TRI-STATE and Sleep Mode Waveforms (t_{PZH}, (t_{PSH}), t_{PHZ})

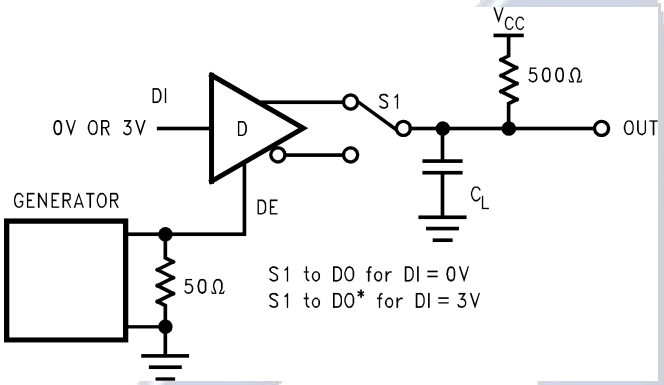

Figure 10. TRI-STATE and Sleep Mode Test Circuit (t_{PZL}, (t_{PSL}), t_{PLZ})

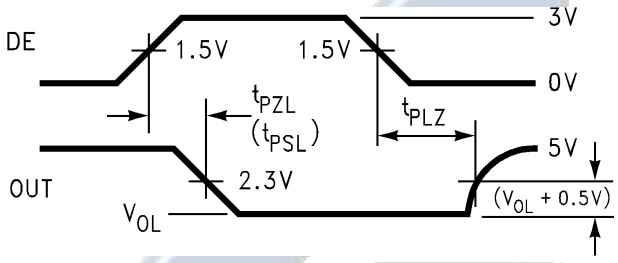

Figure 11. TRI-STATE and Sleep Mode Waveforms (t_{PZL}, (t_{PSL}), t_{PLZ})

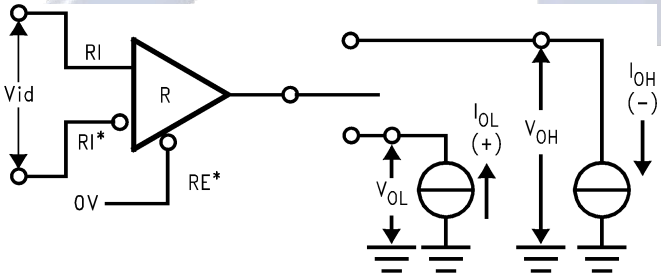

Figure 12. Receiver V_{OH} and V_{OL}

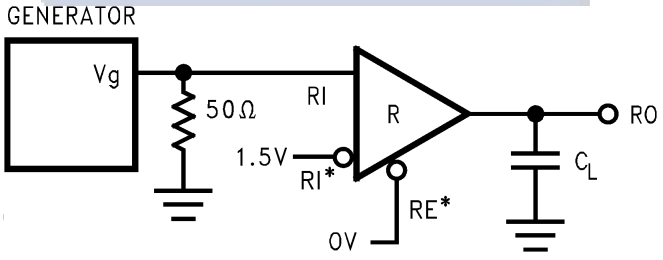

Figure 13. Receiver Differential Propagation Delay Test Circuit

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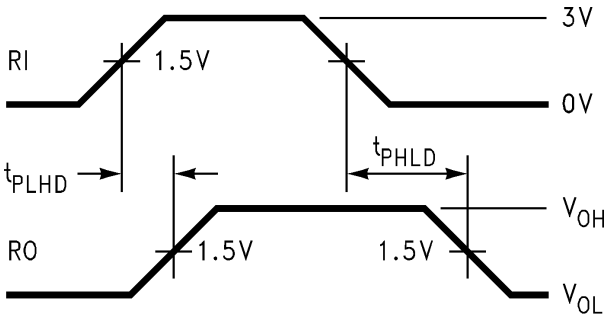

Figure 14. Receiver Differential Propagation Delay Waveforms

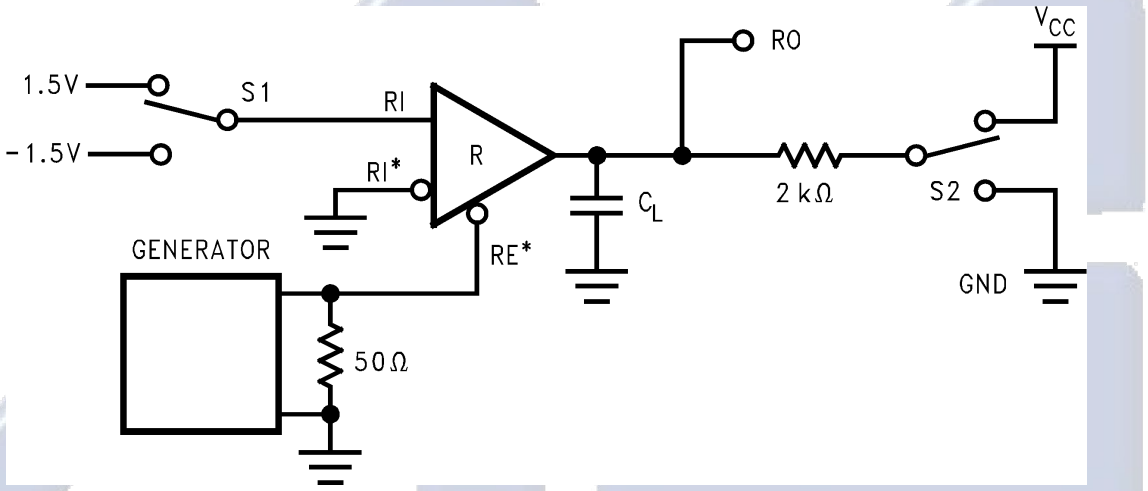

Figure 15. Receiver TRI-STATE and Sleep Mode Test Circuit

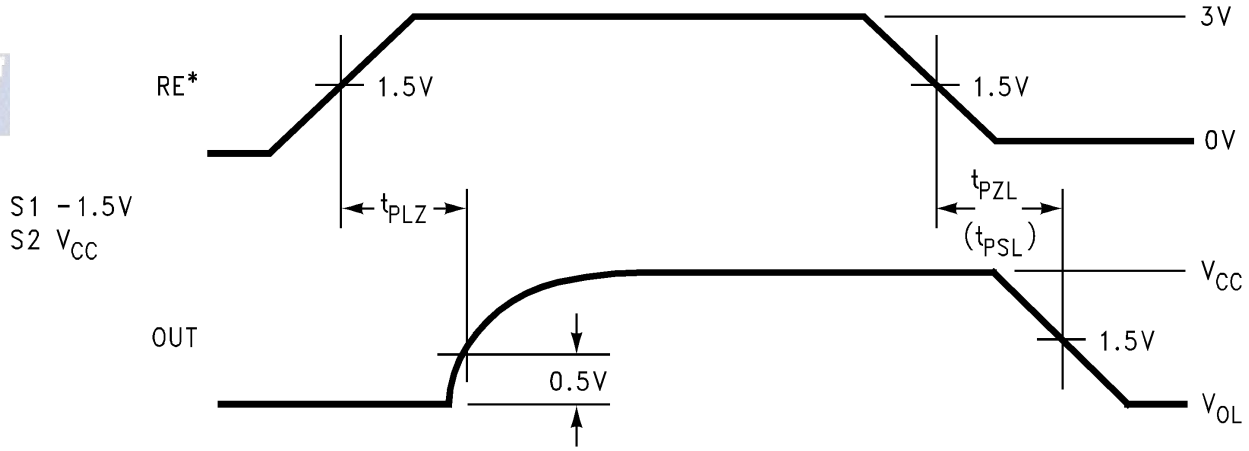

Figure 16. Receiver Enable and Disable Waveforms (t_{PLZ}, t_{PZL}, (t_{PSL}))

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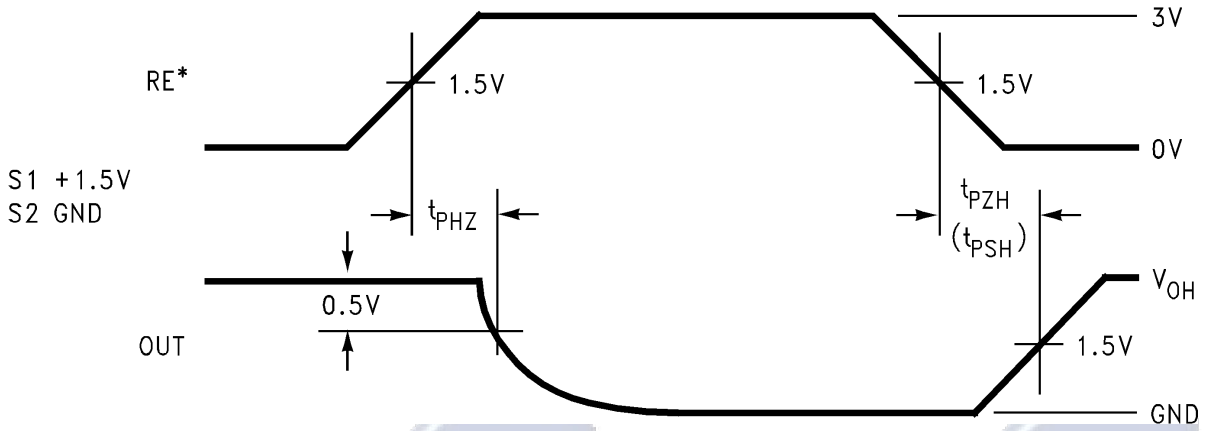

Figure 17. Receiver Enable and Disable Waveforms (t_{PHZ}, t_{PZH}, (t_{PSH}))

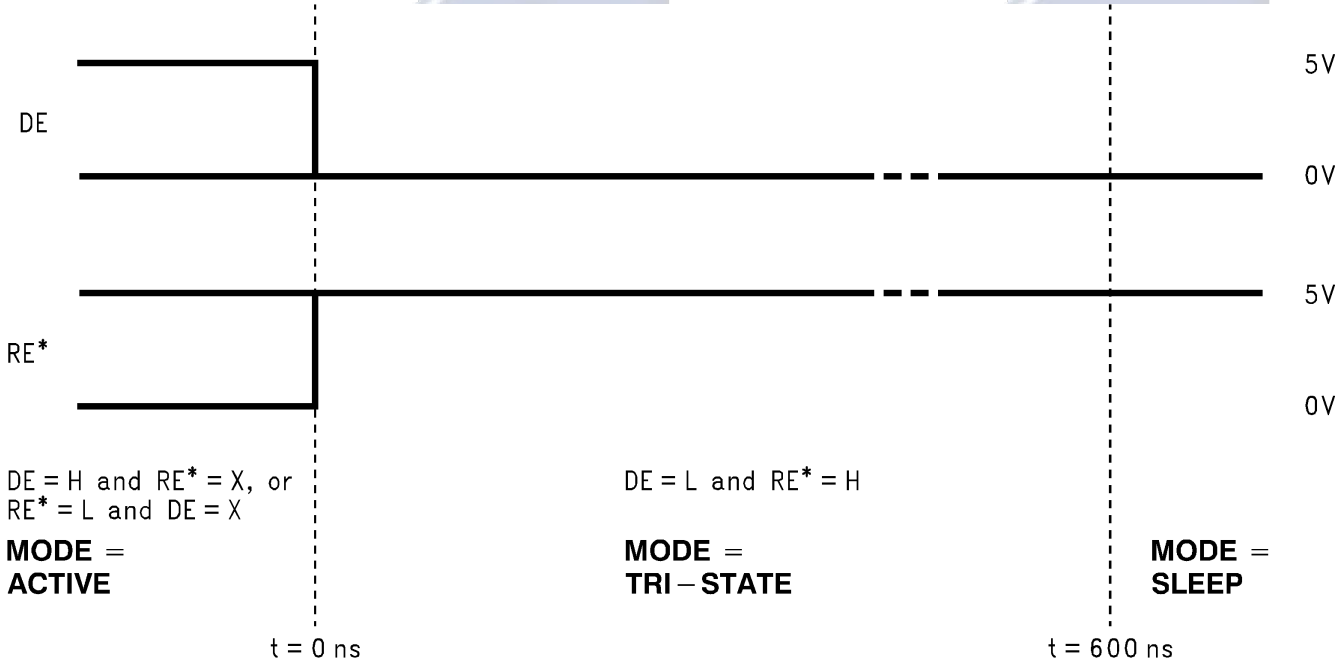

Figure 18. Entering Sleep Mode Conditions

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TYPICAL APPLICATION INFORMATION

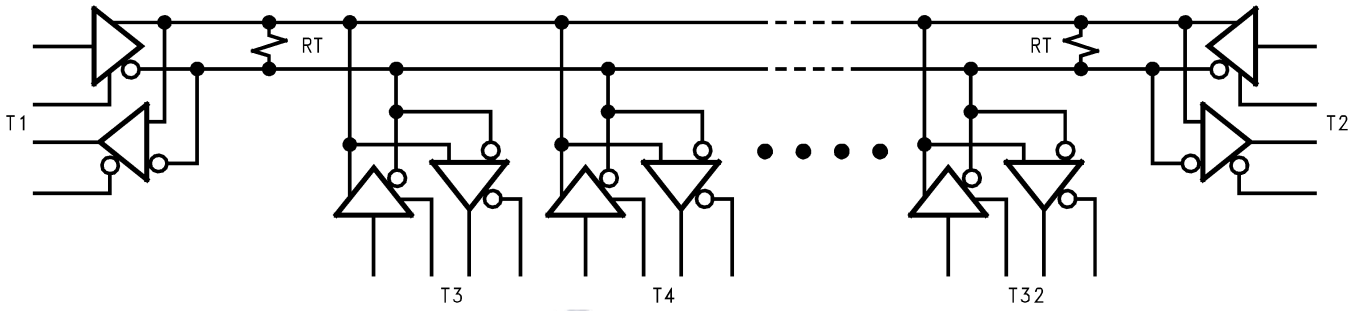

Figure 19. Typical RS-485 Bus Interface

Table 1. DEVICE PIN DESCRIPTIONS

Pin No.	Name	Description
1	RO	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI ≥ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI ≤ DO*/RI* by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
2	RE*	Receiver Output Enable: When RE* is LOW the receiver output is enabled. When RE* is HIGH, the receiver output is in TRI-STATE (OFF). When RE* is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
3	DE	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). When RE* is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
4	DI	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection.
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO*/RI*	Driver Output/Receiver Input, 485 Bus Pin.
8	V_{CC}	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.75V to +5.25V.

UNIT LOAD

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see Figure 20). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes. For example, an aircraft that has 32 rows with 4 seats per row would benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS36C278, the DS36C279, and the DS36C280 all have ½ unit load and ¼ unit load (UL) options available. These devices will allow up to 64 nodes or 128 nodes specified over temperature depending upon which option is selected. The ½ UL option is available in industrial temperature and the ¼ UL is available in commercial temperature.

First, for a ½ UL device the top and bottom borders shown in Figure 20 are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see Figure 20). Second, for a ¼ UL device the top and bottom borders shown in Figure 20 are scaled also. Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see Figure 20).

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The advantage of the ½ UL and ¼ UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS36C278/279/280 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

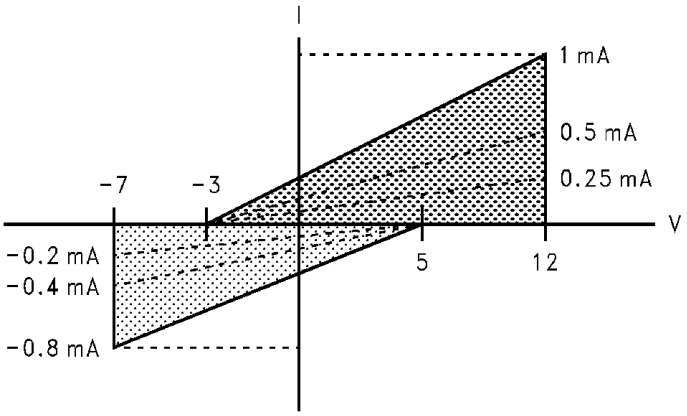

Figure 20. Input Current vs Input Voltage Operating Range

The DS36C279 and DS36C280 have an additional feature which offers more advantages. The DS36C279 has an automatic sleep mode function for power conscious applications. The DS36C280 has a slew rate control for EMI conscious applications. Refer to the sleep mode and slew rate control portion of the application information section in the corresponding datasheet for more information on these features.

SLEEP MODE

The DS36C279 features an automatic shutdown mode that allows the device to save power when not transmitting data. Since the shutdown mode is automatic, no external components are required. It may be used as little or as much as the application requires. The more the feature is utilized, the more power it saves.

The sleep mode is automatically entered when both the driver and receiver are disabled. This occurs when both the DE pin is asserted to a logic low and the RE* pin is asserted to a logic high. Once both pins are asserted the device will enter sleep mode typically in 50 ns. The DS36C279 is ensured to go into sleep mode within 600 ns after both pins are asserted. The device wakes up (comes out of sleep mode) when either the DE pin is asserted to a logic high and/or the RE* pin is asserted to a logic low. After the device enters sleep mode it will take longer for the device to wake up than it does for the device to enable from TRI-STATE. Refer to data specifications t_{PSL} and t_{PSH} and compare with t_{PZL} and t_{PZH} for timing differences.

The benefit of the DS36C279 is definitely its power savings. When active the device has a maximum I_{CC} of 500 µA. When in sleep mode the device has a maximum I_{CC} of only 10 µA, which is 50 times less power than when active. The I_{CC} when the device is active is already very low but when in sleep mode the I_{CC} is ultra low.

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REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGE OPTION ADDENDUM

23-Sep-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS36C279M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	36C27 9M	Samples
DS36C279MX	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	36C27 9M	Samples
DS36C279MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	36C27 9M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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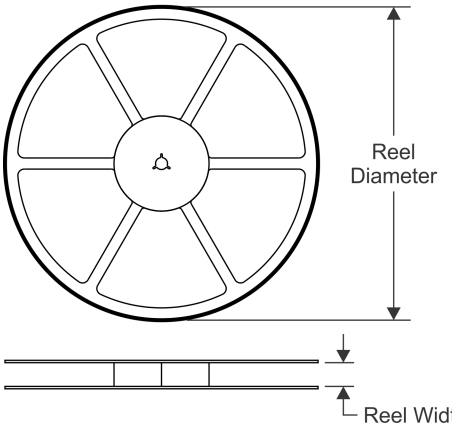
PACKAGE MATERIALS INFORMATION

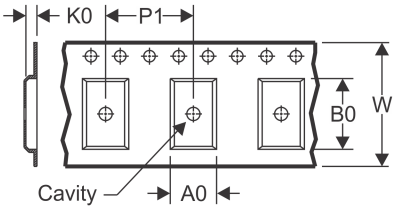
23-Sep-2013

TAPE AND REEL INFORMATION

REEL DIMENSIONS

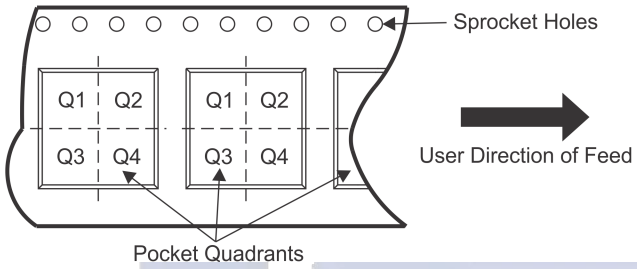


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS36C279MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

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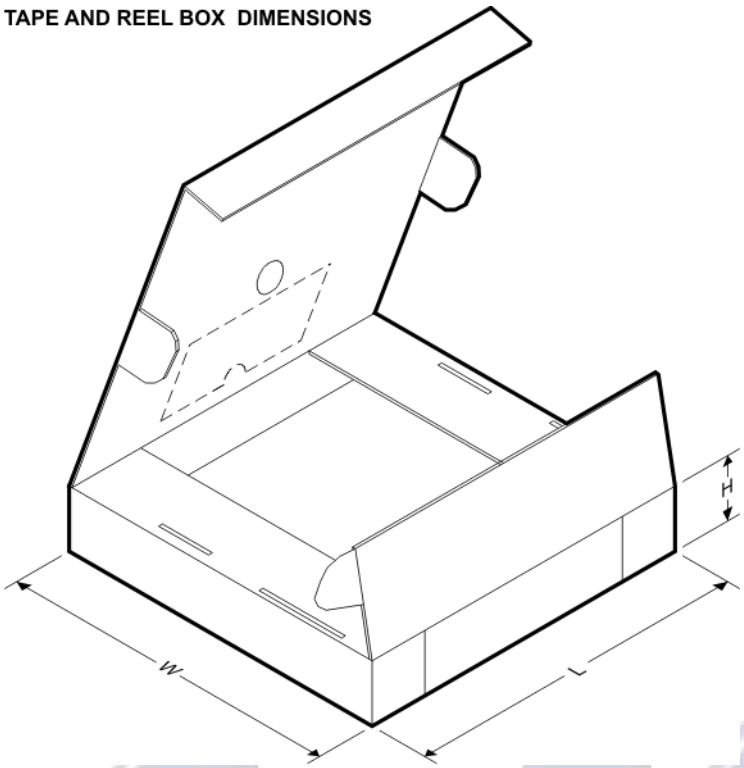
PACKAGE MATERIALS INFORMATION

23-Sep-2013

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS36C279MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

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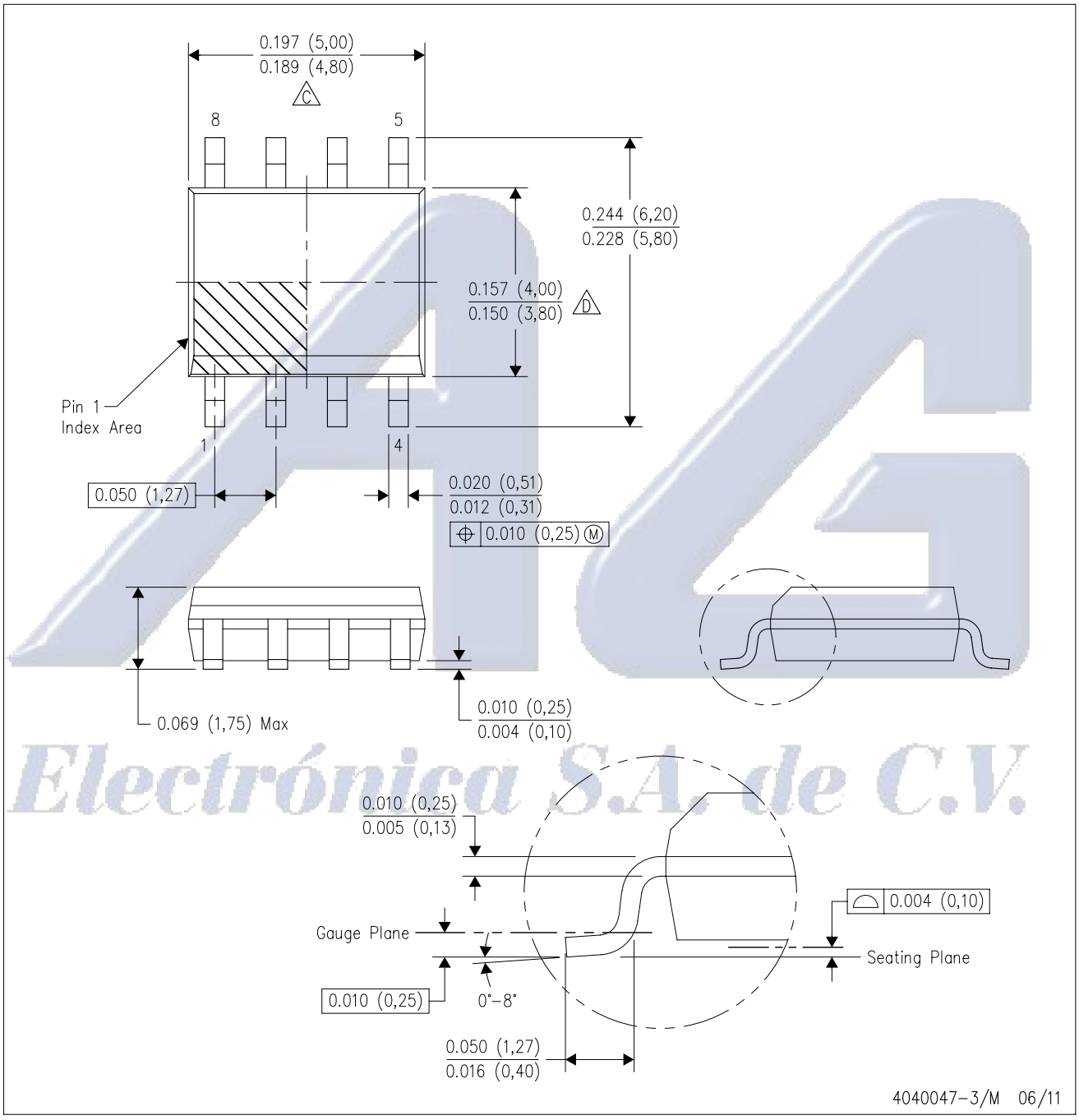
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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