

# FQP13N50C / FQPF13N50C

## N-Channel QFET® MOSFET

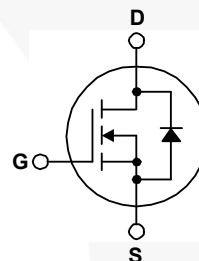
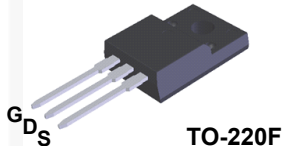
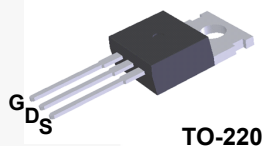
500 V, 13 A, 480 mΩ

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

### Features

- 13 A, 500 V,  $R_{DS(on)} = 480 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 6.5 \text{ A}$
- Low Gate Charge (Typ. 43 nC)
- Low Crss (Typ. 20 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP13N50C	FQPF13N50C	Units
$V_{DSS}$	Drain-Source Voltage	500		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	13	13 *	A
		8	8 *	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	52	52 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	860		mJ
$I_{AR}$	Avalanche Current (Note 1)	13		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	19.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	195	48	W
		1.56	0.39	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FQP13N50C	FQPF13N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.64	2.58	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP13N50C_F105	FQP13N50C	TO-220	Tube	N/A	N/A	50 units
FQPF13N50C_F105	FQPF13N50C	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.5 A	--	0.39	0.48	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 6.5 A	--	15	--	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	1580	2055	pF
C <sub>oss</sub>	Output Capacitance		--	180	235	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	20	25	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 13 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	25	60	ns
t <sub>r</sub>	Turn-On Rise Time		--	100	210	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	130	270	ns
t <sub>f</sub>	Turn-Off Fall Time		--	100	210	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 13 A, V <sub>GS</sub> = 10 V  (Note 4)	--	43	56	nC
Q <sub>gs</sub>	Gate-Source Charge		--	7.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	18.5	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	13	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	52	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 13 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 13 A,	--	410	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs	--	4.5	--	μC

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 6 mH, I<sub>AS</sub> = 13 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 13 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

## Typical Characteristics

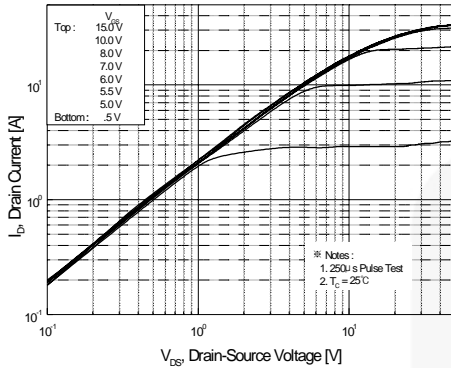


Figure 1. On-Region Characteristics

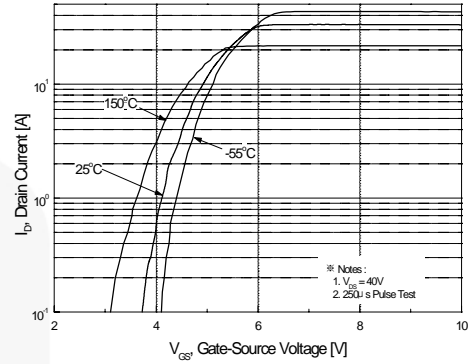


Figure 2. Transfer Characteristics

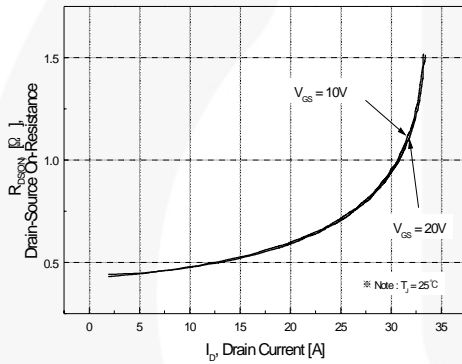


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

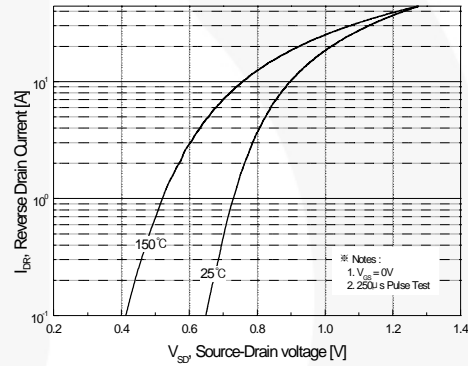


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

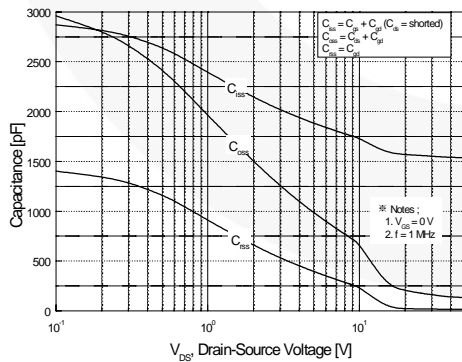


Figure 5. Capacitance Characteristics

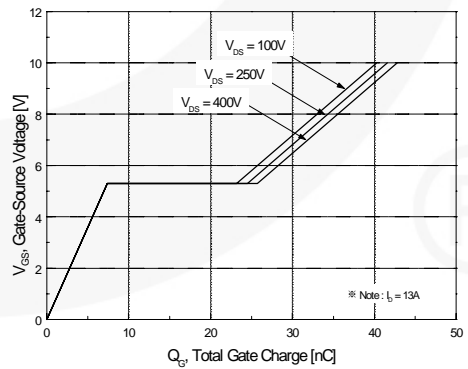
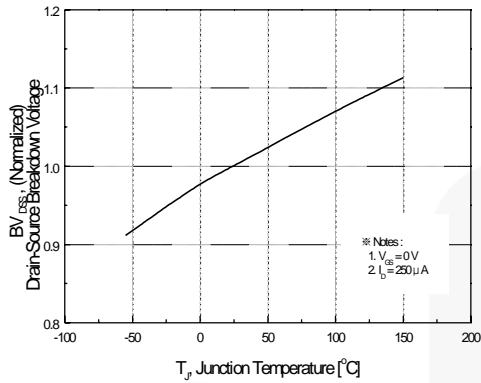
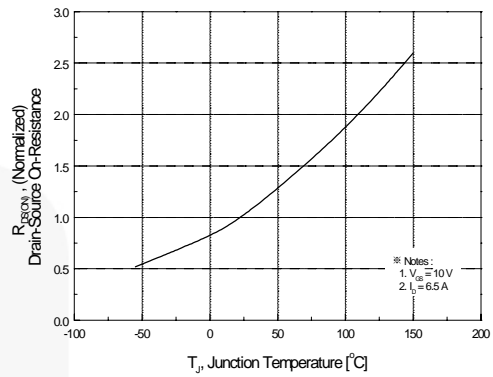


Figure 6. Gate Charge Characteristics

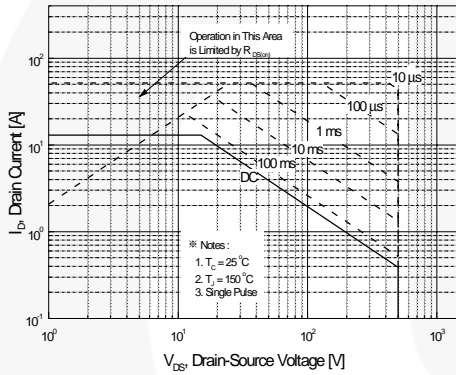
**Typical Characteristics** (continued)



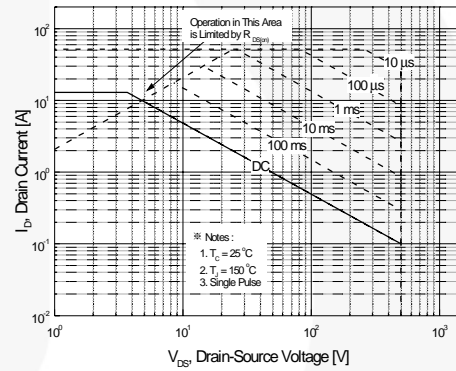
**Figure 7. Breakdown Voltage Variation vs Temperature**



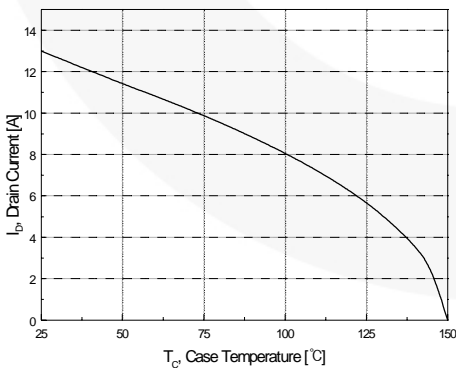
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9-1. Maximum Safe Operating Area for FQP13N50C**



**Figure 9-2. Maximum Safe Operating Area for FQPF13N50C**



**Figure 10. Maximum Drain Current vs Case Temperature**

Typical Characteristics (continued)

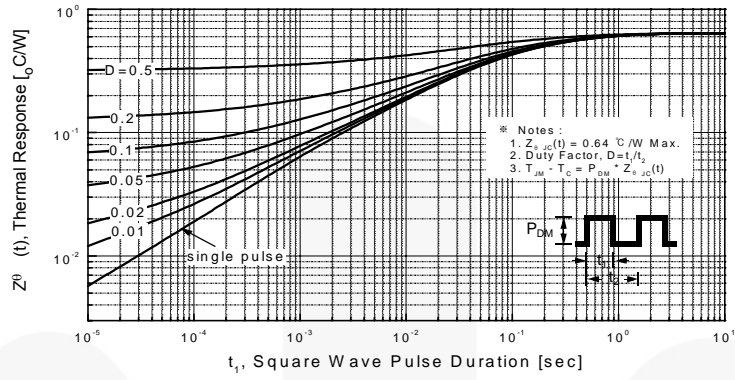


Figure 11-1. Transient Thermal Response Curve for FQP13N50C

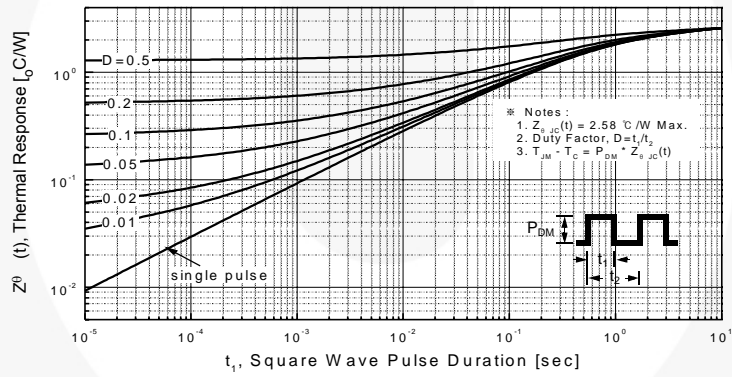


Figure 11-2. Transient Thermal Response Curve for FQPF13N50C



Figure 12. Gate Charge Test Circuit & Waveform

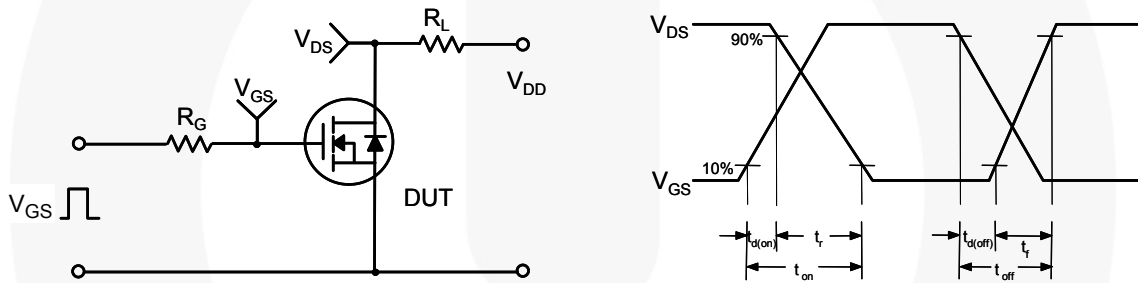


Figure 13. Resistive Switching Test Circuit & Waveforms

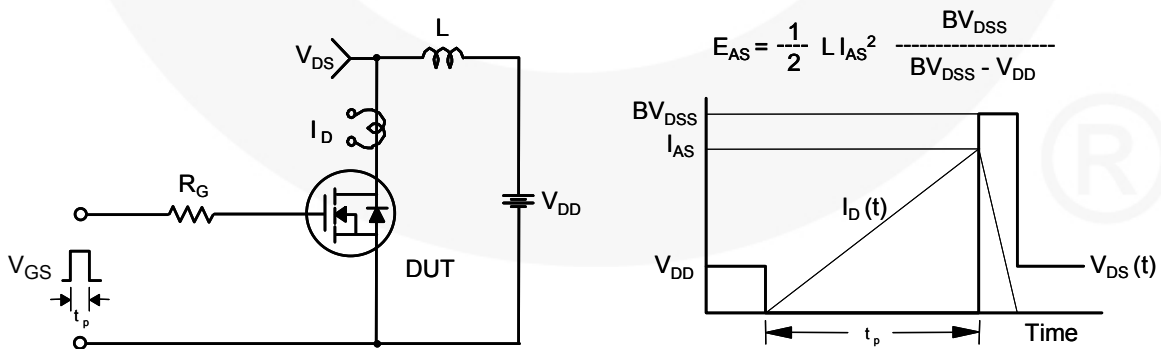


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

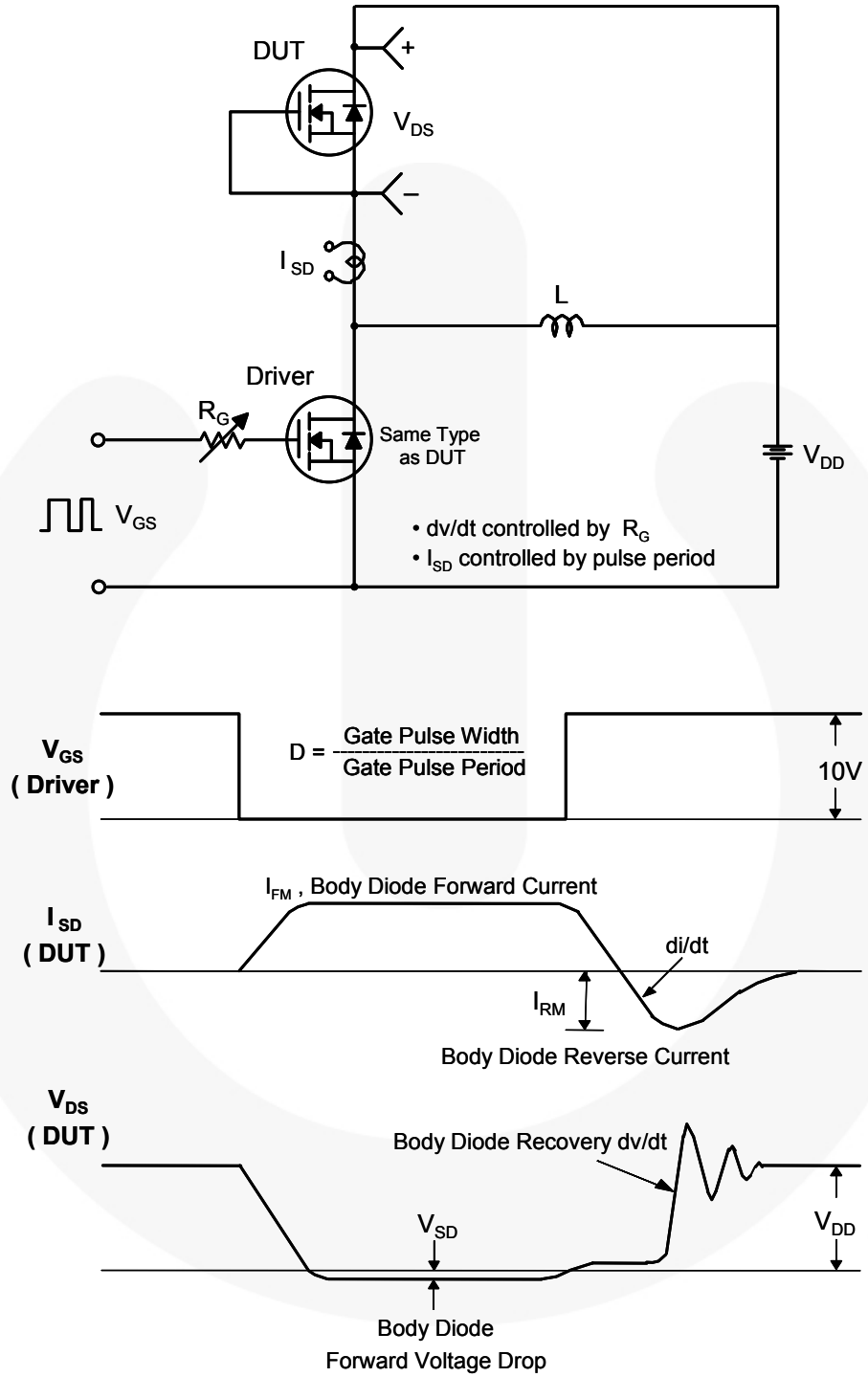
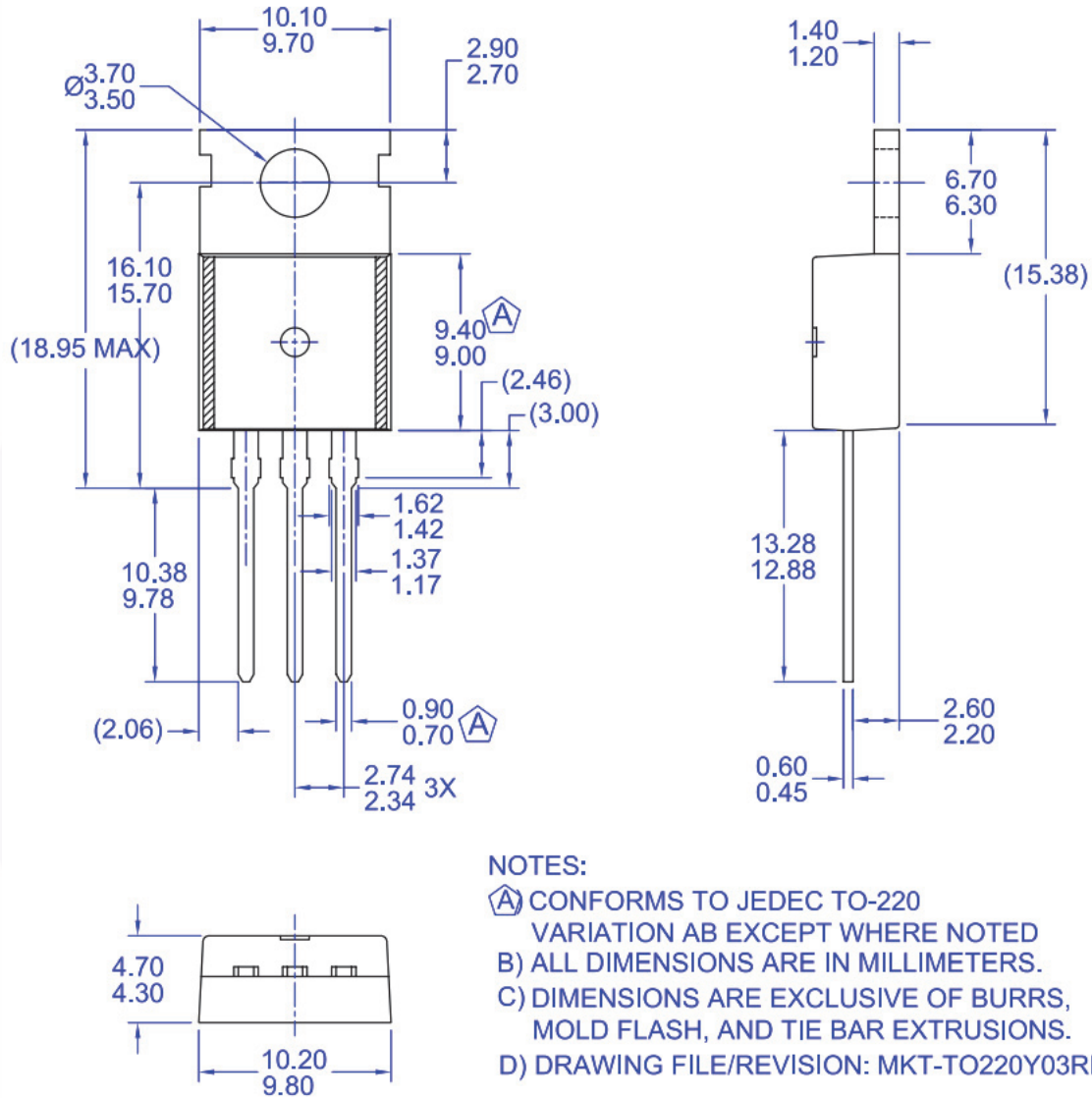


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

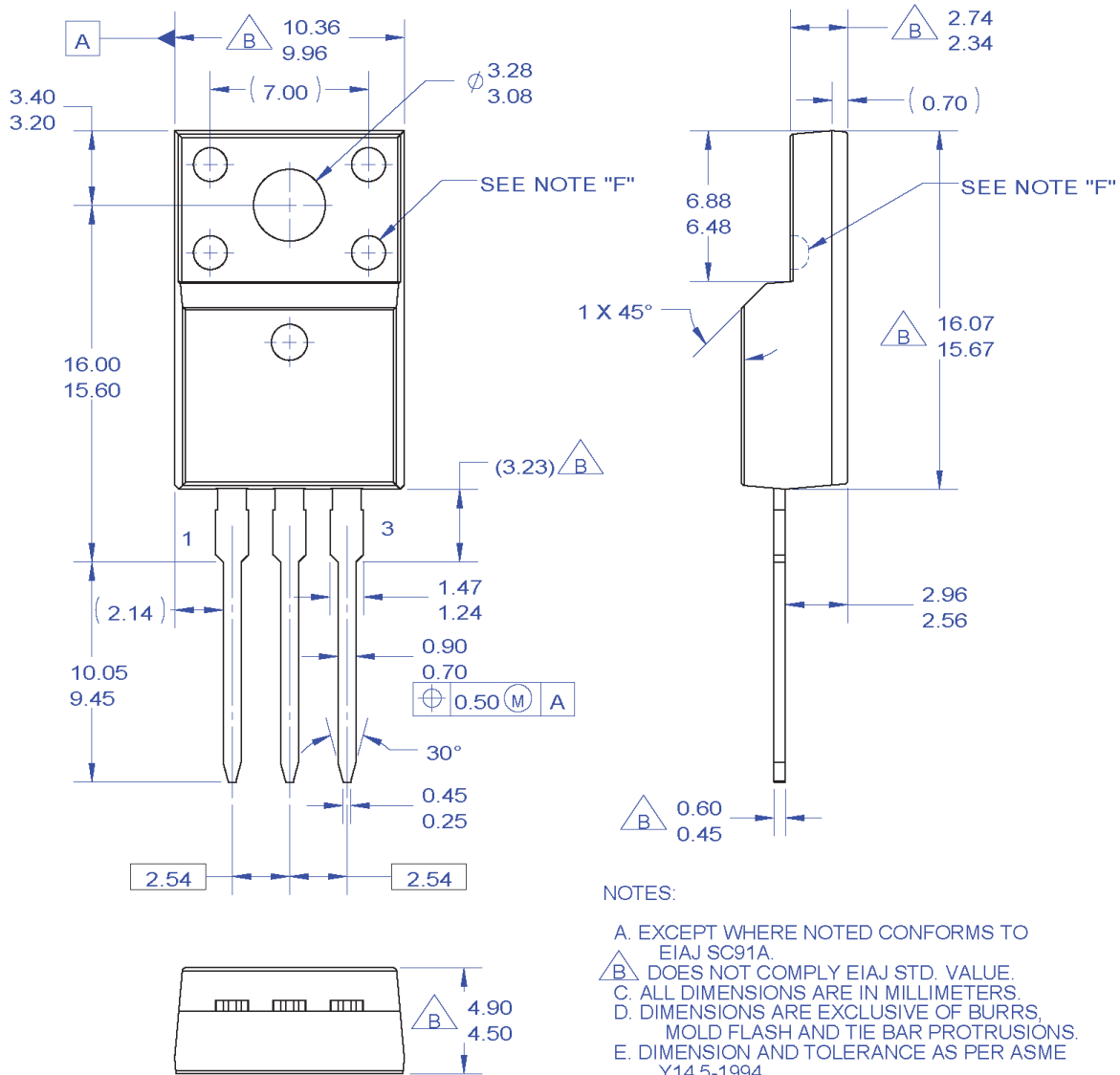
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## Mechanical Dimensions



**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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