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FAIRCHILD SEMICONDUCTOR®

November 2013

FQL40N50

N-Channel QFET® MOSFET

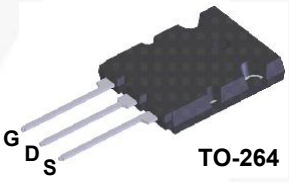
500 V, 40 A, 110 mΩ

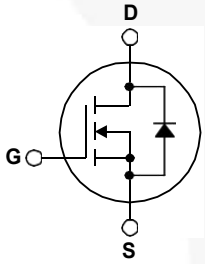
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 40 A, 500 V, $R_{DS(on)}$ = 110 mΛ (Max.) @ V_{GS} = 10 V, I_D = 20 A
- Low Gate Charge (Typ. 155 nC)
- Low Crss (Typ. 95 pF)
- 100% Avalanche Tested





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQL40N50	Unit
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		40	A
	- Continuous (T_C = 100°C)		25	A
I_{DM}	Drain Current - Pulsed	(Note 1)	160	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1780	mJ
I_{AR}	Avalanche Current	(Note 1)	40	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	46	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		460	W
	- Derate above 25°C		3.7	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds.		300	°C

Thermal Characteristics

Symbol	Parameter	FQL40N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.27	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	30	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQL40N50	FQL40N50	TO-264	Tube	N/A	N/A	25 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.48	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 20 A	--	0.085	0.11	Λ
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 20 A	--	29	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	5800	7500	pF
C_{oss}	Output Capacitance		--	880	1150	pF
C_{rss}	Reverse Transfer Capacitance		--	95	120	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 40 A, R_G = 25 Λ (Note 4)	--	140	290	ns
t_r	Turn-On Rise Time		--	440	890	ns
$t_{d(off)}$	Turn-Off Delay Time		--	350	700	ns
t_f	Turn-Off Fall Time		--	250	500	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 40 A, V_{GS} = 10 V (Note 4)	--	155	200	nC
Q_{gs}	Gate-Source Charge		--	37	--	nC
Q_{gd}	Gate-Drain Charge		--	78	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	40	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	160	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 40 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 40 A, dI_F / dt = 100 A/μs	--	520	--	ns
Q_{rr}	Reverse Recovery Charge		--	8.0	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 2.0 mH, I_{AS} = 40 A, V_{DD} = 50 V, R_G = 25 Λ, starting T_J = 25°C.
3. I_{SD} ≤ 40 A, di/dt ≤ 200 A/μs , V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

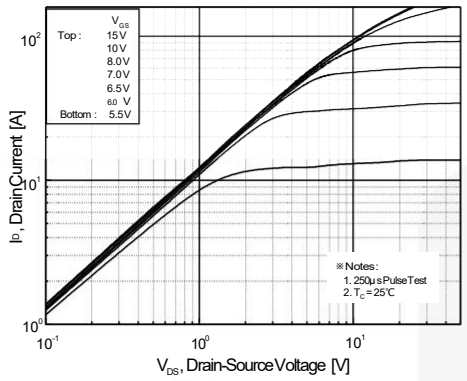


Figure 1. On-Region Characteristics

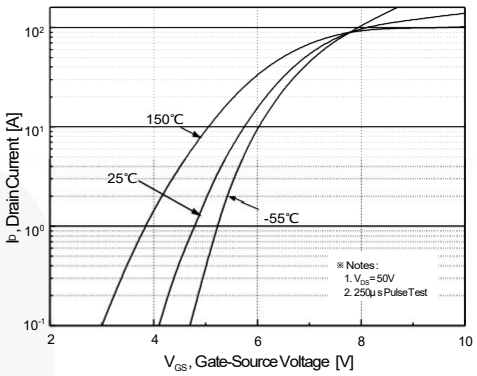


Figure 2. Transfer Characteristics

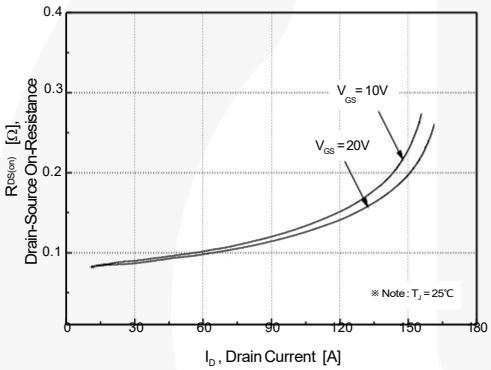


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

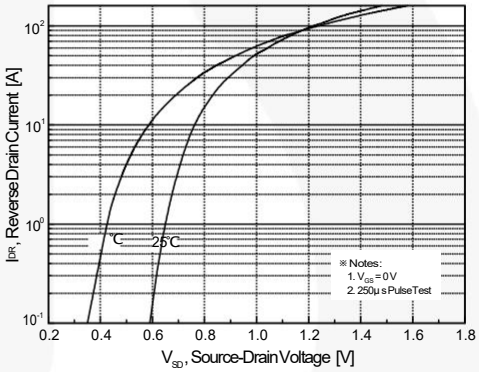


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

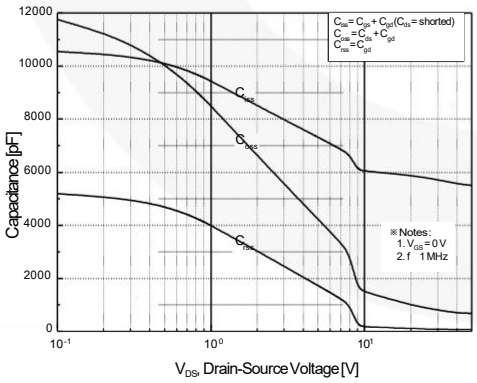


Figure 5. Capacitance Characteristics

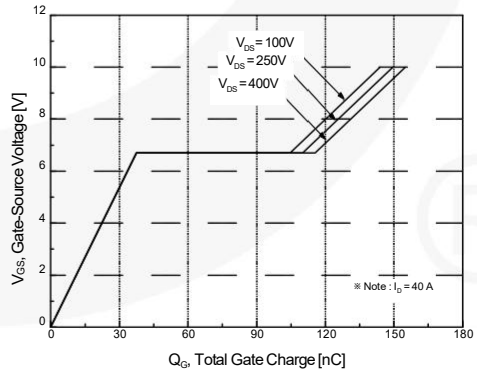


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

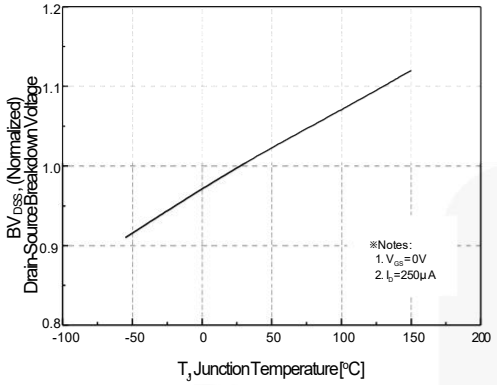


Figure 7. Breakdown Voltage Variation vs. Temperature

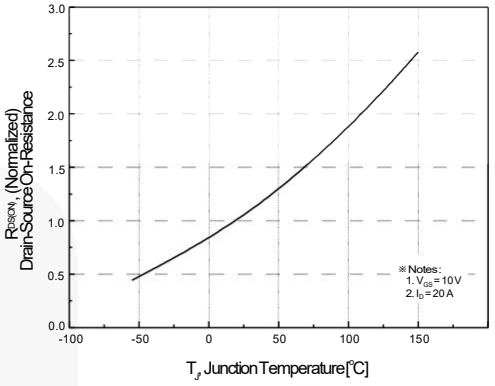


Figure 8. On-Resistance Variation vs. Temperature

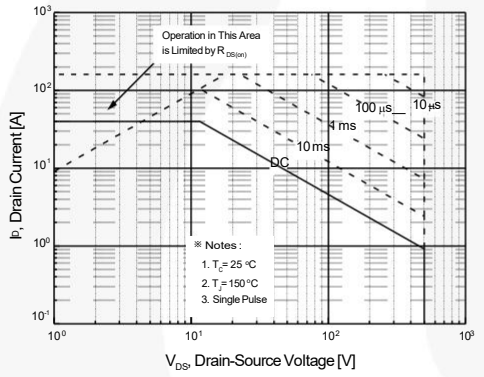


Figure 9. Maximum Safe Operating Area

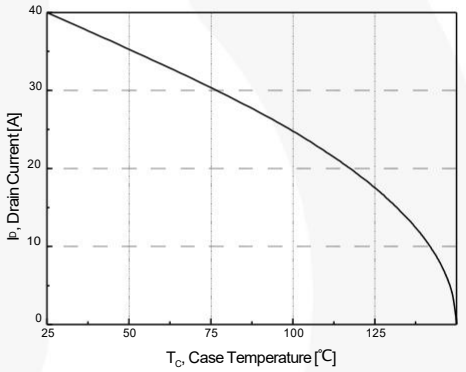


Figure 10. Maximum Drain Current vs. Case Temperature

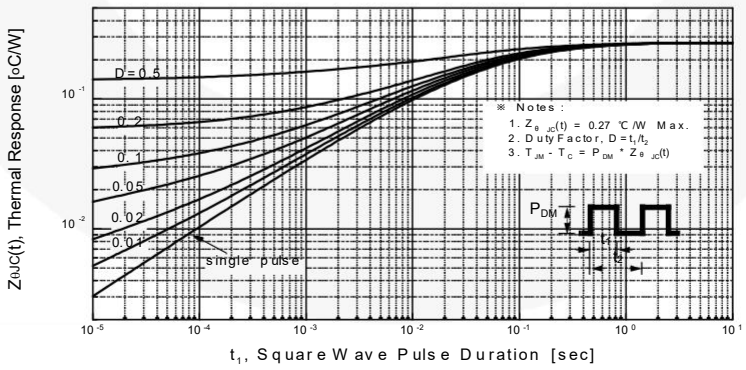


Figure 11. Transient Thermal Response Curve

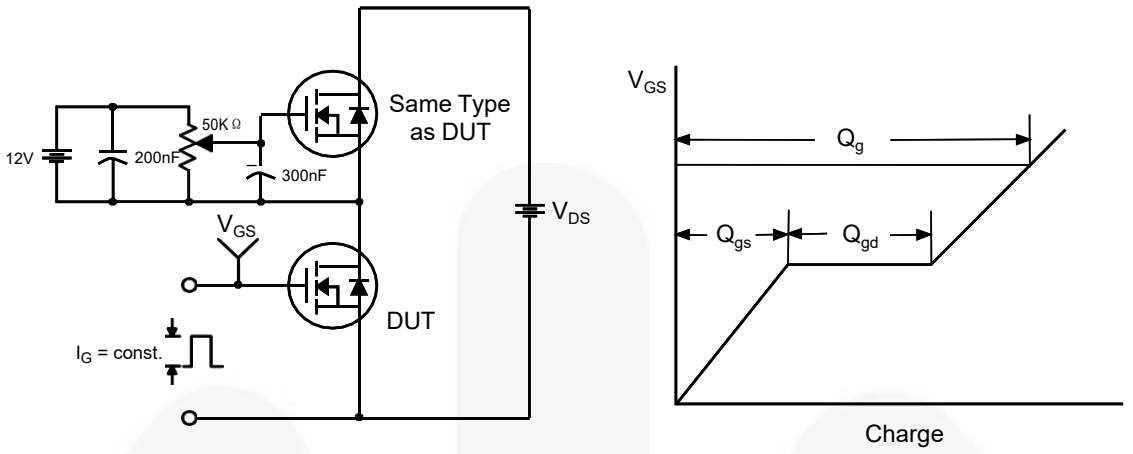


Figure 12. Gate Charge Test Circuit & Waveform

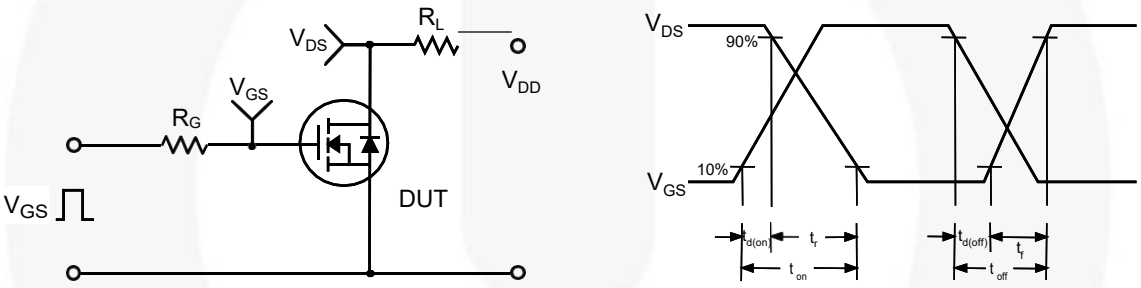


Figure 13. Resistive Switching Test Circuit & Waveforms

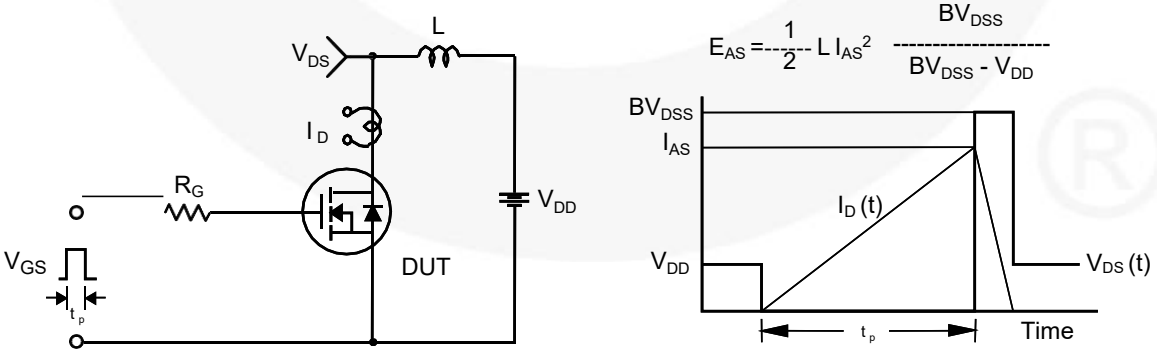


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

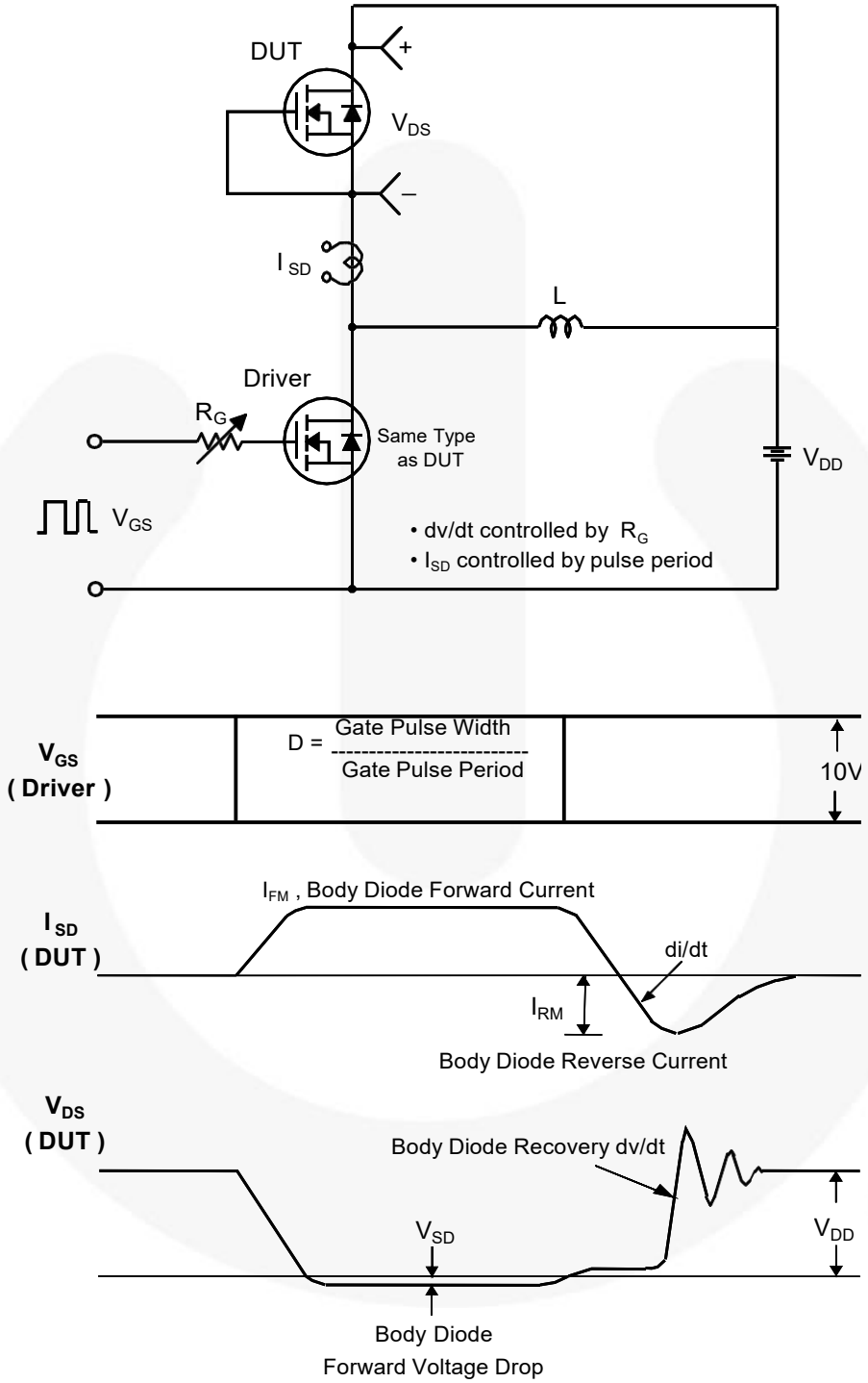


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

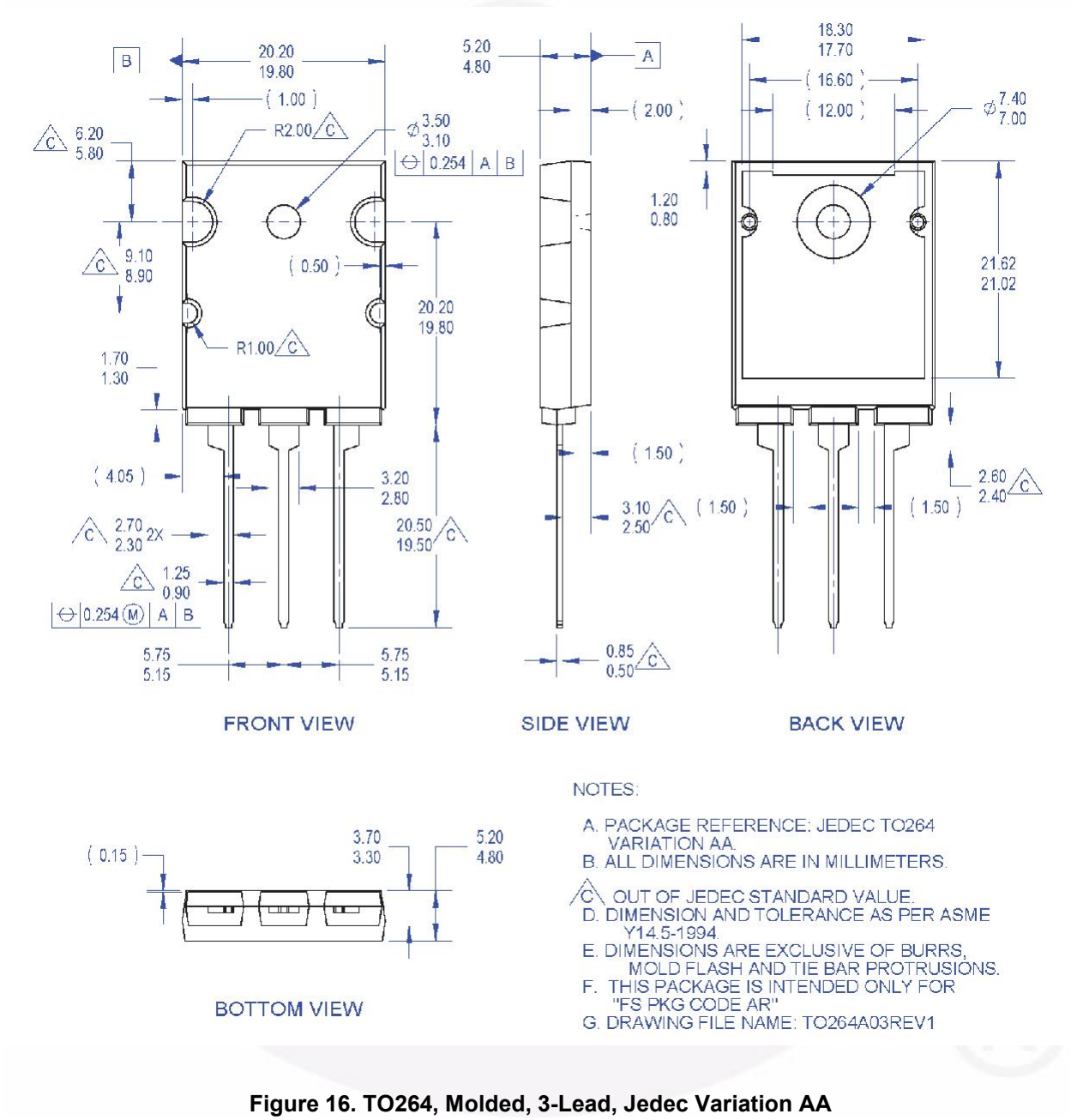


Figure 16. TO264, Molded, 3-Lead, Jedec Variation AA

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