Description (continued)

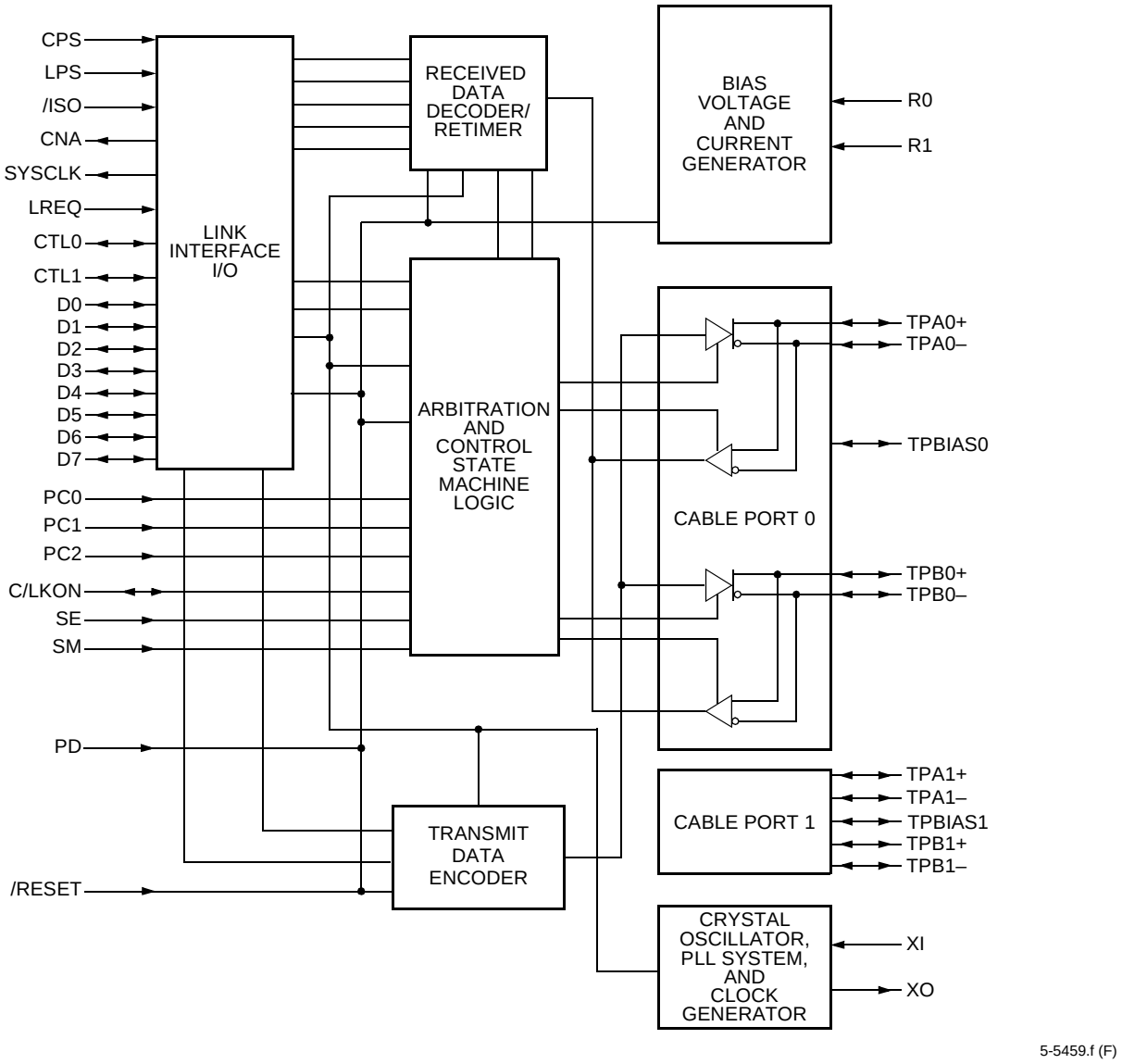
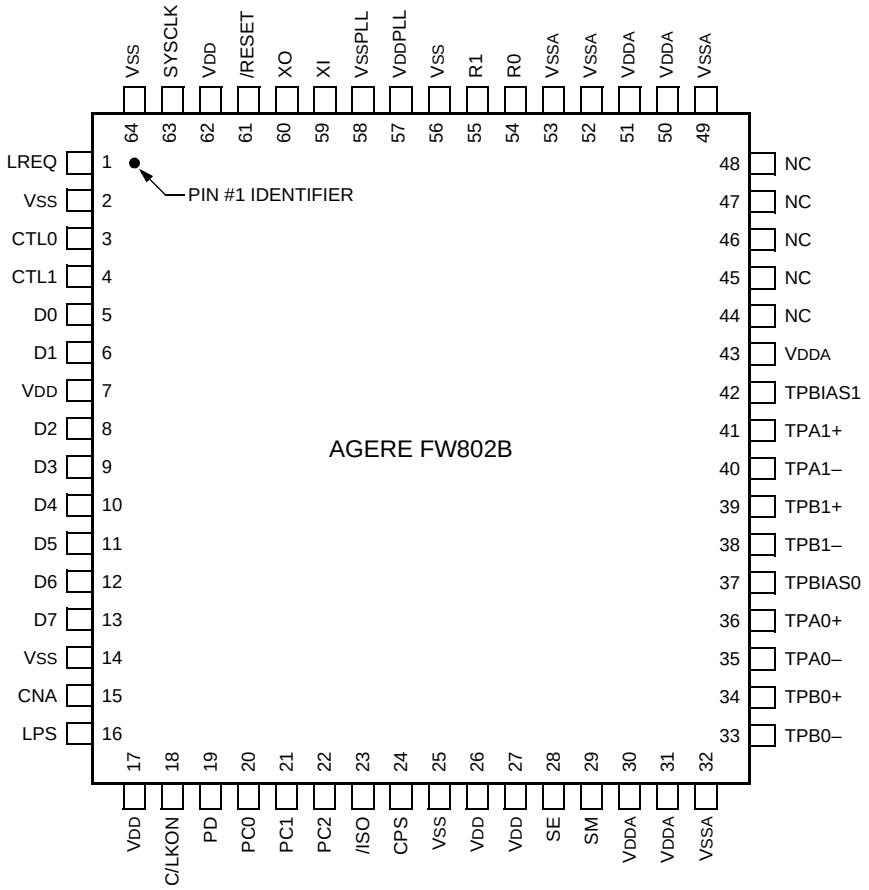


Figure 1. Block Diagram

Signal Information



Note: Active-low signals are indicated by "/" at the beginning of signal names, within this document.

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Figure 2. Pin Assignments

Signal Information (continued)

Table 1. Signal Descriptions

Pin	Signal*	Type	Name/Description
18	C/LKON	I/O	**Bus Manager Capable Input and Link-On Output.** On hardware reset (/RESET), this pin is used to set the default value of the contender status indicated during self-ID. The bit value programming is done by tying the signal through a 10 kΩ resistor to V_{DD} (high, bus manager capable) or to GND (low, not bus manager capable). Using either the pull-up or pull-down resistor allows the link-on output to override the input value when necessary. After hardware reset, this pin is set as an output. If the LPS is inactive, C/LKON indicates one of the following events by asserting a 6.114 MHz signal. 1. FW802B receives a link-on packet addressed to this node. 2. Port_event register bit is 1. 3. Any of the Timeout, Pwr_fail, or Loop register bits are 1 and the Watchdog register bit is also 1. 4. Once activated, the C/LKON output will continue active until the LPS becomes active. The PHY also deasserts the C/LKON output when a *1394* bus reset occurs, if the C/LKON is active due solely to the reception of a link-on packet. **Note:** If an interrupt condition exists which would otherwise cause the C/LKON output to be activated if the LPS were inactive, the C/LKON output will be activated when the LPS subsequently becomes inactive.
15	CNA	O	**Cable-Not-Active Output.** CNA is asserted high when none of the PHY ports are receiving an incoming bias voltage. This circuit remains active during the powerdown mode.
24	CPS	I	**Cable Power Status.** CPS is normally connected to the cable power through a 400 kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This information is maintained in one internal register and is available to the LLC by way of a register read (see Table 8, address register 0000_2, bit 7/PS). In applications that do not sink or source *1394* power (VP), this pin can be tied to ground. **Note:** When this pin is grounded, the Pwr_fail bit in PHY register 0101_2 will be set.
3	CTL0	I/O	**Control I/O.** The CTLn signals are bidirectional communications control signals between the PHY and the LLC. These signals control the passage of information between the two devices. Bus-keeper circuitry is built into these terminals.
4	CTL1		
5, 6, 8, 9, 10, 11, 12, 13	D[0:7]	I/O	**Data I/O.** The Dn signals are bidirectional and pass data between the PHY and the LLC. Bus-keeper circuitry is built into these terminals.

* Active-low signals are indicated by "/" at the beginning of signal names, within this document.

Signal Information (continued)

Table 1. Signal Descriptions (continued)

Pin	Signal*	Type	Name/Description
23	/ISO	I	**Link Interface Isolation Disable Input (Active-Low).** /ISO controls the operation of an internal pulse differentiating function used on the PHY-LLC interface signals, CTLn and Dn, when they operate as outputs. When /ISO is asserted low, the isolation barrier is implemented between PHY and its LLC (as described in Annex J of *IEEE 1394*-1995). /ISO is normally tied high to disable isolation differentiation. Bus-keepers are enabled when /ISO is high (inactive) on CTLn, Dn, and LREQ. When /ISO is low (active), the bus-keepers are disabled. Please refer to Agere's application note *IEEE 1394 Isolation* (AP98-074CMPR) for more information.
16	LPS	I	**Link Power Status.** LPS is connected to either the V_{DD} supplying the LLC or to a pulsed output that is active when the LLC is powered for the purpose of monitoring the LLC power status. If LPS is inactive for more than 1.2 µs and less than 25 µs, the PHY-link interface is reset. If LPS is inactive for greater than 25 µs, the PHY will disable the PHY/link interface to save power. FW802B continues its repeater function.
1	LREQ	I	**Link Request.** LREQ is an output from the LLC that requests the PHY to perform some service. Bus-keeper circuitry is built into this terminal.
44, 45, 46, 47, 48	NC	—	**No Connect.**
20	PC0	I	**Power-Class Indicators.** On hardware reset (/RESET), these inputs set the default value of the power class indicated during SelfID. These bits can be tied to V_{DD} (high) or to ground (low) as required for particular power consumption and source characteristics. In SelfID packet (see Section 4.3.4.1 of the *1394a-2000 Specification*), PC0, the most significant bit of this 3-bit field, corresponds to bit 20, PC1 corresponds to bit 21, and PC2 corresponds to bit 22. As an example, for a Power_Class value of 001, PC0 = 0, PC1 = 0, and PC2 = 1.
21	PC1		
22	PC2		
19	PD	I	**Powerdown.** When asserted high, PD turns off all internal circuitry except the bias-detect circuits that drive the CNA signal. Internal FW802B logic is kept in the reset state as long as PD is asserted. The PD terminal is provided for backward compatibility. It is recommended that the FW802B be allowed to manage its own power consumption using suspend/resume in conjunction with LPS. C/LKON features are defined in the *IEEE 1394*a-2000 specification.
57	V_{DD}PLL	—	**Power for PLL Circuit.** V_{DD}PLL supplies power to the PLL circuitry portion of the device.
58	V_{SS}PLL	—	**Ground for PLL Circuit.** V_{SS}PLL is tied to a low-impedance ground plane.
54	R0	I	**Current Setting Resistor.** An internal reference voltage is applied to a resistor connected between R0 and R1 to set the operating current and the cable driver output current. A low temperature-coefficient resistor (TCR) with a value of 2.49 kΩ ± 1% should be used to meet the *IEEE 1394*-1995 standard requirements for output voltage limits.
55	R1		

* Active-low signals are indicated by "/" at the beginning of signal names, within this document.

Signal Information (continued)

Table 1. Signal Descriptions (continued)

Pin	Signal*	Type	Name/Description
61	/RESET	I	**Reset (Active-Low).** When /RESET is asserted low (active), a *1394* bus reset condition is set on the active cable ports and the FW802B is reset to the reset start state. To guarantee that the PHY will reset, this pin must be held low for at least 2 ms. An internal pull-up resistor connected to V_{DD} is provided so that only an external delay capacitor (0.1 µF) and resistor (510 kΩ), in parallel, are required to connect this pin to ground. This circuitry will ensure that the capacitor will be discharged when PHY power is removed. This input is a standard logic buffer and can also be driven by an open-drain logic output buffer. Do not leave this pin unconnected.
28	SE	I	**Test Mode Control.** SE is used during Agere's manufacturing test and should be tied to V_{SS} for normal operation.
29	SM	I	**Test Mode Control.** SM is used during Agere's manufacturing test and should be tied to V_{SS} for normal operation.
63	SYSCLK	O	**System Clock.** SYSCLK provides a 49.152 MHz clock signal, which is synchronized with the data transfers to the LLC.
36	TPA0+	Analog I/O	**Port0, Port Cable Pair A.** TPA0± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept as short as possible and matched to the external load resistors and to the cable connector. When the FW802B's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
35	TPA0–		
41	TPA1+	Analog I/O	**Port1, Port Cable Pair A.** TPA1± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept as short as possible and matched to the external load resistors and to the cable connector. When the FW802B's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
40	TPA1–		
34	TPB0+	Analog I/O	**Port0, Port Cable Pair B.** TPB0± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept as short as possible and matched to the external load resistors and to the cable connector. When the FW802B's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
33	TPB0–		
39	TPB1+	Analog I/O	**Port1, Port Cable Pair B.** TPB1± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept as short as possible and matched to the external load resistors and to the cable connector. When the FW802B's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
38	TPB1–		

* Active-low signals are indicated by "/" at the beginning of signal names, within this document.

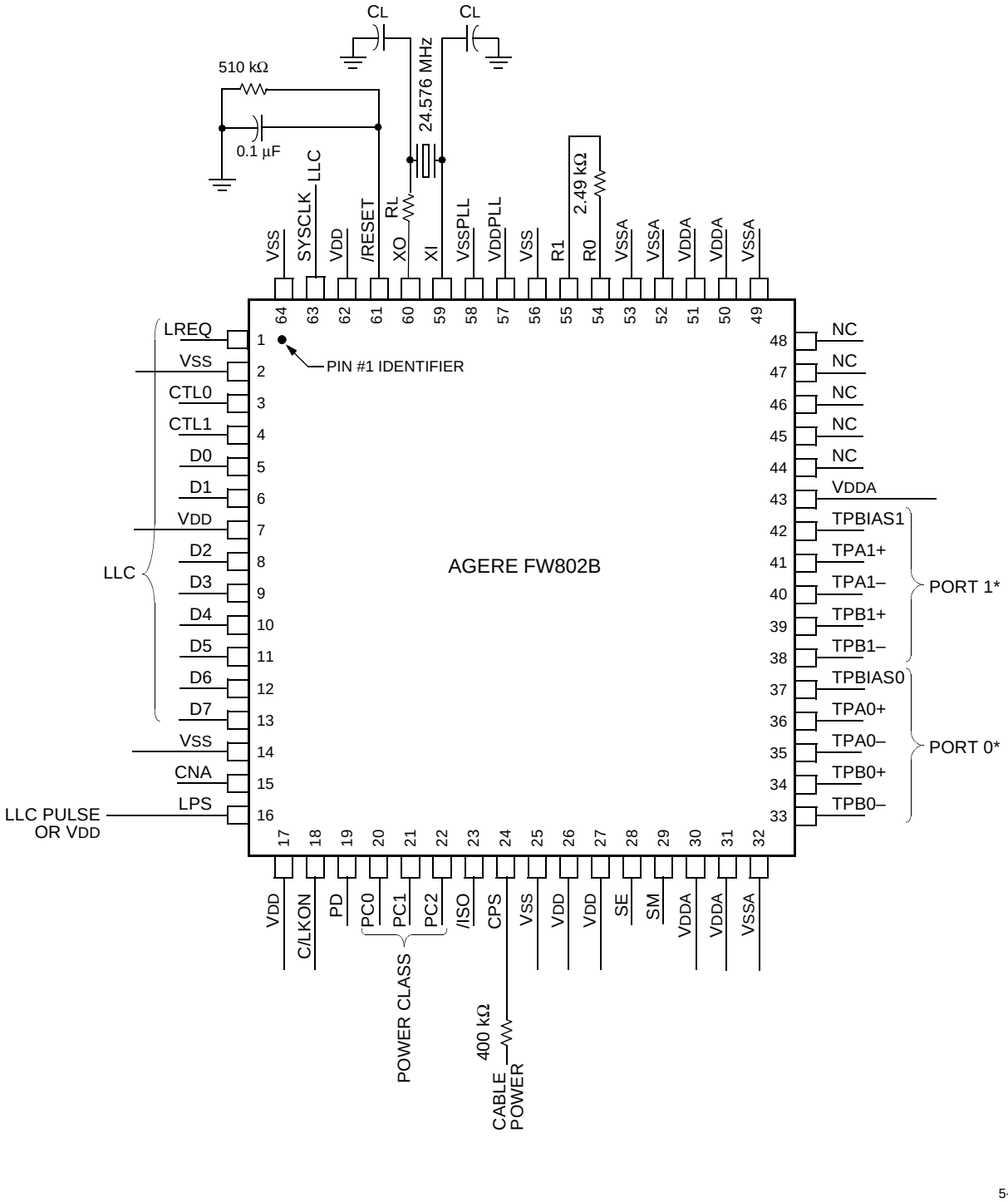
Signal Information (continued)

Table 1. Signal Descriptions (continued)

Pin	Signal*	Type	Name/Description
37	TPBIAS0	Analog I/O	**Portn, Twisted-Pair Bias.** (Where **n** refers to the port number). TPBIAS provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes. When the FW802B's *1394* port pins are not wired to a connector, the unused port pins may be left unconnected. Internal connect-detect circuitry will keep the port in a disconnected state.
42	TPBIAS1		
7, 17, 26, 27, 62	V_{DD}	—	**Digital Power.** V_{DD} supplies power to the digital portion of the device.
30, 31, 43, 50, 51	V_{DDA}	—	**Analog Circuit Power.** V_{DDA} supplies power to the analog portion of the device.
2, 14, 25, 56, 64	V_{SS}	—	**Digital Ground.** All V_{SS} signals should be tied to the low-impedance ground plane.
32, 49, 52, 53	V_{SSA}	—	**Analog Circuit Ground.** All V_{SSA} signals should be tied together to a low-impedance ground plane.
59	XI	—	**Crystal Oscillator.** XI and XO connect to a 24.576 MHz parallel resonant fundamental mode crystal. Although, when a 24.576 MHz clock source is used, it can be connected to XI with XO left unconnected. The optimum values for the external load capacitors and resistor are dependent on the specifications of the crystal used. It is necessary to add an external series resistor (R_L) to the XO pin (see Figures 3 and 5). For more details, refer to the Crystal Selection Considerations section in the data sheet. Note that it is very important to place the crystal as close as possible to the XO and XI pins, i.e., within 0.5 in./1.27 cm.
60	XO		

* Active-low signals are indicated by "/" at the beginning of signal names, within this document.

Application Information



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* See Figure 4 for typical port termination network.

Figure 3. Typical External Component Connections

Application Information (continued)

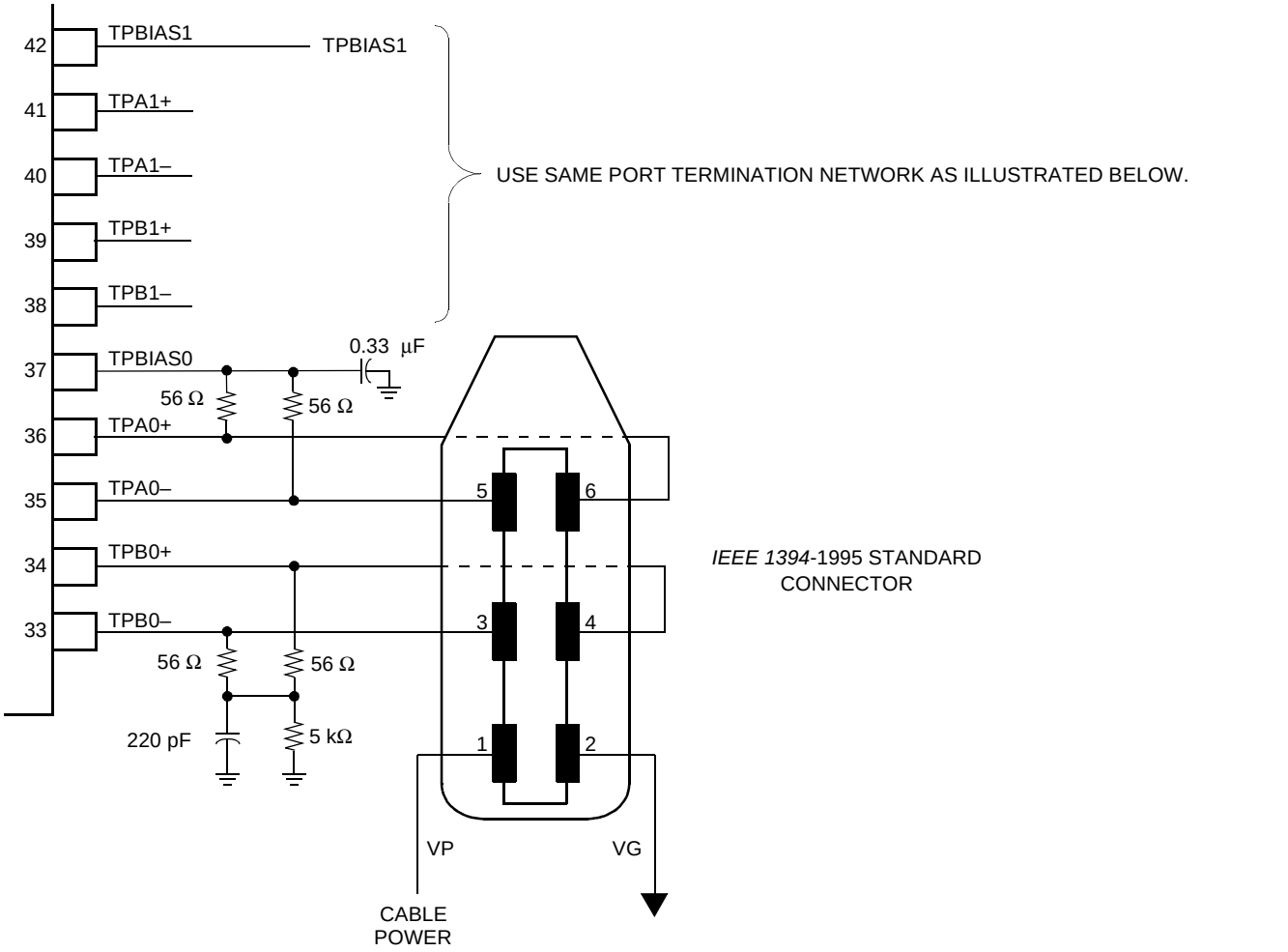


Figure 4. Typical Port Termination Network

Crystal Selection Considerations

The FW802B is designed to use an external 24.576 MHz parallel resonant fundamental mode crystal connected between the XI and XO terminals to provide the reference for an internal oscillator circuit. The *IEEE 1394*a-2000 standard requires that FW802B have less than ±100 ppm total variation from the nominal data rate, which is directly influenced by the crystal. To achieve this, it is recommended that an oscillator with a nominal 50 ppm or less frequency tolerance be used.

The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ±100 ppm.

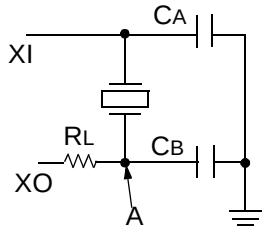
Crystal Selection Considerations (continued)

Load Capacitance

The frequency of oscillation is dependent upon the load capacitance specified for the crystal, in parallel resonant mode crystal circuits. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also capacitances from the FW802B board traces and capacitances of the other FW802B connected components.

The values for load capacitors (C_A and C_B) should be calculated using this formula:

$C_A = C_B = (C_L – C_{stray}) \times 2$



Where:
C_L = load capacitance specified by the crystal manufacturer
Cstray = capacitance of the board and the FW802B, typically 2 pF—3 pF
R_L = load resistance; the value of R_L is dependent on the specific crystal used. Please refer to your crystal manufacturer's data sheet and application notes to determine an appropriate value.

Figure 5. Crystal Circuitry

Adjustment to Crystal Loading

The resistor (R_L) in Figure 5 is recommended for fine-tuning the crystal circuit. The value for this resistor is dependent on the specific crystal used. Please refer to your crystal manufacturer's data sheet and application notes to determine an appropriate value for R_L. A more precise value for this resistor can be obtained by placing different values of R_L on a production board and using an oscilloscope to view the resultant clock waveform at node A for each resistor value. The desired waveform should have the following characteristics: the waveform should be sinusoidal, with an amplitude as large as possible, but not greater than 3.3 V or less than 0 volts.

Crystal/Board Layout

The layout of the crystal portion of the PHY circuit is important for obtaining the correct frequency and minimizing noise introduced into the FW802B PLL. The crystal and two load capacitors (C_A + C_B) should be considered as a unit during layout. They should be placed as close as possible to one another, while minimizing the loop area created by the combination of the three components. Minimizing the loop area minimizes the effect of the resonant current that flows in this resonant circuit. This layout unit (crystal and load capacitors) should then be placed as close as possible to the PHY XI and XO terminals to minimize trace lengths. Vias should not be used to route the XI and XO signals.

1394 Application Support Contact Information

E-mail: support1394@agere.com

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage Range	V_{DD}	3.0	3.6	V
Input Voltage Range*	V_I	–0.5	V_{DD} + 0.5	V
Output Voltage Range at Any Output	V_O	–0.5	V_{DD} + 0.5	V
Operating Free Air Temperature	T_A	0	70	°C
Storage Temperature Range	T_{stg}	–65	150	°C

* Except for 5 V tolerant I/O (CTL0, CTL1, D0—D7, and LREQ) where V_I max = 5.5 V.

Electrical Characteristics

Table 3. Analog Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage	Source power node	$V_{DD—SP}$	3.0	3.3	3.6	V
Differential Input Voltage	Cable inputs, 100 Mbits/s operation	$V_{ID—100}$	142	—	260	mV
	Cable inputs, 200 Mbits/s operation	$V_{ID—200}$	132	—	260	mV
	Cable inputs, 400 Mbits/s operation	$V_{ID—400}$	100	—	260	mV
	Cable inputs, during arbitration	$V_{ID—ARB}$	168	—	265	mV
Common-mode Voltage Source Power Mode	TPB cable inputs, speed signaling off	V_{CM}	1.165	—	2.515	V
	TPB cable inputs, S100 speed signaling on	$V_{CM—SP—100}$	1.165	—	2.515	V
	TPB cable inputs, S200 speed signaling on	$V_{CM—SP—200}$	0.935	—	2.515	V
	TPB cable inputs, S400 speed signaling on	$V_{CM—SP—400}$	0.532	—	2.515	V
Common-mode Voltage Nonsource Power Mode*	TPB cable inputs, speed signaling off	V_{CM}	1.165	—	2.015	V
	TPB cable inputs, S100 speed signaling on	$V_{CM—NSP—100}$	1.165	—	2.015	V
	TPB cable inputs, S200 speed signaling on	$V_{CM—NSP—200}$	0.935	—	2.015	V
	TPB cable inputs, S400 speed signaling on	$V_{CM—NSP—400}$	0.532	—	2.015	V
Receive Input Jitter	TPA, TPB cable inputs, 100 Mbits/s operation	—	—	—	1.08	ns
	TPA, TPB cable inputs, 200 Mbits/s operation	—	—	—	0.5	ns
	TPA, TPB cable inputs, 400 Mbits/s operation	—	—	—	0.315	ns
Receive Input Skew	Between TPA and TPB cable inputs, 100 Mbits/s operation	—	—	—	0.8	ns
	Between TPA and TPB cable inputs, 200 Mbits/s operation	—	—	—	0.55	ns
	Between TPA and TPB cable inputs, 400 Mbits/s operation	—	—	—	0.5	ns
Positive Arbitration Comparator Input Threshold Voltage	—	V_{TH+}	89	—	168	mV
Negative Arbitration Comparator Input Threshold Voltage	—	$V_{TH–}$	–168	—	–89	mV
Speed Signal Input Threshold Voltage	200 Mbits/s	$V_{TH—S200}$	45	—	139	mV
	400 Mbits/s	$V_{TH—S400}$	266	—	445	mV
Output Current	TPBIAS outputs	I_O	–5	—	2.5	mA
TPBIAS Output Voltage	At rated I/O current	V_O	1.665	—	2.015	V
Current Source for Connect Detect Circuit	—	I_{CD}	—	—	76	µA

* For a node that does not source power (see Section 4.2.2.2 in *IEEE 1394*-1995 Standard).

Electrical Characteristics (continued)

Table 4. Driver Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Differential Output Voltage	56 Ω load	V_{OD}	172	—	265	mV
Off-state Common-mode Voltage	Drivers disabled	V_{OFF}	—	—	20	mV
Driver Differential Current, TPA+, TPA–, TPB+, TPB–	Driver enabled, speed signaling off*	I_{DIFF}	–1.05	—	1.05	mA
Common-mode Speed Signaling Current, TPB+, TPB–	200 Mbits/s speed signaling enabled†	I_{SP}	–2.53	—	–4.84	mA
	400 Mbits/s speed signaling enabled†	I_{SP}	–8.1	—	–12.4	mA

* Limits are defined as the algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– as the algebraic sum of driver currents.
† Limits are defined as the absolute limit of each of TPB+ and TPB– driver currents.

Electrical Characteristics (continued)

Table 5. Device Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Current:	V_{DD} = 3.3 V					
One Port Active		I_{DD}	—	54	—	mA
All Ports Active		I_{DD}	—	74	—	mA
No Ports Active, (Microlow-power Sleep Mode) LPS = 0		I_{DD}	—	50	—	µA
PD = 1		I_{DD}	—	50	—	µA
High-level Output Voltage	I_{OH} max, V_{DD} = min	V_{OH}	V_{DD} – 0.4	—	—	V
Low-level Output Voltage	I_{OL} min, V_{DD} = max	V_{OL}	—	—	0.4	V
High-level Input Voltage	CMOS inputs	V_{IH}	0.7 V_{DD}	—	—	V
Low-level Input Voltage	CMOS inputs	V_{IL}	—	—	0.2 V_{DD}	V
Pull-up Current, /RESET Input	V_I = 0 V	I_I	11	—	32	µA
Powerup Reset Time, /RESET Input	V_I = 0 V	—	2	—	—	ms
Rising Input Threshold Voltage /RESET Input	—	V_{IRST}	1.1	—	1.4	V
Output Current	SYSCLK	I_{OL}/I_{OH} @ TTL	–16	—	16	mA
	Control, data	I_{OL}/I_{OH} @ CMOS	–12	—	12	mA
	CNA	I_{OL}/I_{OH}	–16	—	16	mA
	C/LKON	I_{OL}/I_{OH}	–2	—	2	mA
Input Current, LREQ, LPS, PD, SE, SM, PC[0:2] Inputs	V_I = V_{DD} or 0 V	I_I	—	—	°±1	µA
Off-state Output Current, CTL[0:1], D[0:7], C/LKON I/Os	V_O = V_{DD} or 0 V	I_{OZ}	—	—	°±5	µA
Power Status Input Threshold Voltage, CPS Input	400 kΩ resistor	V_{TH}	7.5	—	8.5	V
Rising Input Threshold Voltage*, LREQ, CTLn, Dn	—	V_{IT+}	$V_{DD}/2$ + 0.3	—	$V_{DD}/2$ + 0.8	V
Falling Input Threshold Voltage*, LREQ, CTLn, Dn	—	$V_{IT–}$	$V_{DD}/2$ – 0.8	—	$V_{DD}/2$ – 0.3	V
Bus Holding Current, LREQ, CTLn, Dn	V_I = 1/2(V_{DD})	—	250	—	550	µA
Rising Input Threshold Voltage LPS	—	V_{LIH}	—	—	0.24 V_{DD} + 1	V
Falling Input Threshold Voltage LPS	—	V_{LIL}	0.24 V_{DD} + 0.2	—	—	V

* Device is capable of both differentiated and undifferentiated operation.

Timing Characteristics

Table 6. Switching Characteristics

Symbol	Parameter	Measured	Test Conditions	Min	Typ	Max	Unit
—	Jitter, Transmit	TPA, TPB	—	—	—	0.15	ns
—	Transmit Skew	Between TPA and TPB	—	—	—	±0.1	ns
t_r	Rise Time, Transmit (TPA/TPB)	10% to 90%	R_l = 56 Ω, C_l = 10 pF	—	—	1.2	ns
t_f	Fall Time, Transmit (TPA/TPB)	90% to 10%	R_l = 56 Ω, C_l = 10 pF	—	—	1.2	ns
t_{su}	Setup Time, Dn, CTLn, LREQ↑↓ to SYSCLK↑	50% to 50%	See Figure 6.	6	—	—	ns
t_h	Hold Time, Dn, CTLn, LREQ↑↓ from SYSCLK↑	50% to 50%	See Figure 6.	0	—	—	ns
t_d	Delay Time, SYSCLK↑ to Dn, CTLn↑↓	50% to 50%	See Figure 7.	1	—	6	ns

Table 7. Clock Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
External Clock Source Frequency	f	24.5735	24.5760	24.5785	MHz

Timing Waveforms

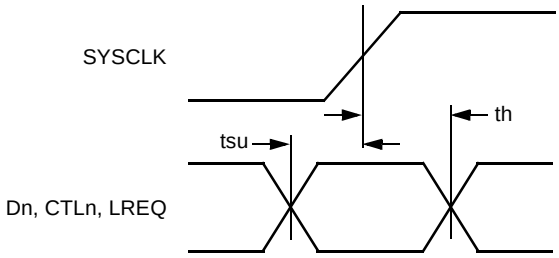


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Figure 6. Dn, CTLn, and LREQ Input Setup and Hold Times Waveforms

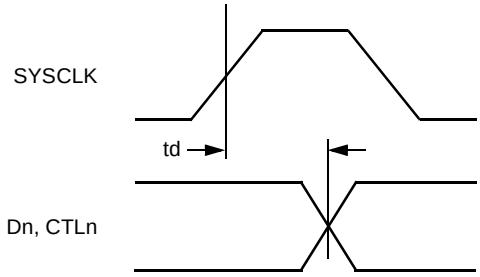

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Figure 7. Dn, CTLn Output Delay Relative to SYSCLK Waveforms

Internal Register Configuration

The PHY register map is shown below in Table 8. (Refer to *IEEE 1394*a-2000, 5B.1 for more information).

Table 8. PHY Register Map for the Cable Environment

Address	Contents							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0000_2	Physical_ID						R	PS
0001_2	RHB	IBR	Gap_count					
0010_2	Extended (7)			XXXXX	Total_ports			
0011_2	Max_speed			XXXXX	Delay			
0100_2	LCtrl	Contender	Jitter			Pwr_class		
0101_2	Watchdog	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
0111_2	Page_select			XXXXX	Port_select			
1000_2	Register 0 Page_select							
⋮	⋮							⋮
1111_2	Register 7 Page_select							

REQUIRED XXXXX RESERVED

The meaning of the register fields within the PHY register map are defined by Table 9 below. Power reset values not specified are resolved by the operation of the PHY state machines subsequent to a power reset.

Table 9. PHY Register Fields for the Cable Environment

Field	Size	Type	Power Reset Value	Description
Physical_ID	6	r	000000	The address of this node determined during self-identification. A value of 63 indicates a malconfigured bus; the link will not transmit any packets.
R	1	r	0	When set to one, indicates that this node is the root.
PS	1	r	—	Cable power active.
RHB	1	rw	0	**Root Hold-off Bit.** When set to one, the force_root variable is TRUE, which instructs the PHY to attempt to become the root during the next tree identify process.
IBR	1	rw	0	**Initiate Bus Reset.** When set to one, instructs the PHY to set ibr TRUE and reset_time to RESET_TIME. These values in turn cause the PHY to initiate a bus reset without arbitration; the reset signal is asserted for 166 µs. This bit is self-clearing.
Gap_count	6	rw	$3F_{16}$	Used to configure the arbitration timer setting in order to optimize gap times according to the topology of the bus. See Section 4.3.6 of *IEEE* Standard *1394a*-2000 for the encoding of this field.
Extended	3	r	7	This field has a constant value of seven, which indicates the extended PHY register map.

Internal Register Configuration (continued)

Table 9. PHY Register Fields for the Cable Environment (continued)

Field	Size	Type	Power Reset Value	Description
Total_ports	4	r	2	The number of ports implemented by this PHY. This count reflects the number.
Max_speed	3	r	010_2	Indicates the speed(s) this PHY supports: 000_2 = 98.304 Mbits/s 001_2 = 98.304 and 196.608 Mbits/s 010_2 = 98.304, 196.608, and 393.216 Mbits/s 011_2 = 98.304, 196.608, 393.216, and 786.43 Mbits/s 100_2 = 98.304, 196.608, 393.216, 786.432, and 1,572.864 Mbits/s 101_2 = 98.304, 196.608, 393.216, 786.432, 1,572.864, and 3,145.728 Mbits/s All other values are reserved for future definition.
Delay	4	r	0000	Worst-case repeater delay, expressed as 144 + (delay * 20) ns.
LCtrl	1	rw	1	**Link Active.** Cleared or set by software to control the value of the L bit transmitted in the node's self-ID packet 0, which will be the logical AND of this bit and LPS active.
Contender	1	rw	See description.	Cleared or set by software to control the value of the C bit transmitted in the self-ID packet. Powerup reset value is set by C/LKON pin.
Jitter	3	r	000	The difference between the fastest and slowest repeater data delay, expressed as (jitter + 1) * 20 ns.
Pwr_class	3	rw	See description.	**Power-Class.** Controls the value of the pwr field transmitted in the self-ID packet. See Section 4.3.4.1 of *IEEE* Standard *1394*a-2000 for the encoding of this field. PC0, PC1, and PC2 pins set up power reset value.
Watchdog	1	rw	0	When set to one, the PHY will set Port_event to one if resume operations commence for any port.
ISBR	1	rw	0	**Initiate Short (Arbitrated) Bus Reset.** A write of one to this bit instructs the PHY to set ISBR true and reset_time to SHORT_RESET_TIME. These values in turn cause the PHY to arbitrate and issue a short bus reset. This bit is self-clearing.
Loop	1	rw	0	**Loop Detect.** A write of one to this bit clears it to zero.
Pwr_fail	1	rw	1	**Cable Power Failure Detect.** Set to one when the PS bit changes from one to zero. A write of one to this bit clears it to zero.
Timeout	1	rw	0	**Arbitration State Machine Timeout.** A write of one to this bit clears it to zero (see MAX_ARB_STATE_TIME).
Port_event	1	rw	0	**Port Event Detect.** The PHY sets this bit to one if any of connected, bias, disabled, or fault change for a port whose Int_enable bit is one. The PHY also sets this bit to one if resume operations commence for any port and Watchdog is one. A write of one to this bit clears it to zero.

Internal Register Configuration (continued)

Table 9. PHY Register Fields for the Cable Environment (continued)

Field	Size	Type	Power Reset Value	Description
Enab_accel	1	rw	0	**Enable Arbitration Acceleration.** When set to one, the PHY will use the enhancements specified in Section 4.4 of *1394*a-2000 specification. PHY behavior is unspecified if the value of Enab_accel is changed while a bus request is pending.
Enab_multi	1	rw	0	**Enable Multispeed Packet Concatenation.** When set to one, the link will signal the speed of all packets to the PHY.
Page_select	3	rw	000	Selects which of eight possible PHY register pages are accessible through the window at PHY register addresses 1000_2 through 1111_2, inclusive.
Port_select	4	rw	000	If the page selected by Page_select presents per-port information, this field selects which port's registers are accessible through the window at PHY register addresses 1000_2 through 1111_2, inclusive. Ports are numbered monotonically starting at zero, p0.

The port status page is used to access configuration and status information for each of the PHY's ports. The port is selected by writing zero to Page_select and the desired port number to Port_select in the PHY register at address 0111_2. The format of the port status page is illustrated by Table 10 below; reserved fields are shown shaded. The meanings of the register fields with the port status page are defined by Table 11.

Table 10. PHY Register Page 0: Port Status Page

Address	Contents							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1000_2	AStat		BStat		Child	Connected	Bias	Disabled
1001_2	Negotiated_speed			Int_enable	Fault	XXXXX	XXXXX	XXXXX
1010_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
1011_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
1100_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
1101_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
1110_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
1111_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX

REQUIRED XXXXX RESERVED

Internal Register Configuration (continued)

The meaning of the register fields with the port status page are defined by Table 11 below.

Table 11. PHY Register Port Status Page Fields

Field	Size	Type	Power Reset Value	Description
AStat	2	r	—	TPA line state for the port: 00_2 = invalid 01_2 = 1 10_2 = 0 11_2 = Z
BStat	2	r	—	TPB line state for the port (same encoding as AStat).
Child	1	r	0	If equal to one, the port is a child; otherwise, a parent. The meaning of this bit is undefined from the time a bus reset is detected until the PHY transitions to state T1: Child Handshake during the tree identify process (see Section 4.4.2.2 in *IEEE* Standard *1394*-1995).
Connected	1	r	0	If equal to one, the port is connected.
Bias	1	r	0	If equal to one, incoming TPBIAS is detected.
Disabled	1	rw	0	If equal to one, the port is disabled.
Negotiated_speed	3	r	000	Indicates the maximum speed negotiated between this PHY port and its immediately connected port; the encoding is the same as for the PHY register Max_speed field.
Int_enable	1	rw	0	**Enable Port Event Interrupts.** When set to one, the PHY will set Port_event to one if any of connected, bias, disabled, or fault (for this port) change state.
Fault	1	rw	0	Set to one if an error is detected during a suspend or resume operation. A write of one to this bit clears it to zero.

Internal Register Configuration (continued)

The vendor identification page is used to identify the PHY's vendor and compliance level. The page is selected by writing one to Page_select in the PHY register at address 0111_2. The format of the vendor identification page is shown in Table 12; reserved fields are shown shaded.

Table 12. PHY Register Page 1: Vendor Identification Page

Address	Contents							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1000_2	Compliance_level							
1001_2	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX
1010_2	Vendor_ID							
1011_2								
1100_2								
1101_2	Product_ID							
1110_2								
1111_2								

REQUIRED XXXXX RESERVED

The meaning of the register fields within the vendor identification page are defined by Table 13.

Table 13. PHY Register Vendor Identification Page Fields

Field	Size	Type	Description
Compliance_level	8	r	Standard to which the PHY implementation complies: 0 = not specified 1 = *IEEE 1394*a-2000 Agere's FW802B compliance level is 1. All other values reserved for future standardization.
Vendor_ID	24	r	The company ID or organizationally unique identifier (OUI) of the manufacturer of the PHY. Agere's vendor ID is $00601D_{16}$. This number is obtained from the *IEEE* registration authority committee (RAC). The most significant byte of Vendor_ID appears at PHY register location 1010_2 and the least significant at 1100_2.
Product_ID	24	r	The meaning of this number is determined by the company or organization that has been granted Vendor_ID. Agere's FW802B product ID is 080201_{16}. The most significant byte of Product_ID appears at PHY register location 1101_2 and the least significant at 1111_2.

The vendor-dependent page provides access to information used in manufacturing test of the FW802B.

Outline Diagrams

64-Pin TQFP

Dimensions are in millimeters

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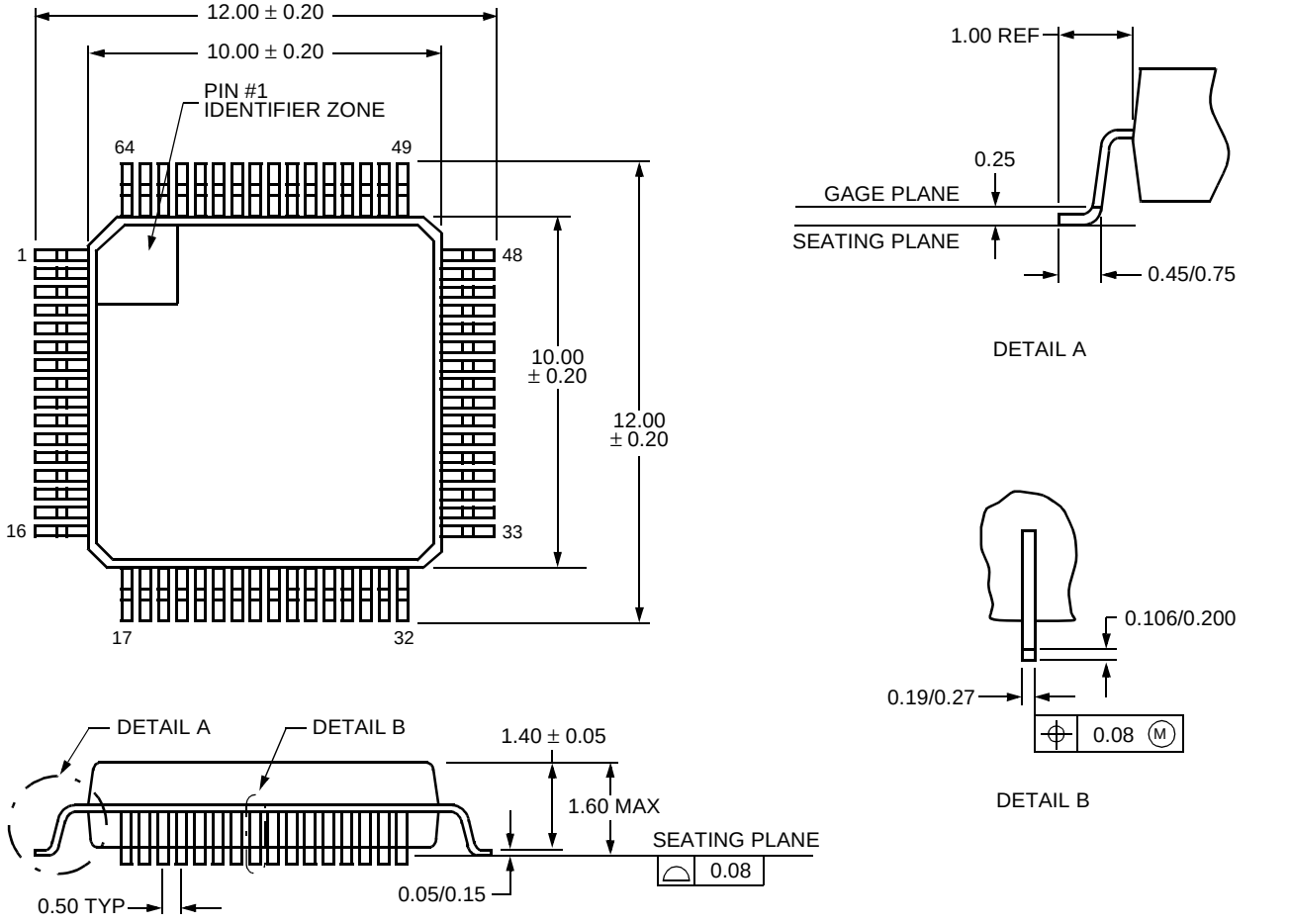

5-3080 (F)

Ordering Information

Device Code	Package	Comcode
FW802B-DB	64-Pin TQFP	700032322
L-FW802B-DB	64-Pin TQFP (lead-free)*	700067297

* In an effort to better serve its customers and the environment, Agere is switching to lead-free packaging on this product (no intentional addition of lead).