HD74LS273

Octal D-type Positive-edge-triggered Flip-Flops (with Clear)

The HD74LS273, positive-edge-triggered flip-flops utilize LS TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse.

When the clock input is at either the high or low level, the D input signal has no effect at the output.

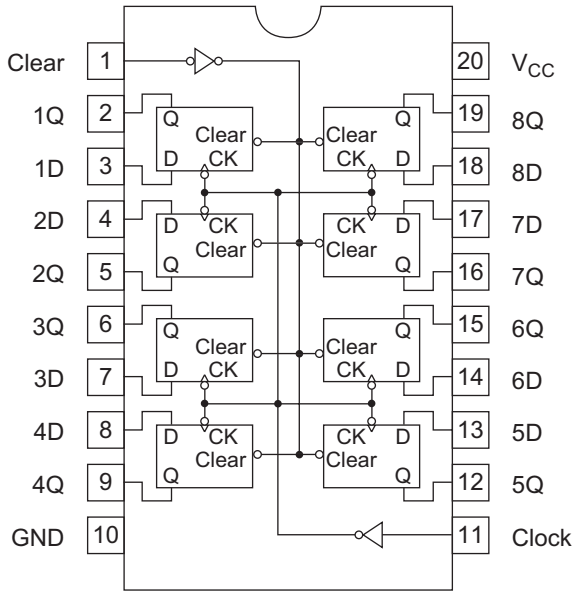
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS273P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS273FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS273RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



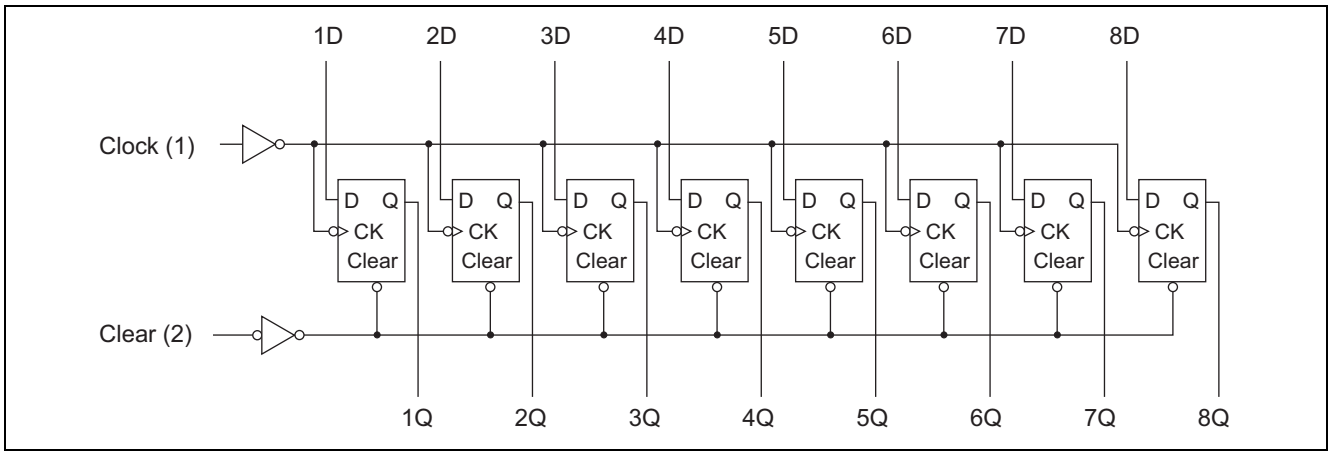
(Top view)

Function Table

Inputs			Output
Clear	**Clock**	**D**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Notes: H; high level, L; low level, X; irrelevant
↑; transition from low to high level
Q_0; level of Q before the indicated steady-state input conditions were established.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Clock pulse width	$t_{w\ (clock)}$	20	—	—	ns
Clear pulse width	$t_{w\ (clear)}$	20	—	—	ns
Data setup time	$t_{su\ (data)}$	20↑	—	—	ns
Clear (inactive-state) setup time	$t_{su\ (clear)}$	25↑	—	—	ns
Data hold time	$t_{h\ (data)}$	5↑	—	—	ns

Electrical Characteristics

($Ta = -20$ to $+75$ °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.4		I_{OL} = 4 mA
Input current	I_{IH}	—		20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—		–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—		0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current	I_{CC}**	—	17	27	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V is applied to clock.

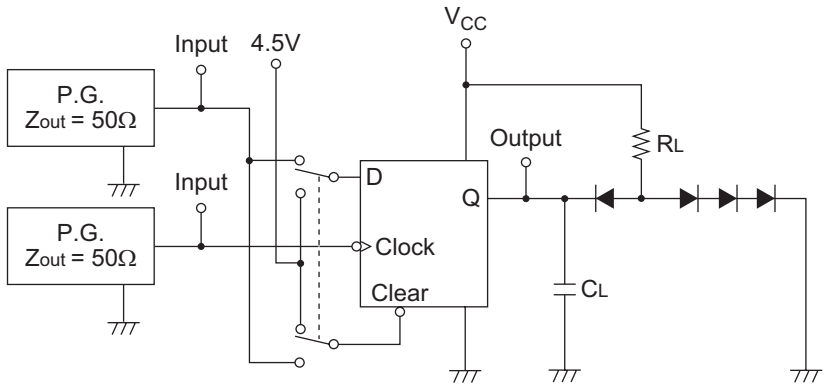
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	30	40	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PHL}	Clear	—	18	27	ns	
	t_{PLH}	Clock	—	17	27		
	t_{PHL}		—	18	27		

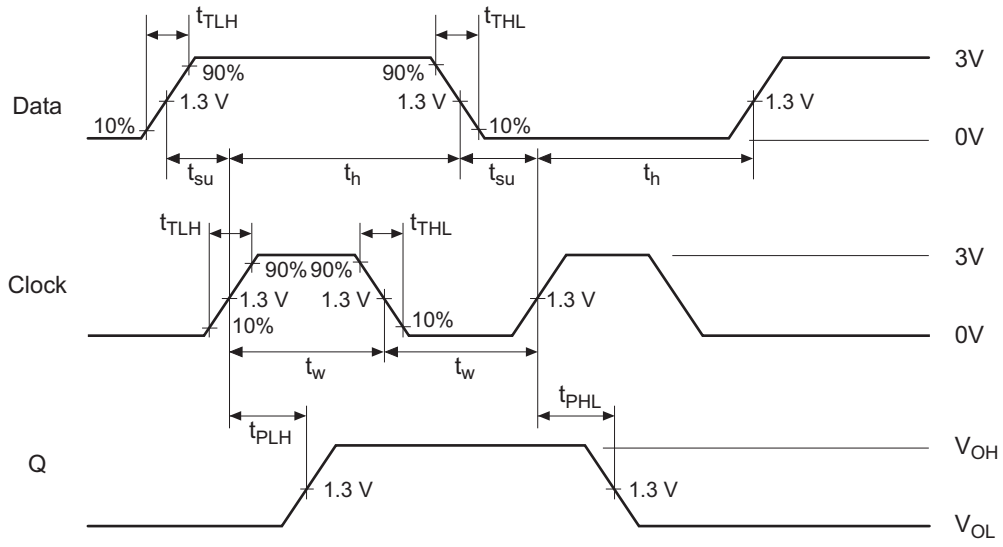
Testing Method

Test Circuit



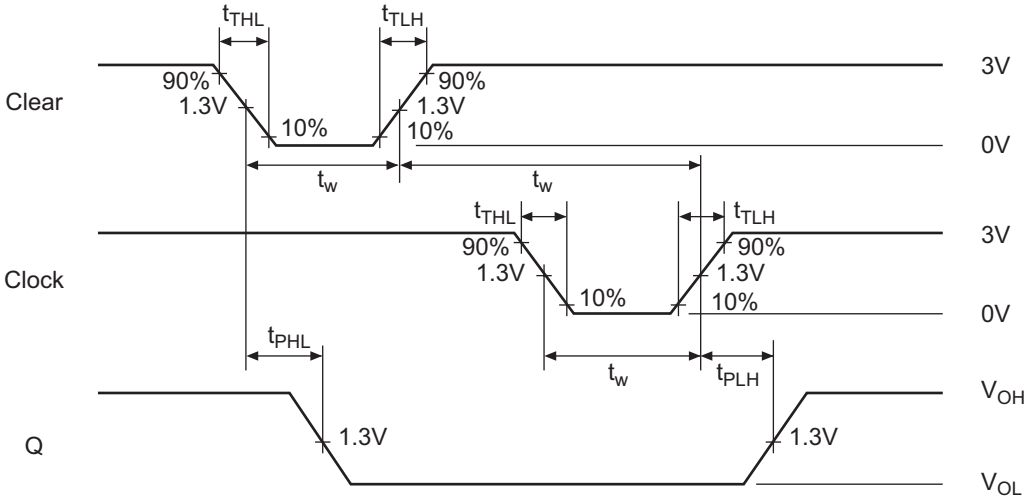
Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveforms 1



Notes: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns,
Clock input; PRR = 1 MHz, duty cycle 50%
Data input; PRR = 500 kHz, duty cycle 50%

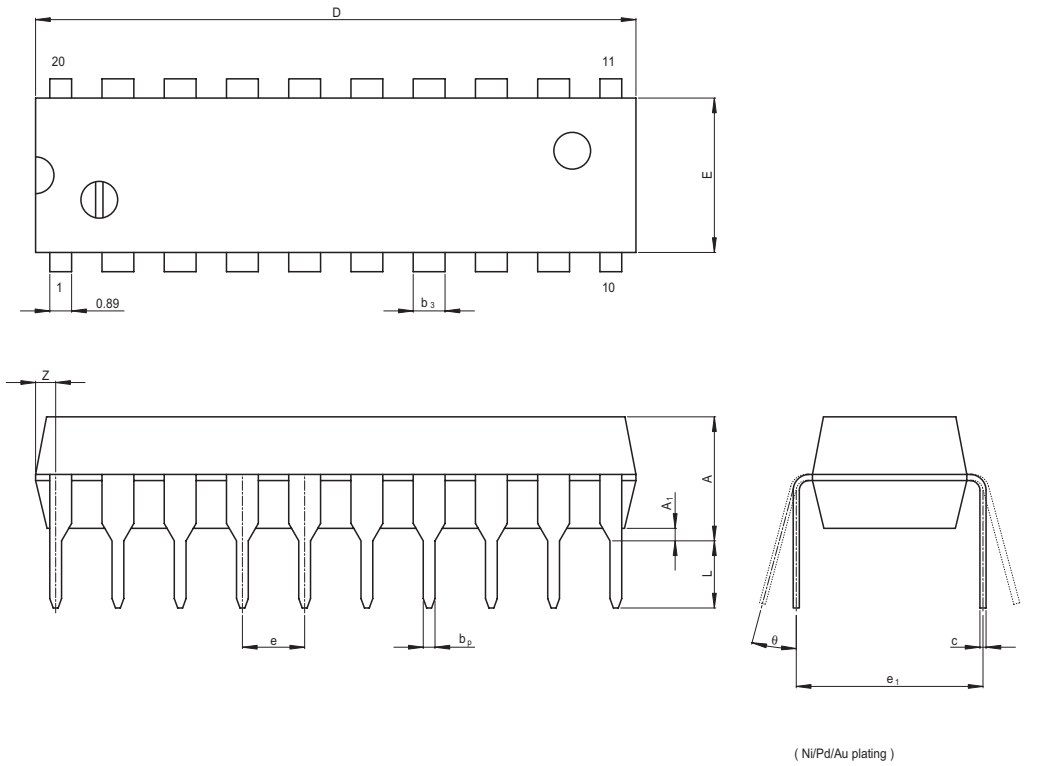
Waveforms 2



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz.

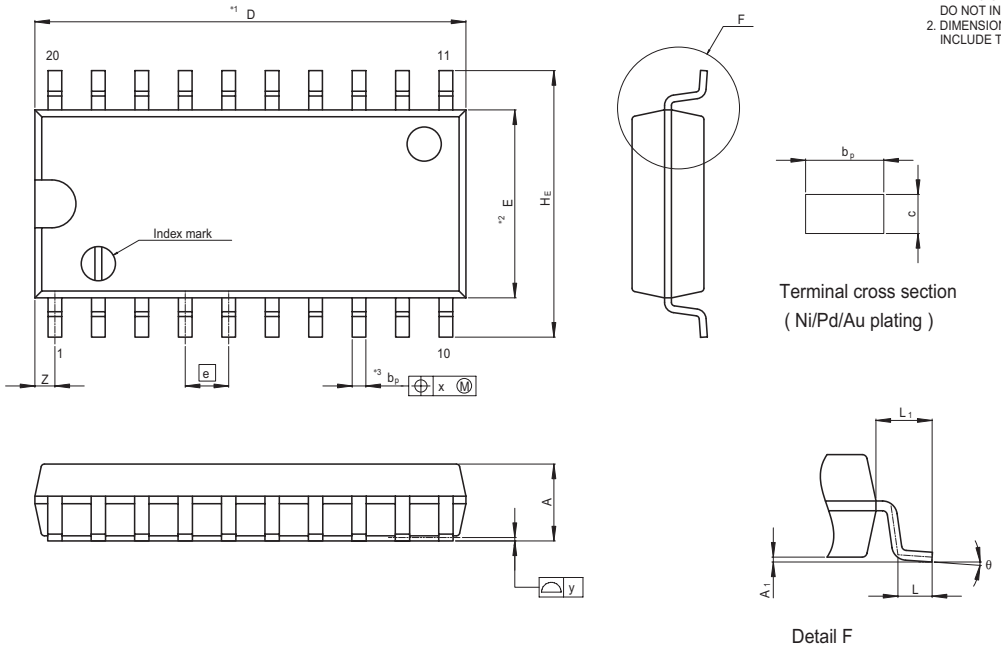
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.3x24.5-2.54	PRDP0020AC-B	DP-20NEV	1.26g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	24.50	25.40
E	——	6.30	7.00
A	——	——	5.08
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.27
L	2.54	——	——

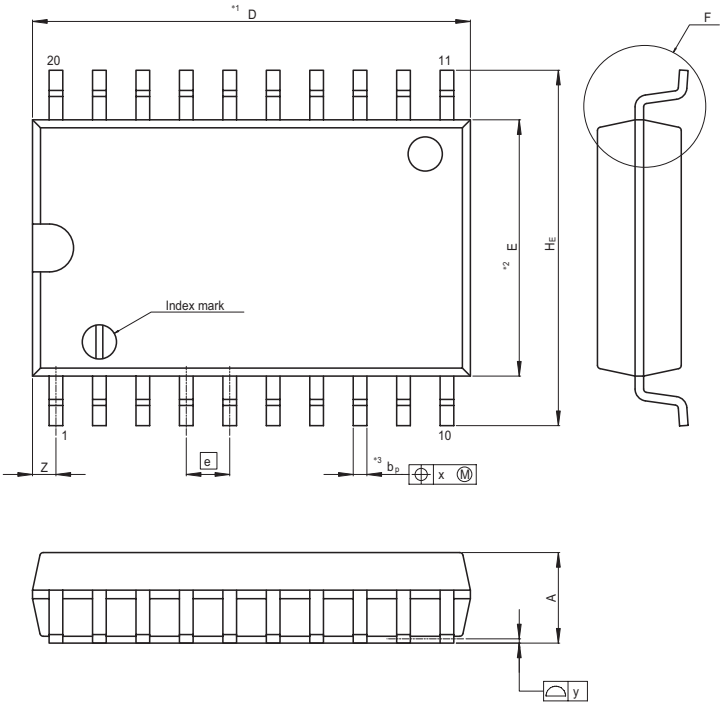
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g



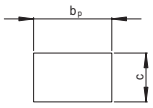
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	12.60	13.0
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

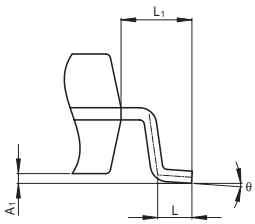
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-7.5x12.8-1.27	PRSP0020DC-A	FP-20DBV	0.52g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   @ DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   @ INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	12.80	13.2
E	——	7.50	——
A_2	——	——	——
A_1	0.10	0.20	0.30
A	——	——	2.65
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.20	0.25	0.30
c_1	——	——	——
θ	0°	——	8°
H_E	10.00	10.40	10.65
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.935
L	0.40	0.70	1.27
L_1	——	1.45	——