

HD74LS164

8-Bit Parallel-Out Serial-in Shift Register

REJ03D0448-0200

Rev.2.00

Feb.18.2005

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

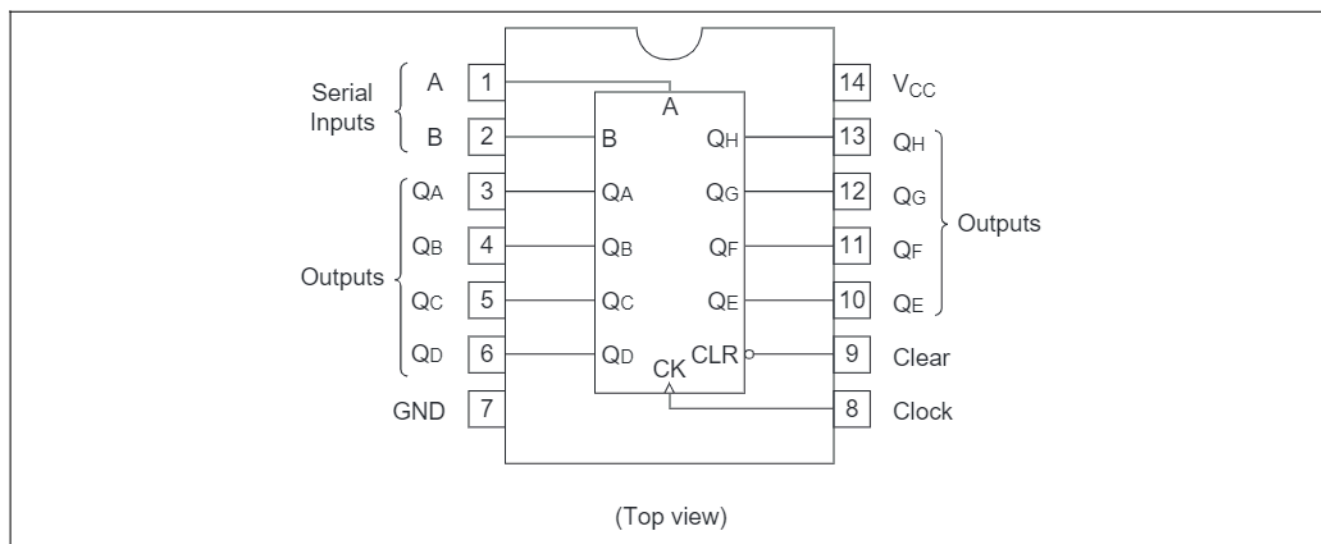
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS164P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS164FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LS164RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

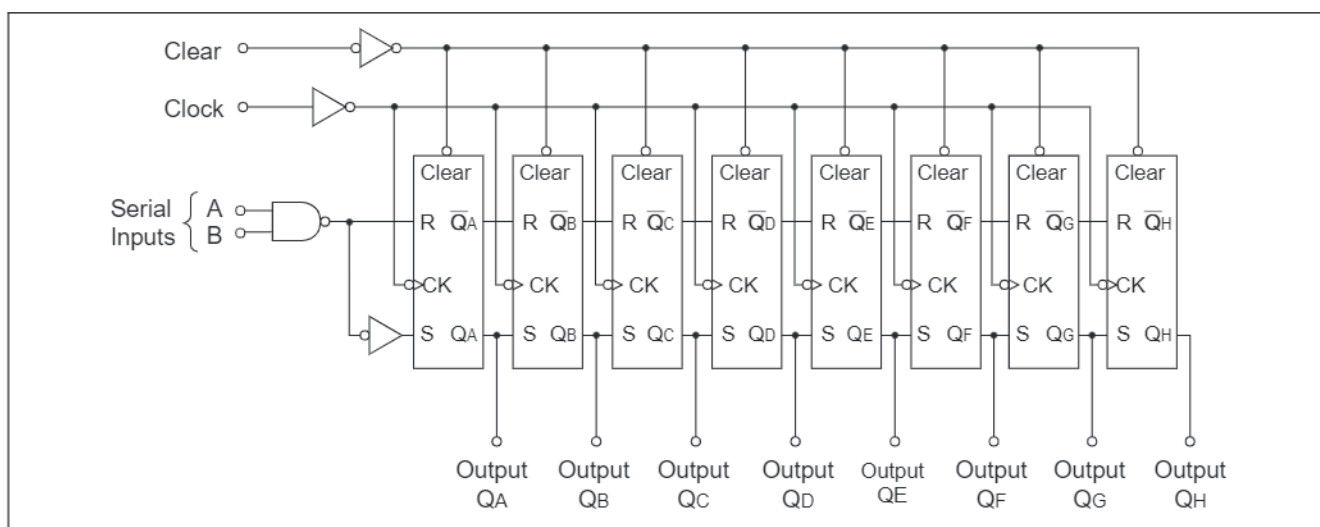


Function Table

Inputs				Outputs		
Clear	Clock	A	B	Q _A	Q _BQ _H	
L	X	X	X	L	L	L
H	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	↑	H	H	H	Q _{An}	Q _{Gn}
H	↑	L	X	L	Q _{An}	Q _{Gn}
H	↑	X	L	L	Q _{An}	Q _{Gn}

- Notes: 1. H; high level, L; low level, X; irrelevant
 2. ↑; transition from low to high level
 3. Q_{A0}, Q_{B0}, Q_{H0}; the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
 4. Q_{An}, Q_{Gn}; the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	T _{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
Output current	I _{OH}	—	—	-400	mA
	I _{OL}	—	—	8	mA
Operating temperature	T _{opr}	-20	25	75	°C
Clock frequency	f _{clock}	0	—	25	MHz
Clock pulse width	t _w (CK)	20	—	—	ns
Clear pulse width	t _w (CLR)	20	—	—	ns
Data setup time	t _{su}	15	—	—	ns
Data hold time	t _h	5	—	—	ns

Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V _{IH}	2.0	—	—	V	
	V _{IL}	—	—	0.8	V	
Output voltage	V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μ A
	V _{OL}	—	—	0.4	V	I _{OL} = 4 mA
		—	—	0.5		I _{OL} = 8 mA
Input current	I _{IH}	—	—	20	μ A	V _{CC} = 5.25 V, V _I = 2.7 V
	I _{IL}	—	—	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	I _I	—	—	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
Short-circuit output current	I _{OS}	-20	—	-100	mA	V _{CC} = 5.25 V
Supply current**	I _{CC}	—	16	27	mA	V _{CC} = 5.25 V
Input clamp voltage	V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

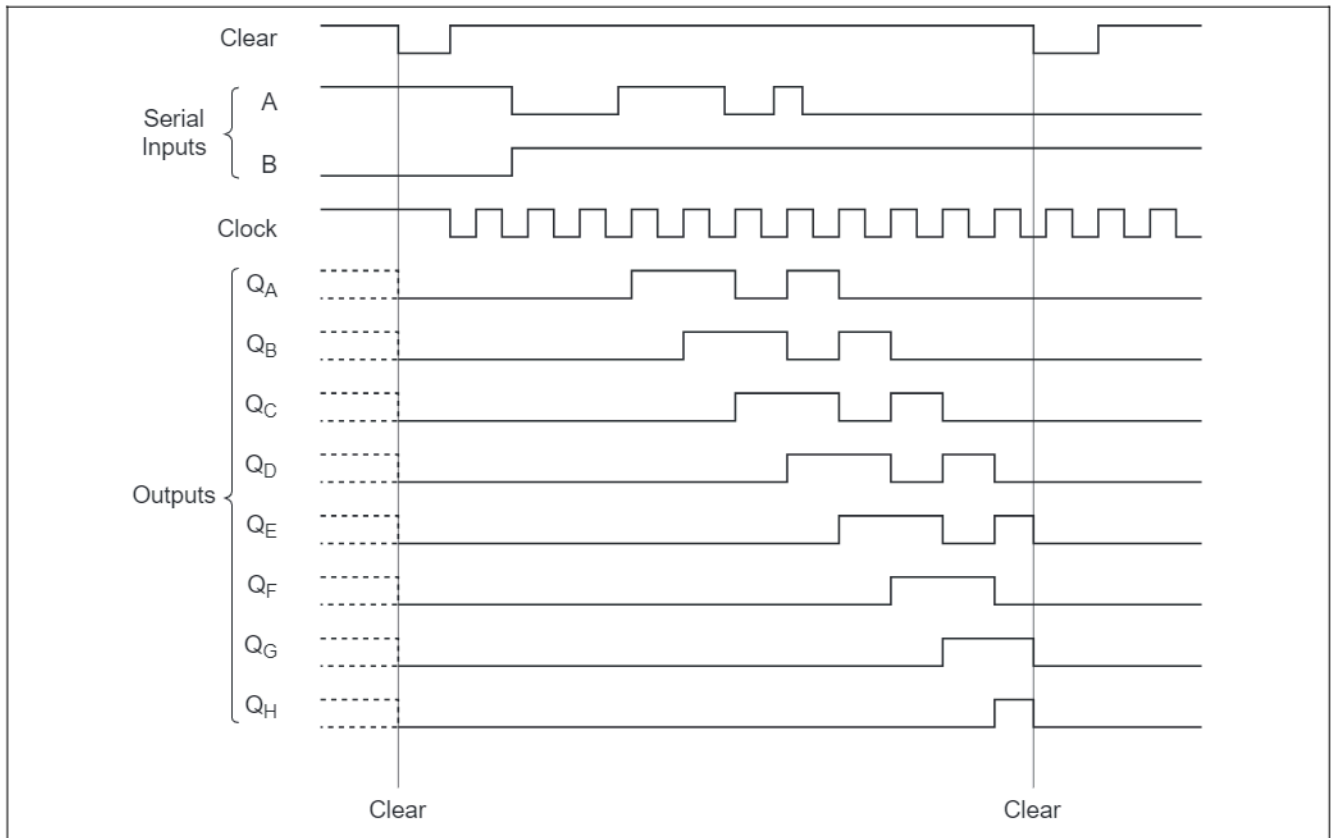
** I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary grounded, then 4.5 V applied to clear.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

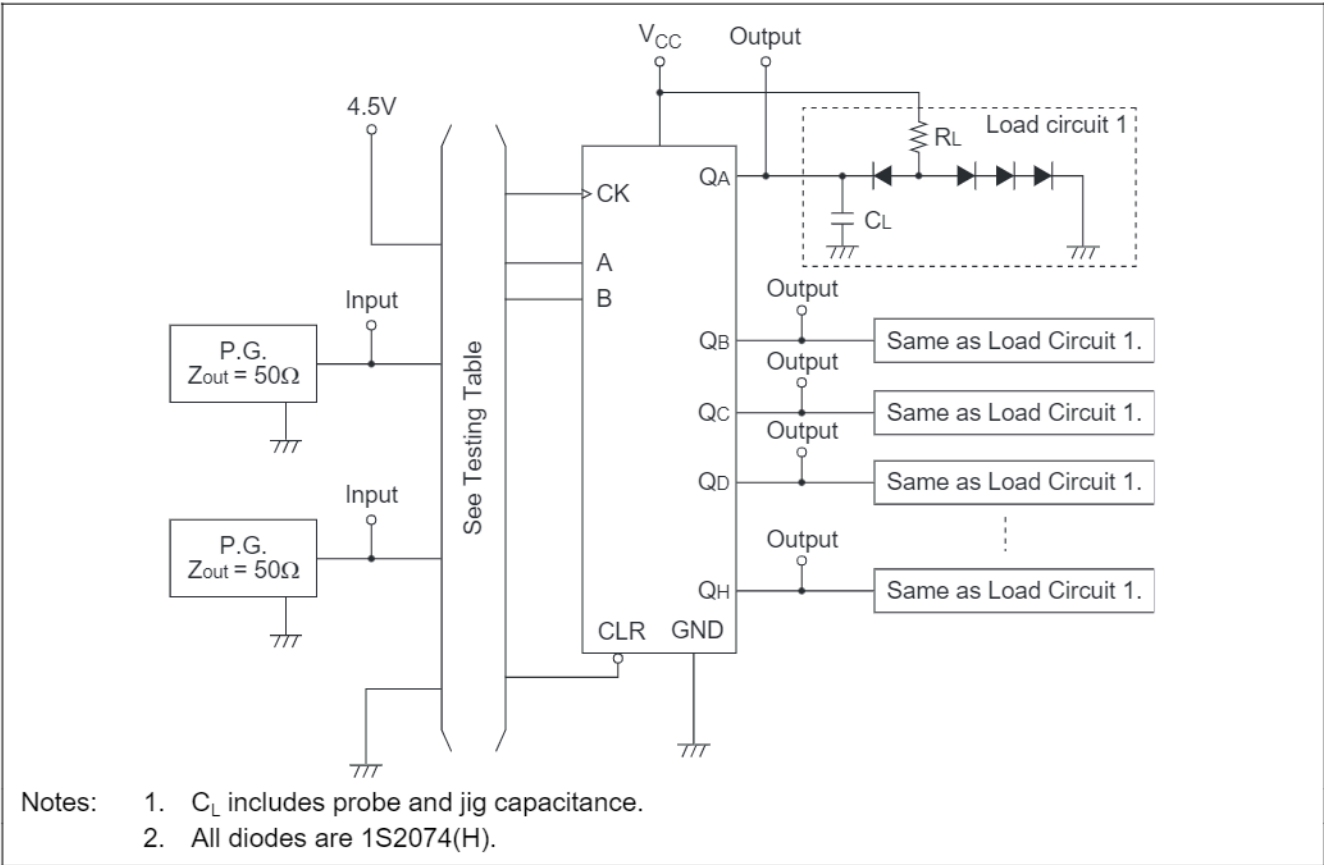
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f _{max}			25	36	—	MHz	C _L = 15 pF, R _L = 2 k Ω
Propagation delay time	t _{PHL}	Clear	Q	—	24	36	ns	
	t _{PLH}	Clock	Q	—	17	27	ns	
	t _{PHL}	Clock	Q	—	21	32	ns	

Typical Clear, Shift, and Clear Sequences



Testing Method

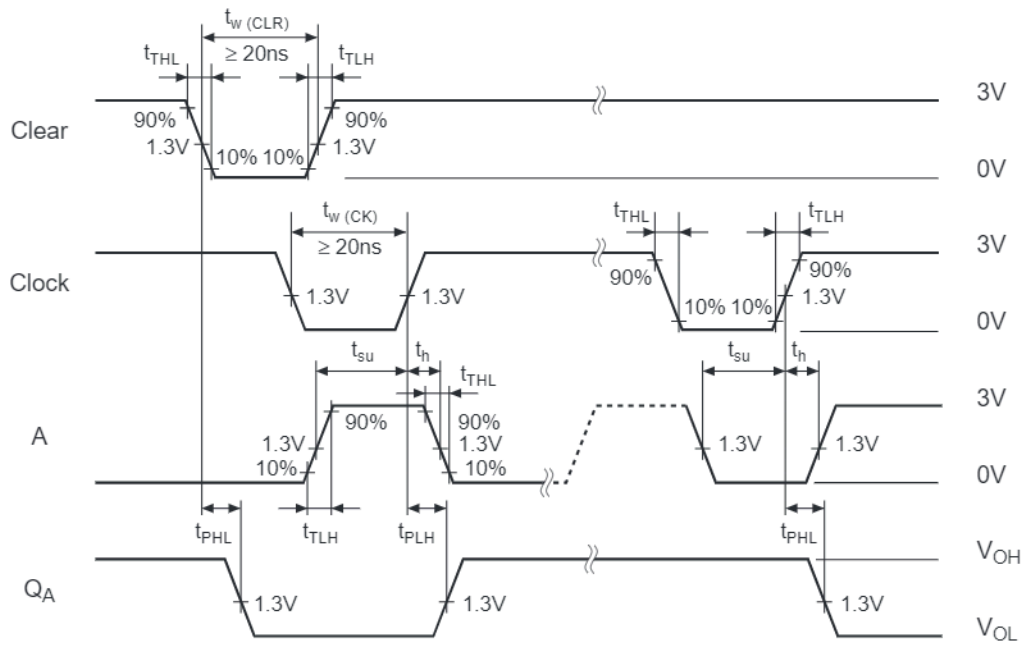
Test Circuit



Testing Table

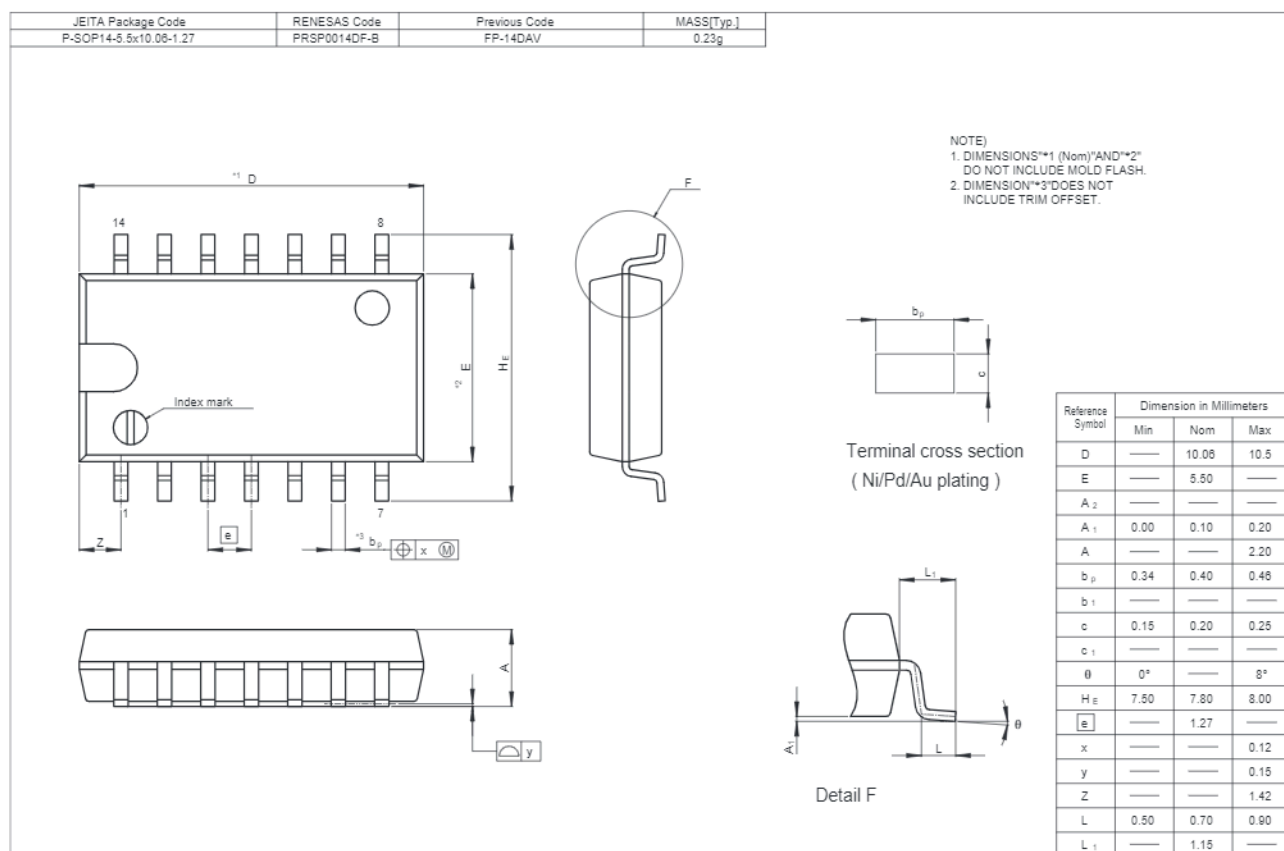
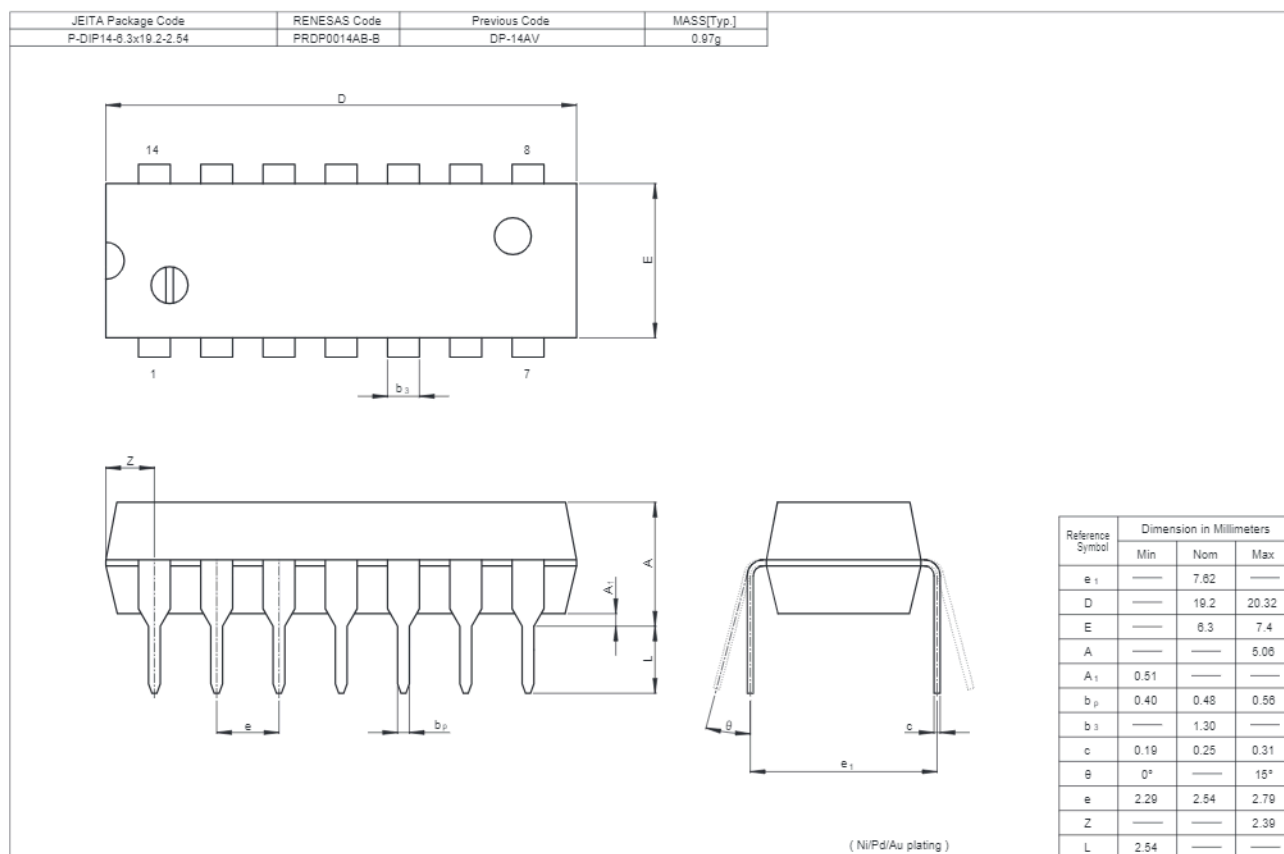
Item	From input to output	Inputs				Outputs							
		CLR	CK	A	B	QA	QB	QC	QD	QE	QF	QG	QH
f_{max}		4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PLH}	Clear→Q	IN	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
t_{PHL}	CK→Q	4.5V	IN	IN	4.5V	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT

Waveform

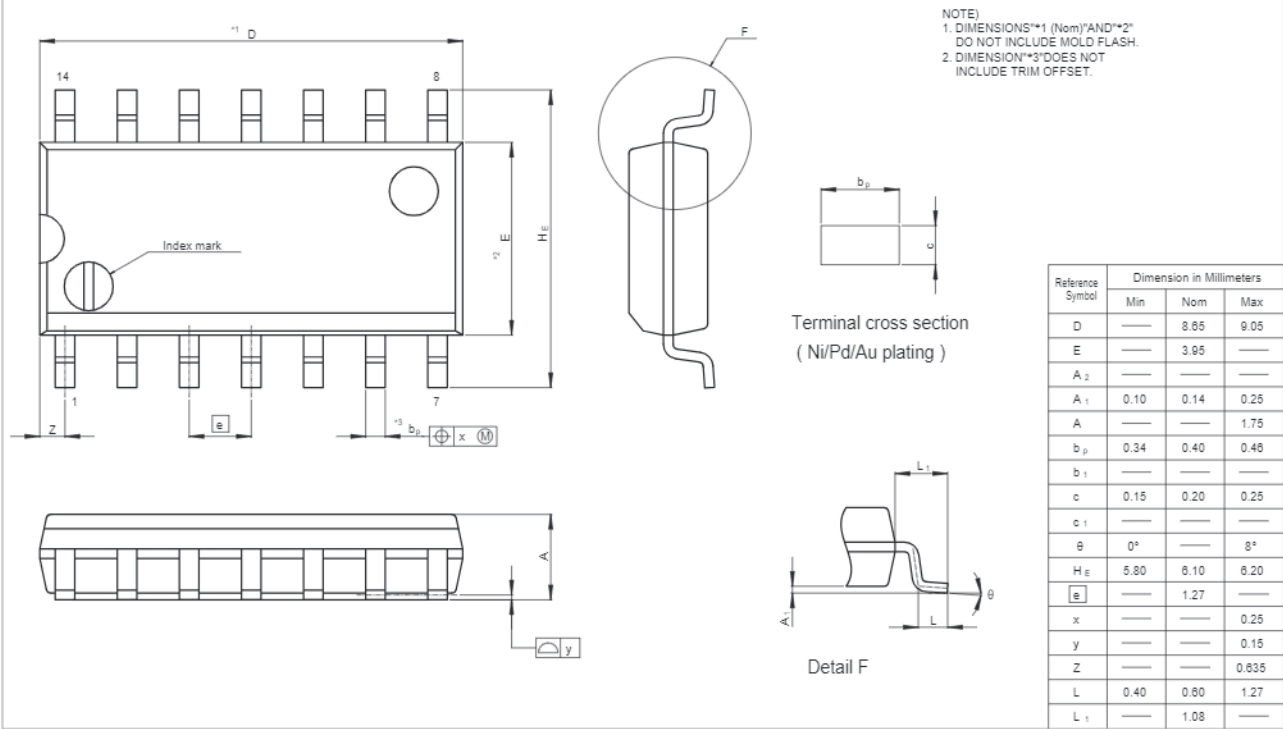


- Notes:
1. Input pulse; $t_{\text{TLH}} \leq 15\text{ ns}$, $t_{\text{THL}} \leq 6\text{ ns}$, PRR = 1 MHz, (Clock, Clear), PRR = 500 kHz (A or B)
 2. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the timing chart.

Package Dimensions



JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-3.95x8.85-1.27	PRSP0014DE-A	FP-14DNU	0.13g



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