intersil

ICM7555, ICM7556

November 1996

General Purpose Timers

Features

- Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556
- Low Supply Current
  - ICM7555. . . . . 60μA
  - ICM7556. . . . . 120μA
- Extremely Low Input Currents 20pA
- High Speed Operation 1MHz
- Guaranteed Supply Voltage Range . . . . 2V to 18V
- Temperature Stability . . . . 0.005%/°C at 25°C
- Normal Reset Function - No Crowbarring of Supply During Output Transition
- Can be Used with Higher Impedance Timing Elements than Regular 555/6 for Longer RC Time Constants
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Output Source/Sink Driver can Drive TTL/CMOS
- Outputs have Very Low Offsets, HI and LO

Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

Description

The ICM7555 and ICM7556 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555 and ICM7556 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

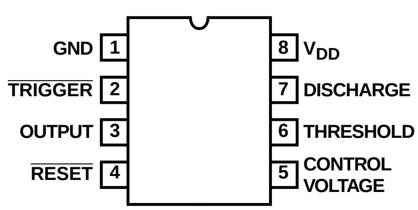
Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7555CBA (7555CBA)	0 to 70	8 Ld SOIC	M18.5
ICM7555IBA (7555IBA)	-25 to 85	8 Ld SOIC	M18.5
ICM7555IPA	-25 to 85	8 Ld PDIP	E8.3
ICM7555ITV	-25 to 85	8 Pin Metal Can	T8.C
ICM7555MTV (Note)	-55 to 125	8 Pin Metal Can	T8.C
ICM7556IPD	-25 to 85	14 Ld PDIP	E14.3
ICM7556MJD (Note)	-55 to 125	14 Ld CERDIP	F14.3

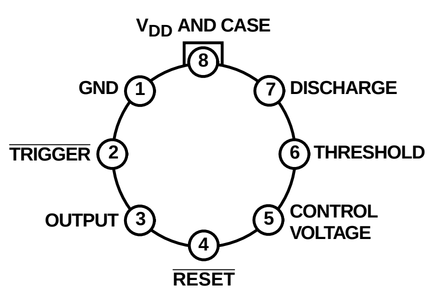
NOTE: Add /883B to part number if 883B processing is desired.

Pinouts

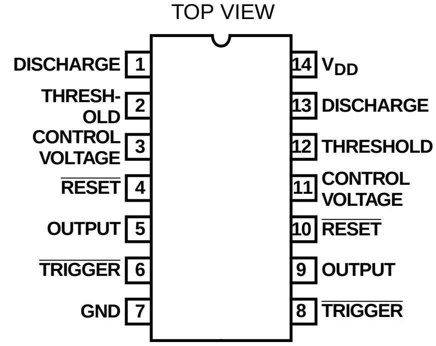
ICM7555 (PDIP, SOIC)
TOP VIEW



ICM7555 (METAL CAN)
TOP VIEW



ICM7556 (PDIP, CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number 2867.2

Absolute Maximum Ratings

Supply Voltage . . . . +18V
Input Voltage
Trigger, Control Voltage, Threshold,
Reset (Note 1). . . . . .V+ +0.3V to GND -0.3V
Output Current 100mA

Operating Conditions

Temperature Range
ICM7555C. . . . . 0^oC to 70^oC
ICM7555I, ICM7556I. . . . . -25^oC to 85^oC
ICM7555M, ICM7556M. . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^oC/W)	θ_{JC} (^oC/W)
CERDIP Package	80	24
Metal Can Package	165	80
14 Lead PDIP Package	115	N/A
8 Lead PDIP Package	110	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Hermetic Package) . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V- -0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple supply systems, the supply of the ICM7555/6 must be turned on first.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Applies to ICM7555 and ICM7556, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		$T_A = 25^oC$ MIN	TYP	MAX	(NOTE 4) -55^oC TO 125^oC MIN	TYP	MAX	UNITS
Static Supply Current	I_{DD}	ICM7555	V_{DD} = 5V	-	40	200	-	-	300	µA
			V_{DD} = 15V	-	60	300	-	-	300	µA
		ICM7556	V_{DD} = 5V	-	80	400	-	-	600	µA
			V_{DD} = 15V	-	120	600	-	-	600	µA
Monostable Timing Accuracy		R_A = 10K, C = 0.1µF, V_{DD} = 5V		-	2	-	-	-	-	%
				-	-	-	858	-	1161	µs
Drift with Temperature (Note 3)		V_{DD} = 5V		-	-	-	-	150	-	ppm/^oC
		V_{DD} = 10V		-	-	-	-	200	-	ppm/^oC
		V_{DD} = 15V		-	-	-	-	250	-	ppm/^oC
Drift with Supply (Note 3)		V_{DD} = 5V to 15V		-	0.5	-	-	0.5	-	%/V
Astable Timing Accuracy		$R_A = R_B$ = 10K, C = 0.1µF, V_{DD} = 5V		-	2	-	-	-	-	%
				-	-	-	1717	-	2323	µs
Drift with Temperature (Note 3)		V_{DD} = 5V		-	-	-	-	150	-	ppm/^oC
		V_{DD} = 10V		-	-	-	-	200	-	ppm/^oC
		V_{DD} = 15V		-	-	-	-	250	-	ppm/^oC
Drift with Supply (Note 3)		V_{DD} = 5V to 15V		-	0.5	-	-	0.5	-	%/V
Threshold Voltage	V_{TH}	V_{DD} = 15V		62	67	71	61	-	72	% V_{DD}
Trigger Voltage	V_{TRIG}	V_{DD} = 15V		28	32	36	27	-	37	% V_{DD}
Trigger Current	I_{TRIG}	V_{DD} = 15V		-	-	10	-	-	50	nA
Threshold Current	I_{TH}	V_{DD} = 15V		-	-	10	-	-	50	nA
Control Voltage	V_{CV}	V_{DD} = 15V		62	67	71	61	-	72	% V_{DD}
Reset Voltage	V_{RST}	V_{DD} = 2V to 15V		0.4	-	1.0	0.2	-	1.2	V
Reset Current	I_{RST}	V_{DD} = 15V		-	-	10	-	-	50	nA

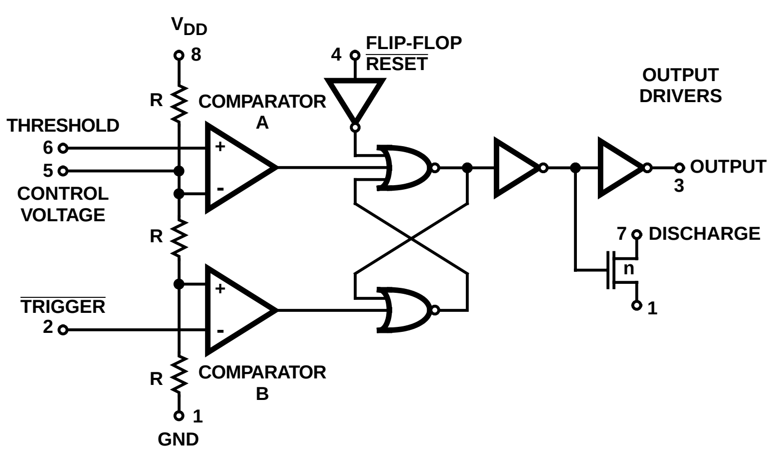
Electrical Specifications Applies to ICM7555 and ICM7556, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A = 25^oC$			(NOTE 4) -55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Discharge Leakage	I_{DIS}	V_{DD} = 15V	-	-	10	-	-	50	nA
Output Voltage	V_{OL}	V_{DD} = 15V, I_{SINK} = 20mA	-	0.4	1.0	-	-	1.25	V
		V_{DD} = 5V, I_{SINK} = 3.2mA	-	0.2	0.4	-	-	0.5	V
	V_{OH}	V_{DD} = 15V, I_{SOURCE} = 0.8mA	14.3	14.6	-	14.2	-	-	V
		V_{DD} = 5V, I_{SOURCE} = 0.8mA	4.0	4.3	-	3.8	-	-	V
Discharge Output Voltage	V_{DIS}	V_{DD} = 5V, I_{SINK} = 15mA	-	0.2	0.4	-	-	0.6	V
		V_{DD} = 15V, I_{SINK} = 15mA	-	-	-	-	-	0.4	V
Supply Voltage (Note 3)	V_{DD}	Functional Operation	2.0	-	18.0	3.0	-	16.0	V
Output Rise Time (Note 3)	t_R	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Output Fall Time (Note 3)	t_F	R_L = 10M, C_L = 10pF, V_{DD} = 5V	-	75	-	-	-	-	ns
Oscillator Frequency (Note 3)	f_{MAX}	V_{DD} = 5V, R_A = 470Ω, R_B = 270Ω, C = 200pF	-	1	-	-	-	-	MHz

NOTES:

3. These parameters are based upon characterization data and are not tested.
4. Applies only to military temperature range product (M suffix).

Functional Diagram



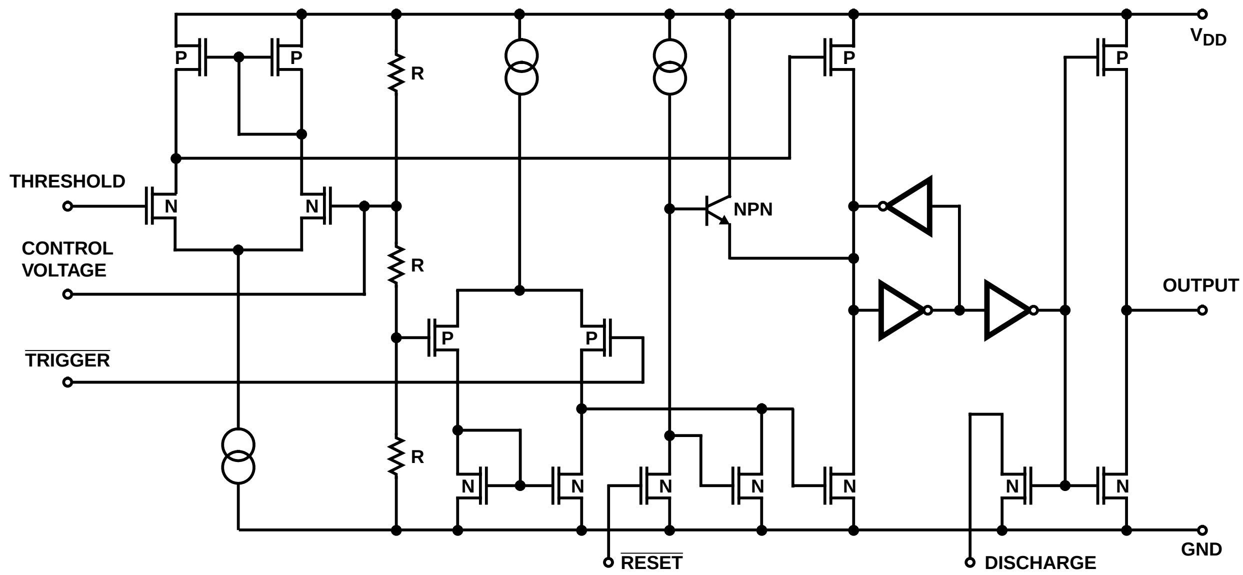
NOTE: This functional diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ±20% (Typ)

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
Don't Care	Don't Care	Low	Low	On
$>^2/_3$(V+)	$>^1/_3$(V+)	High	Low	On
$<^2/_3$(V+)	$>^1/_3$(V+)	High	Stable	Stable
Don't Care	$<^1/_3$(V+)	High	High	Off

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Schematic Diagram



R = 100kΩ ±20% (TYP)

Application Information

General

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 1.

The ICM7555/6 produces supply current spikes of only 2mA - 3mA instead of 300mA - 400mA and supply decoupling is normally not necessary. Also, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

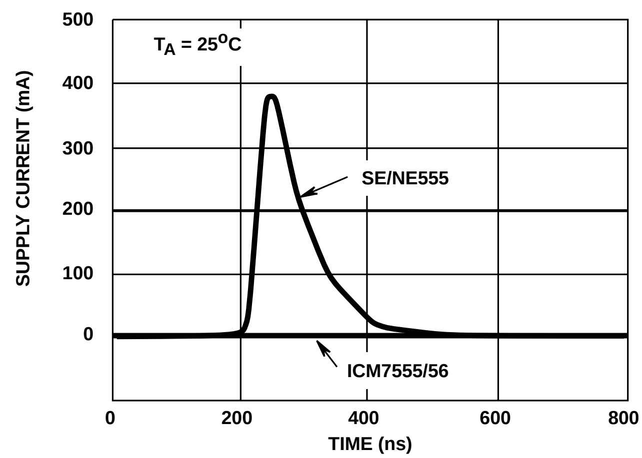


FIGURE 1. SUPPLY CURRENT TRANSIENT COMPARED WITH A STANDARD BIPOLAR 555 DURING AN OUTPUT TRANSITION

Power Supply Considerations

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply current can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 2 and 3.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more the ICM7555/6 will drive at least 2 standard TTL loads.

Astable Operation

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 2A. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5V to +15V.

$$f = \frac{1}{1.4\ RC}$$

The timer can also be connected as shown in Figure 2B. In this circuit, the frequency is:

$$f = 1.44/(R_A + 2R_B)C$$

The duty cycle is controlled by the values of R_A and R_B, by the equation:

$$D = (R_A + R_B)/(R_A + 2R_B)$$

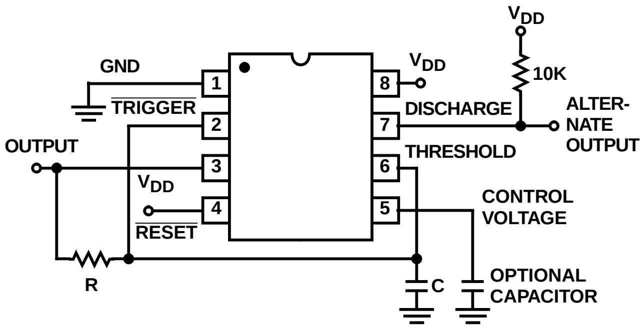


FIGURE 2A. ASTABLE OPERATION

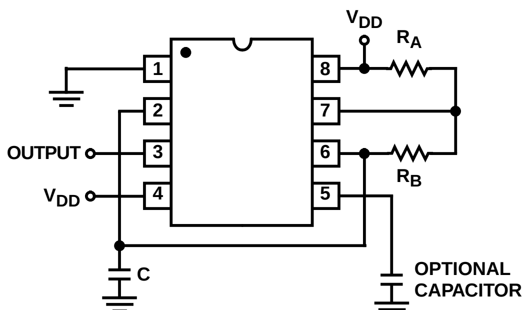


FIGURE 2B. ALTERNATE ASTABLE CONFIGURATION

Monostable Operation

In this mode of operation, the timer functions as a one-shot, see Figure 3. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip-flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant t = R_AC. When the voltage across the capacitor equals $^2/_3$ V+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

$$t_{OUTPUT} = -\ln(^1/_3)\ R_AC = 1.1R_AC$$

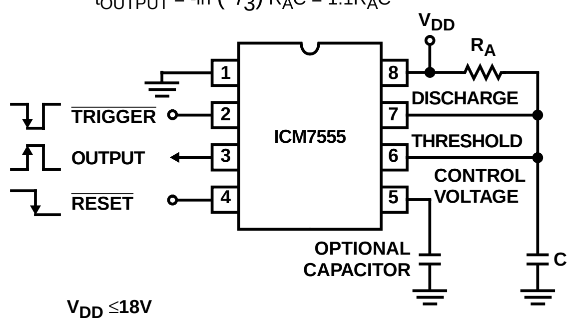


FIGURE 3. MONOSTABLE OPERATION

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e., 0.6V to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

Typical Performance Curves

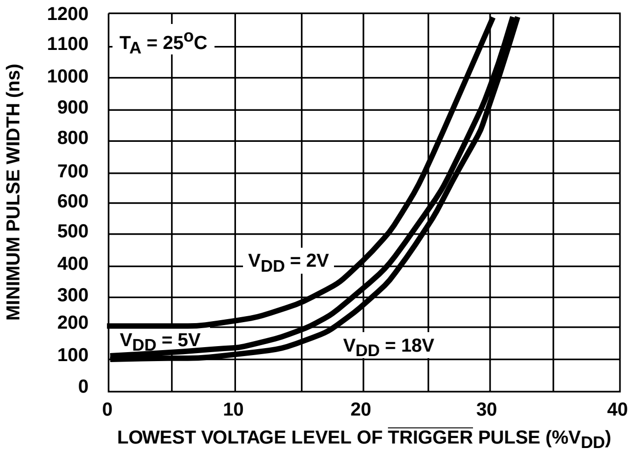


FIGURE 4. MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

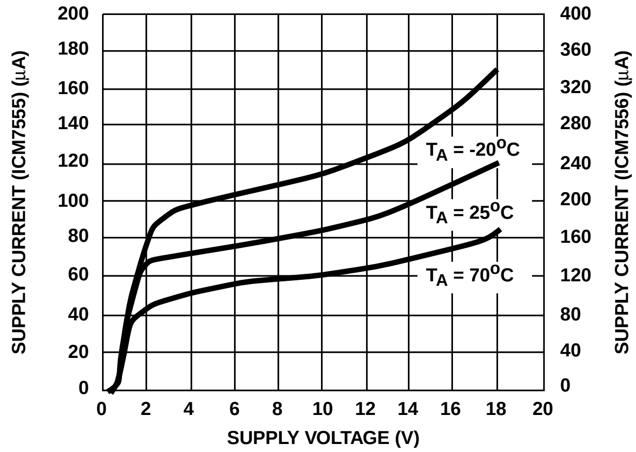


FIGURE 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

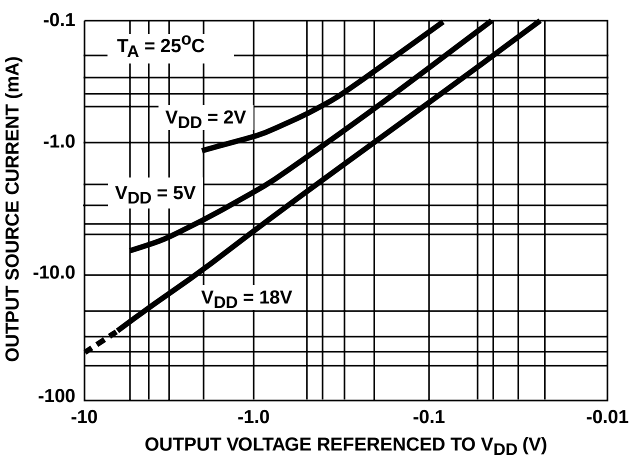


FIGURE 6. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

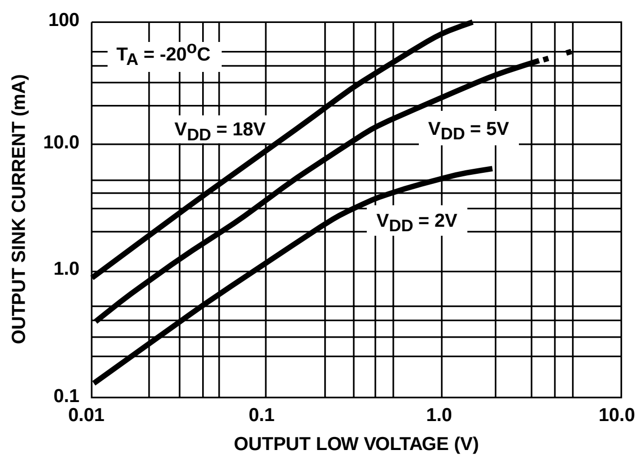


FIGURE 7. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

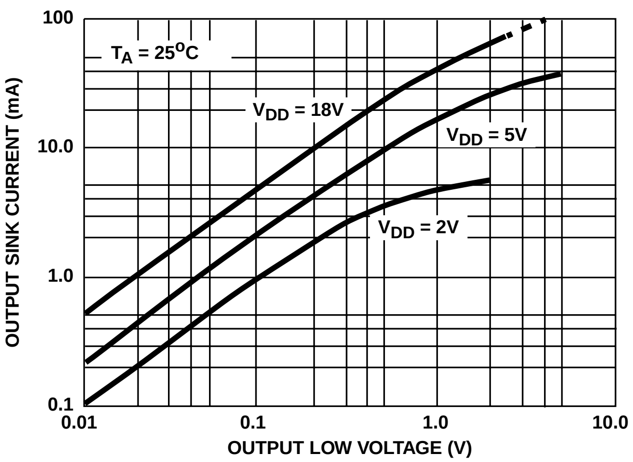


FIGURE 8. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

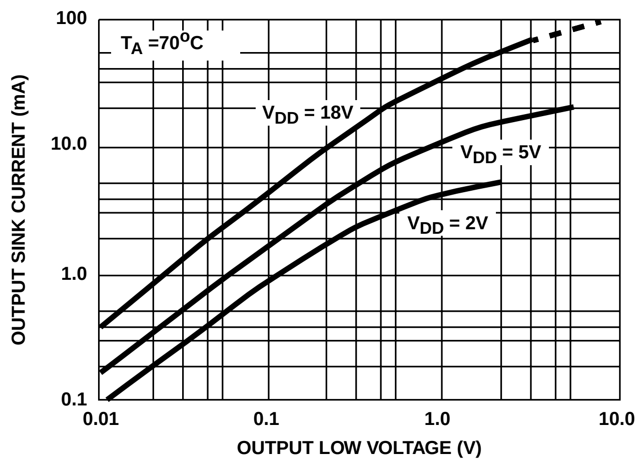


FIGURE 9. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

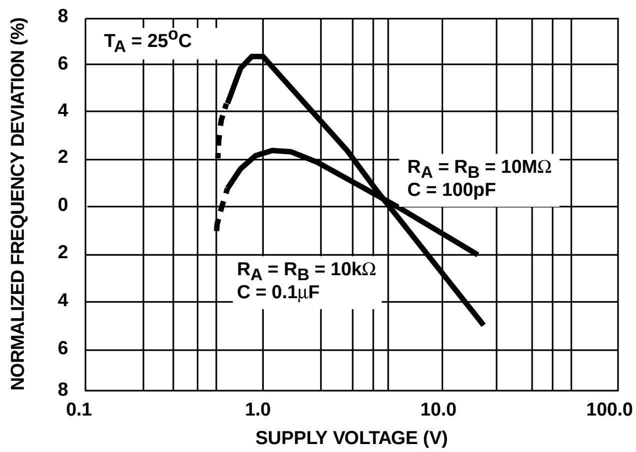


FIGURE 10. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs SUPPLY VOLTAGE

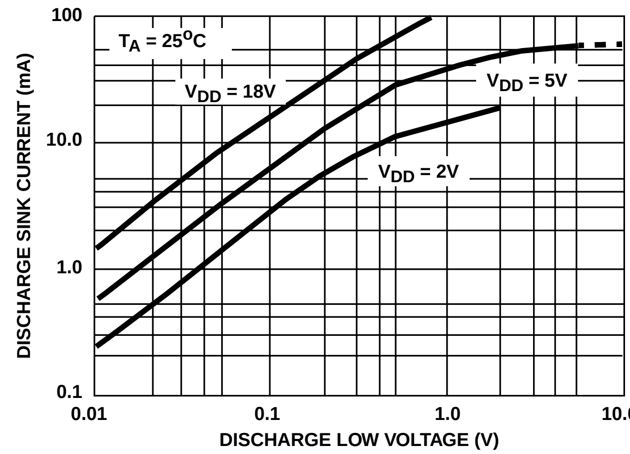


FIGURE 11. DISCHARGE OUTPUT CURRENT vs DISCHARGE OUTPUT VOLTAGE

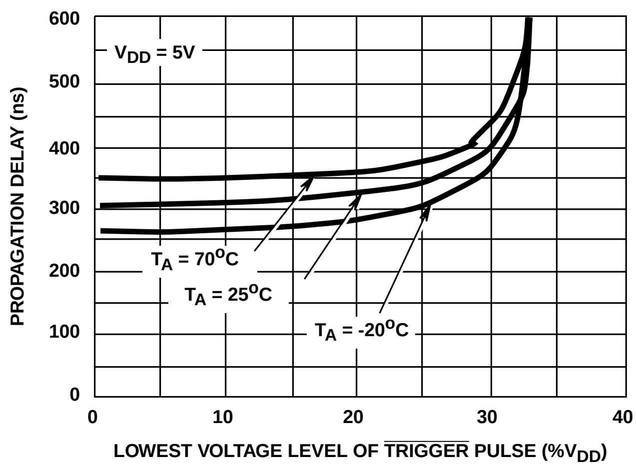


FIGURE 12. PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE

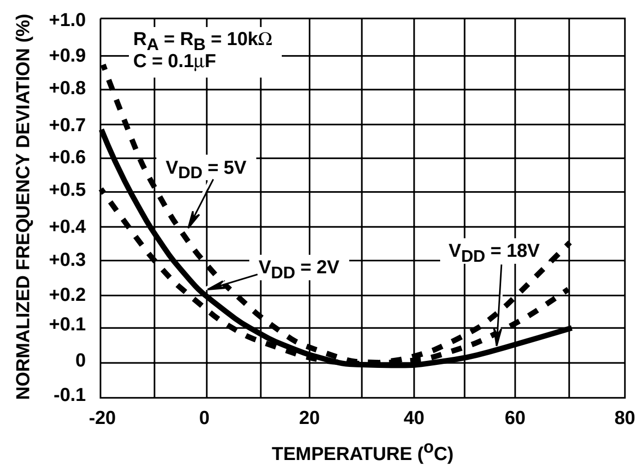


FIGURE 13. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs TEMPERATURE

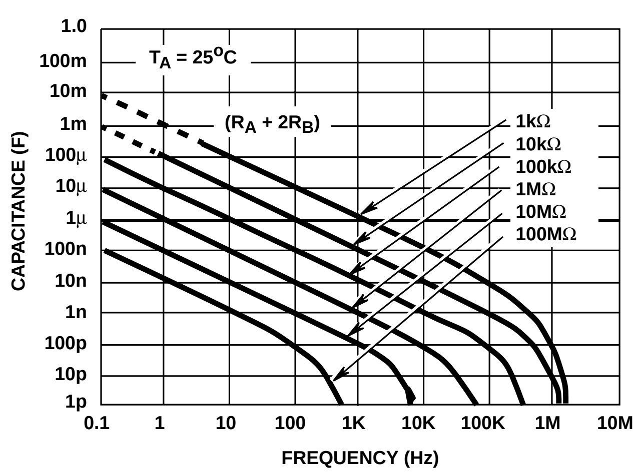


FIGURE 14. FREE RUNNING FREQUENCY vs R_A, R_B AND C

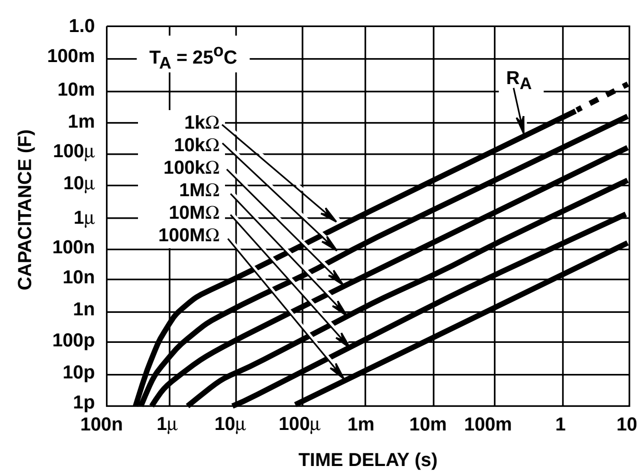


FIGURE 15. TIME DELAY IN THE MONOSTABLE MODE vs R_A AND C

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029