

International IOR Rectifier

SMPS MOSFET

IRFP15N60L

PD - 94415A

Applications

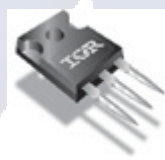
- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ typ.	T_{rr} typ.	I_D
600V	385m Ω	130ns	15A



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	15	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	9.7	
I_{DM}	Pulsed Drain Current ①	60	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	280	W
	Linear Derating Factor	2.3	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	11	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	15	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	60		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 15\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	130	200	ns	$T_J = 25^\circ\text{C}$, $I_F = 15\text{A}$
		—	240	360		$T_J = 125^\circ\text{C}$, $di/dt = 100\text{A}/\mu\text{s}$ ④
Q_{rr}	Reverse Recovery Charge	—	450	670	nC	$T_J = 25^\circ\text{C}$, $I_S = 15\text{A}$, $V_{GS} = 0\text{V}$ ④
		—	1080	1620		$T_J = 125^\circ\text{C}$, $di/dt = 100\text{A}/\mu\text{s}$ ④
I_{RRM}	Reverse Recovery Current	—	5.8	8.7	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.39	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	385	460	m Ω	$V_{GS} = 10V, I_D = 9.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$
R_G	Internal Gate Resistance	—	0.79	—	Ω	$f = 1MHz$, open drain

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	8.3	—	—	S	$V_{DS} = 50V, I_D = 9.0A$
Q_g	Total Gate Charge	—	—	100	nC	$I_D = 15A$ $V_{DS} = 480V$ $V_{GS} = 10V$, See Fig. 7 & 15 ④
Q_{gs}	Gate-to-Source Charge	—	—	30	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	46	nC	
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	$V_{DD} = 300V$ $I_D = 15A$ $R_G = 1.8\Omega$ $V_{GS} = 10V$, See Fig. 11a & 11b ④
t_r	Rise Time	—	44	—		
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		
t_f	Fall Time	—	5.5	—		
C_{iss}	Input Capacitance	—	2720	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	260	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	20	—		$f = 1.0MHz$, See Fig. 5
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	120	—		$V_{GS} = 0V, V_{DS} = 0V$ to $480V$ ⑤
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	100	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	320	mJ
I_{AR}	Avalanche Current ①	—	15	A
E_{AR}	Repetitive Avalanche Energy ①	—	28	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.44	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	40	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 2.9mH$, $R_G = 25\Omega$, $I_{AS} = 15A$, $dv/dt = 10V/ns$. (See Figure 12a)
- ③ $I_{SD} \leq 15A$, $di/dt \leq 650A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

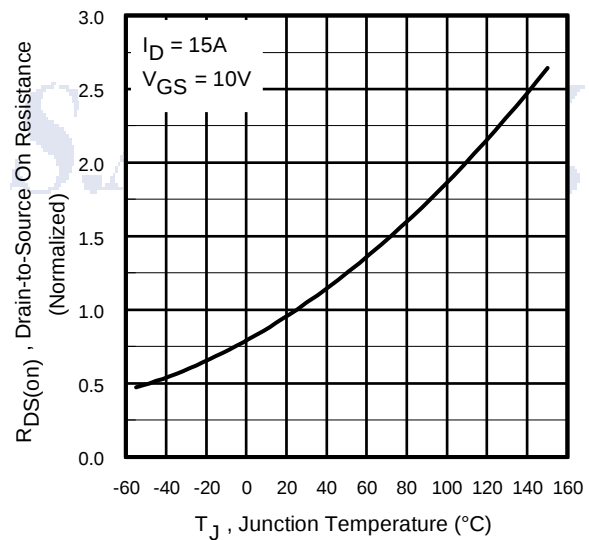
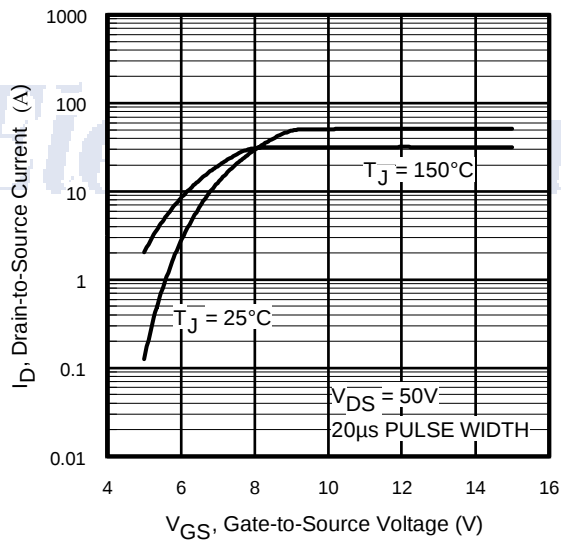
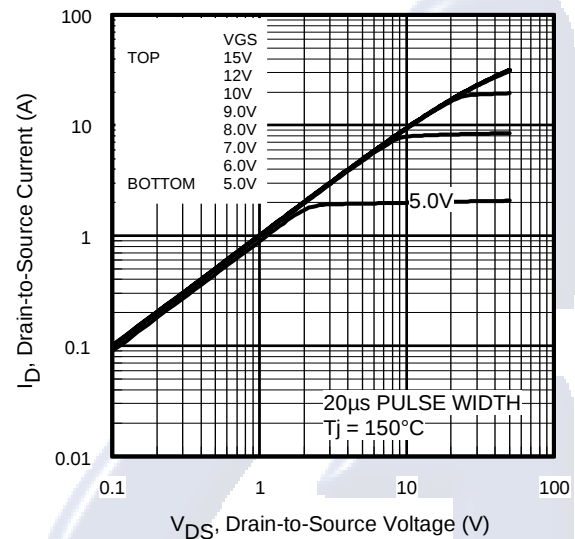
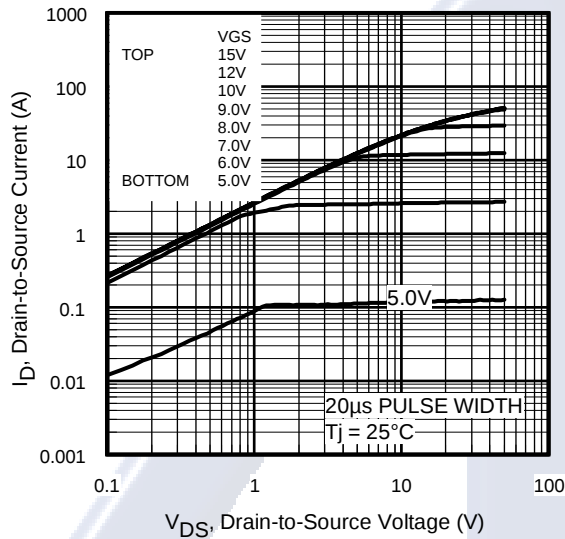
④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to $80\% V_{DSS}$.
 $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to $80\% V_{DSS}$.

⑥ R_θ is measured at T_J approximately 90°C

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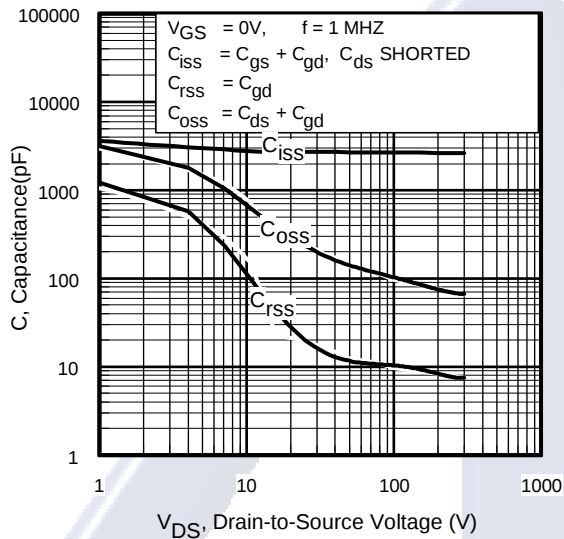


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

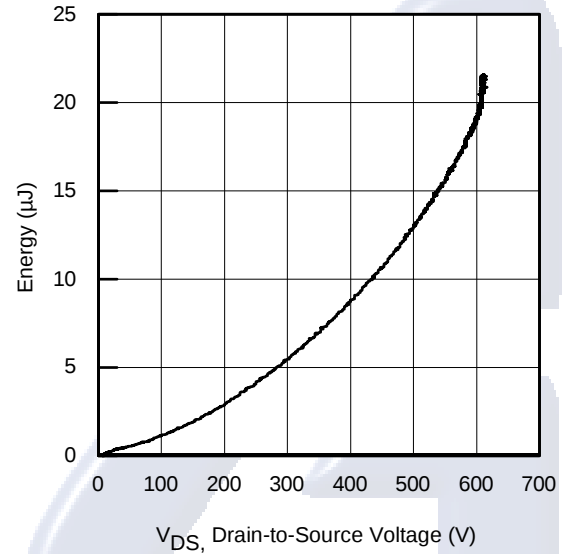


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

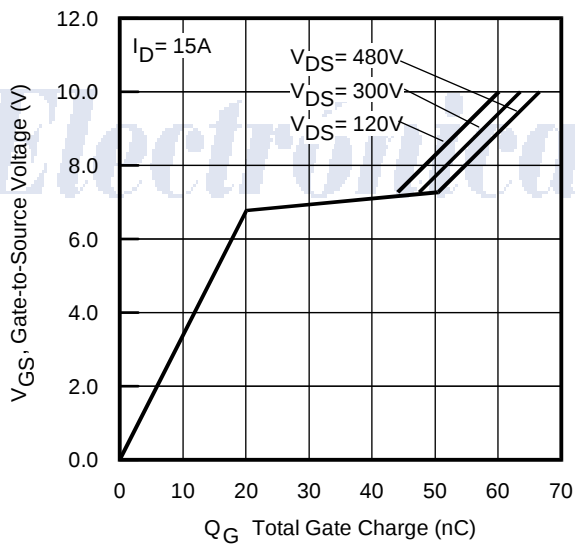


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

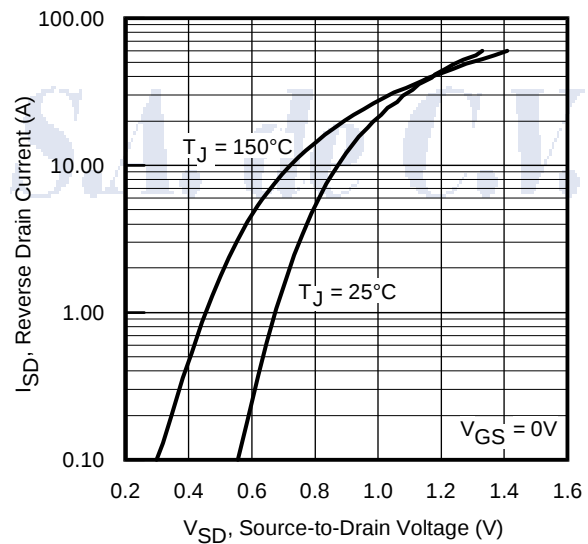


Fig 8. Typical Source-Drain Diode Forward Voltage

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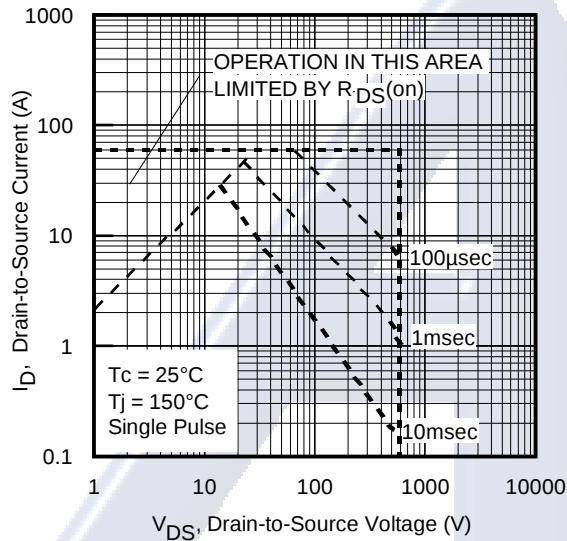


Fig 9. Maximum Safe Operating Area

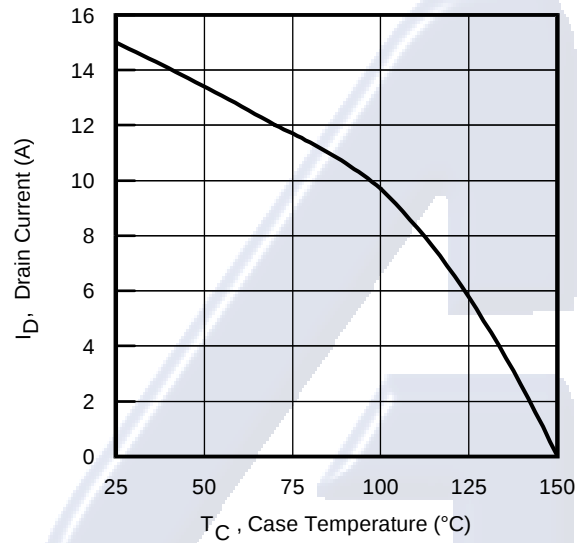


Fig 10. Maximum Drain Current vs. Case Temperature

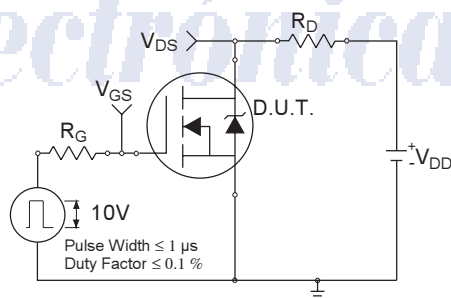


Fig 11a. Switching Time Test Circuit

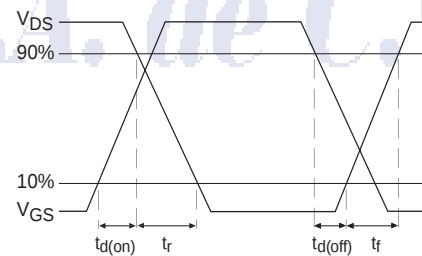


Fig 11b. Switching Time Waveforms

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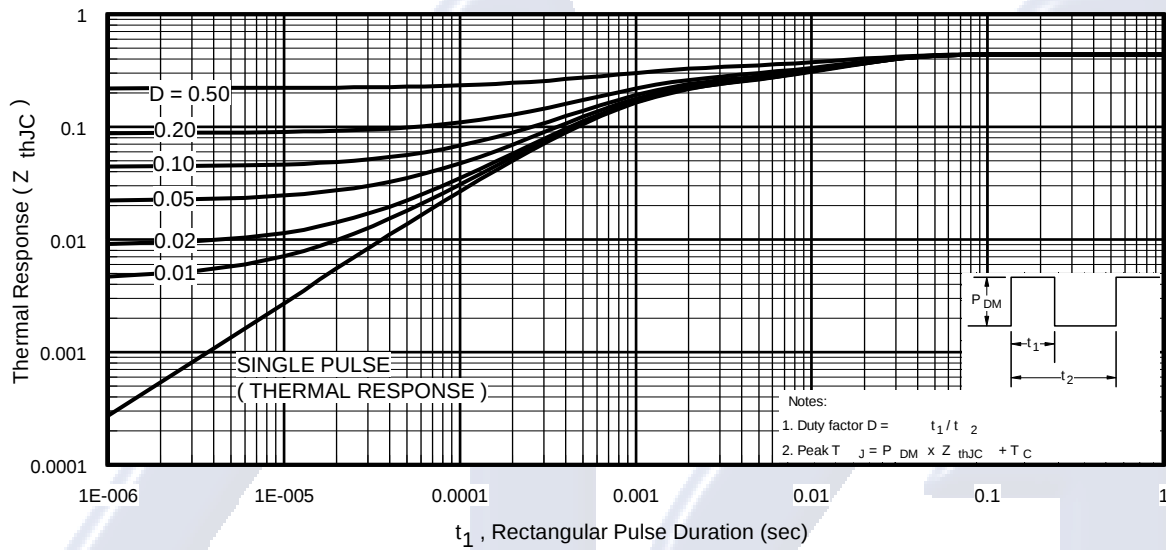
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Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Case

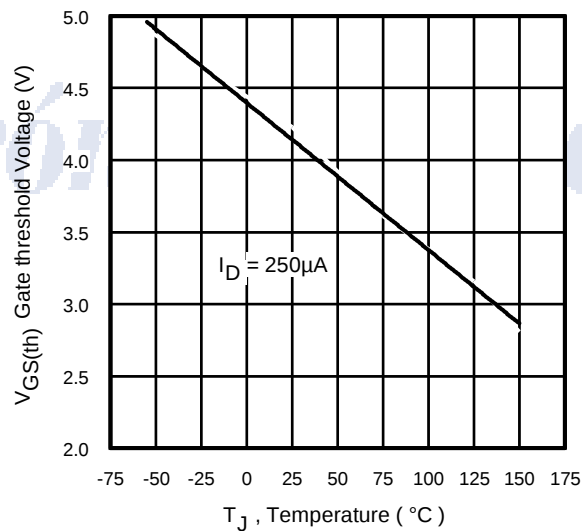


Fig 13. Threshold Voltage vs. Temperature

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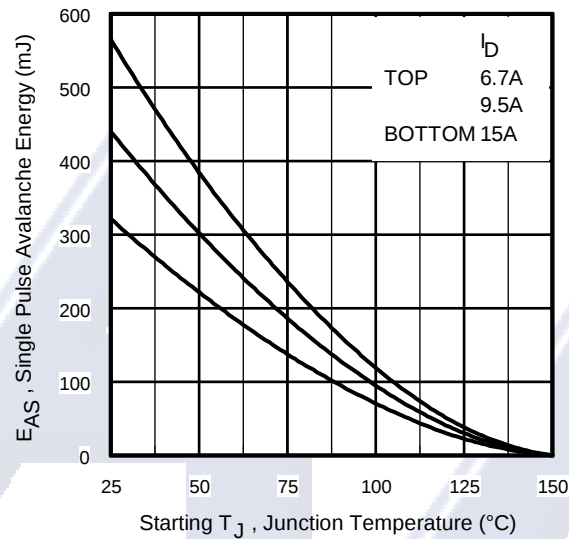


Fig 14a. Maximum Avalanche Energy vs. Drain Current

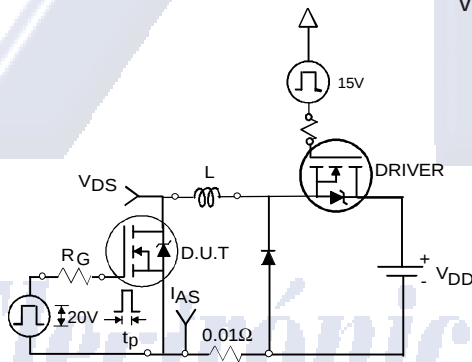


Fig 14b. Unclamped Inductive Test Circuit

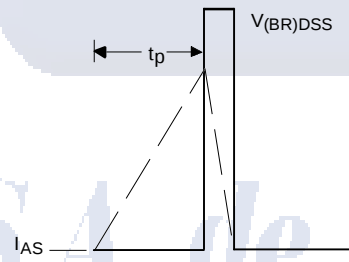


Fig 14c. Unclamped Inductive Waveforms

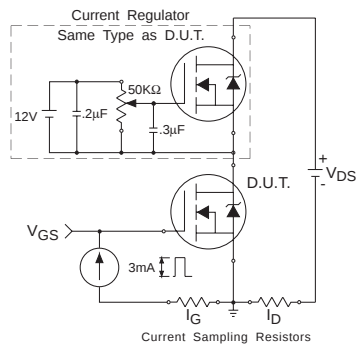


Fig 15a. Gate Charge Test Circuit

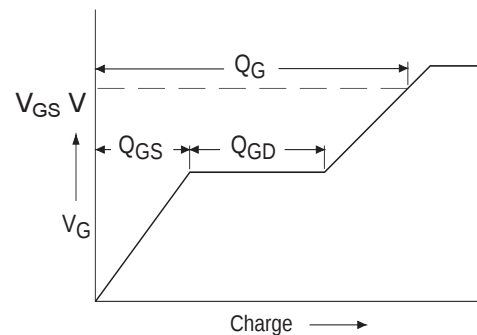


Fig 15b. Basic Gate Charge Waveform

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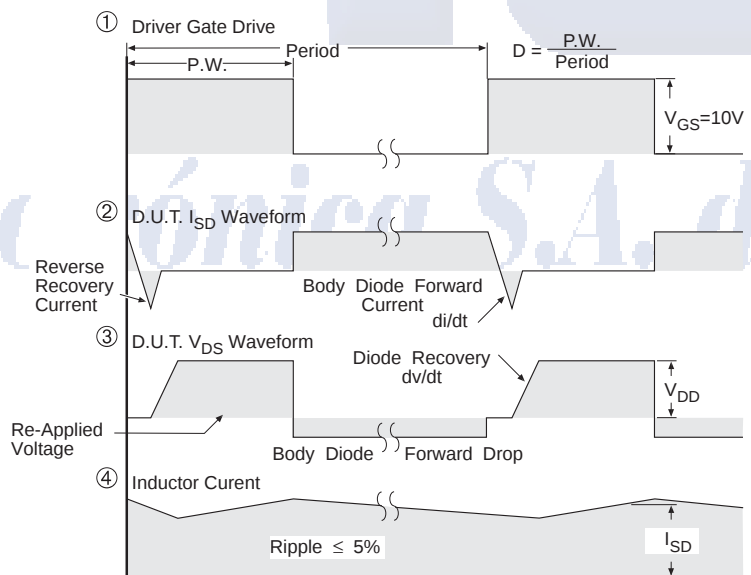
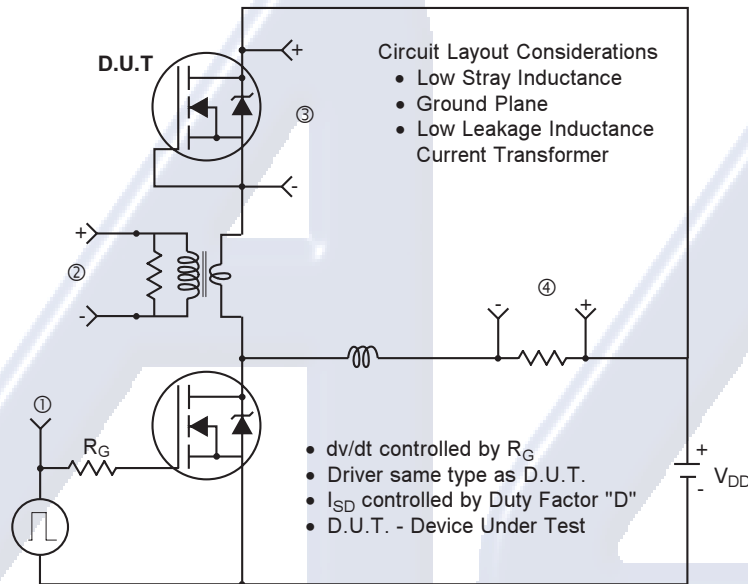
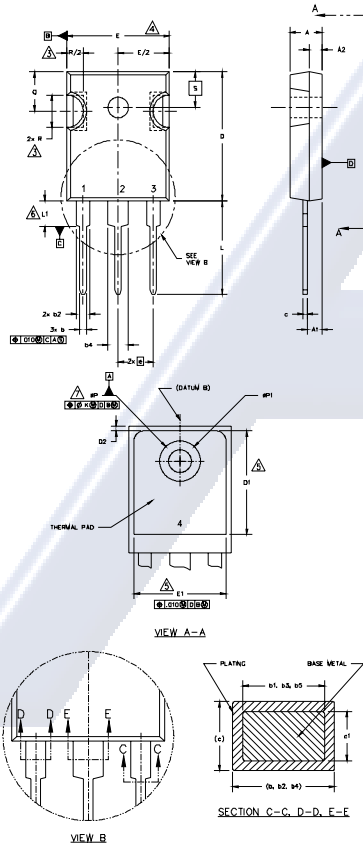
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RectifierPeak Diode Recovery dv/dt Test Circuit* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. For N-Channel HEXFET® Power MOSFETs

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
 2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
 3. CONTOUR OF SLOT OPTIONAL.
 4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
 6. LEAD FINISH UNCONTROLLED IN L1.
 7. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91].
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION C.

SYMBOL	DIMENSIONS		NOTES	
	INCHES	MILLIMETERS		
A	.185	.209	4.65	5.31
A1	.087	.102	2.21	2.59
A2	.059	.098	1.50	2.49
b	.039	.055	0.99	1.40
b1	.039	.053	0.99	1.35
b2	.065	.094	1.65	2.39
b3	.065	.092	1.65	2.37
b4	.102	.135	2.59	3.43
b5	.102	.133	2.59	3.38
c	.015	.034	0.38	0.86
c1	.015	.030	0.38	0.76
D	.776	.815	19.71	20.70
D1	.515	—	13.08	—
D2	.020	.030	0.51	0.76
E	.602	.625	15.29	15.87
E1	.540	—	15.72	—
e	.215 BSC	5.46 BSC		
ek	.010	2.54		
L	.559	.634	14.20	16.10
L1	.146	.169	3.71	4.29
N	3	7.62 BSC		
ϕP	.140	.144	3.56	3.66
$\phi P1$	—	.275	—	6.98
Q	.209	.224	5.31	5.69
R	.178	.216	4.52	5.49
S	.217 BSC	5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

IGBTs, CoPACK

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER
- 4 - COLLECTOR

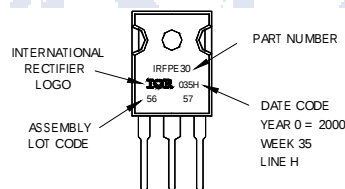
DIODES

- 1 - ANODE/OPEN
- 2 - CATHODE
- 3 - ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line
position indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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