

# IRFR2407PbF IRFU2407PbF

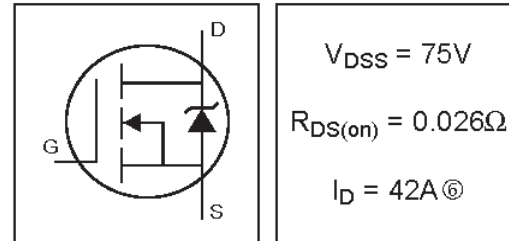
HEXFET® Power MOSFET

- Surface Mount (IRFR2407)
- Straight Lead (IRFU2407)
- Advanced Process Technology
- Dynamic dv/dt Rating
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

### Description

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



$$V_{DS} = 75V$$

$$R_{DS(on)} = 0.026\Omega$$

$$I_D = 42A \text{ @}$$



### Absolute Maximum Ratings

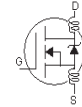
	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	42@	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	29@	
$I_{DM}$	Pulsed Drain Current @	170	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy @	130	mJ
$I_{AR}$	Avalanche Current @	25	A
$E_{AR}$	Repetitive Avalanche Energy @	11	mJ
dv/dt	Peak Diode Recovery dv/dt @	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

### Thermal Resistance

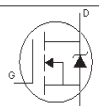
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

\* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

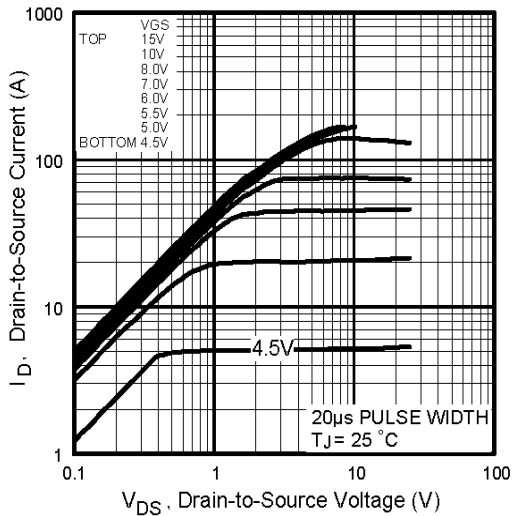
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.078	—	$V/^\circ C$	Reference to $25^\circ C, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0218	0.026	$\Omega$	$V_{GS} = 10V, I_D = 25A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	27	—	—	S	$V_{DS} = 25V, I_D = 25A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 150^\circ C$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	74	110	nC	$I_D = 25A$
$Q_{gs}$	Gate-to-Source Charge	—	13	19		$V_{DS} = 60V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	22	34		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 38V$
$t_r$	Rise Time	—	90	—		$I_D = 25A$
$t_{d(off)}$	Turn-Off Delay Time	—	65	—		$R_G = 6.8\Omega$
$t_f$	Fall Time	—	66	—		$V_{GS} = 10V$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	2400	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	340	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	77	—		$f = 1.0MHz$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	15700	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	220	—		$V_{GS} = 0V, V_{DS} = 60V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	220	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$

## Source-Drain Ratings and Characteristics

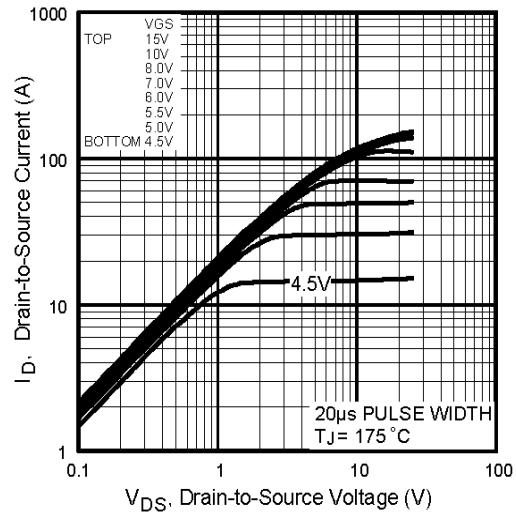
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	42 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	170		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ C, I_S = 25A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ C, I_F = 25A$
$Q_{rr}$	Reverse Recovery Charge	—	400	600	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

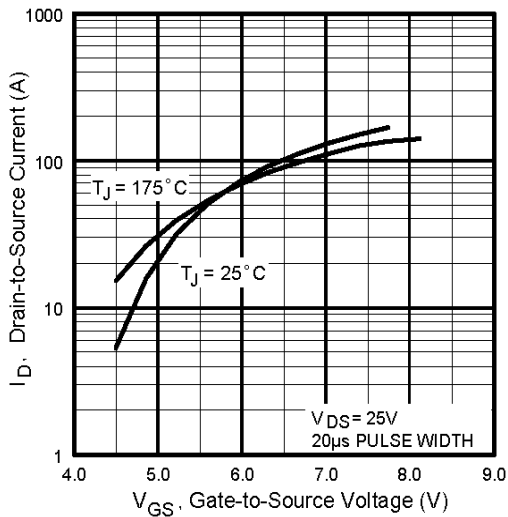
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ C, L = 0.42mH, R_G = 25\Omega, I_{AS} = 25A$ .
- ③  $I_{SD} \leq 25A, di/dt \leq 290A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ C$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A



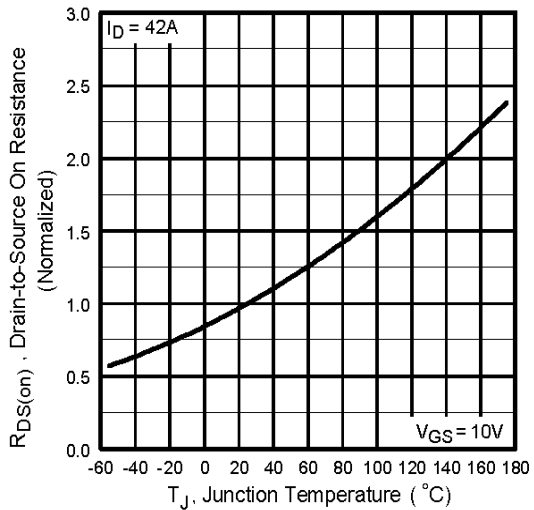
**Fig 1.** Typical Output Characteristics



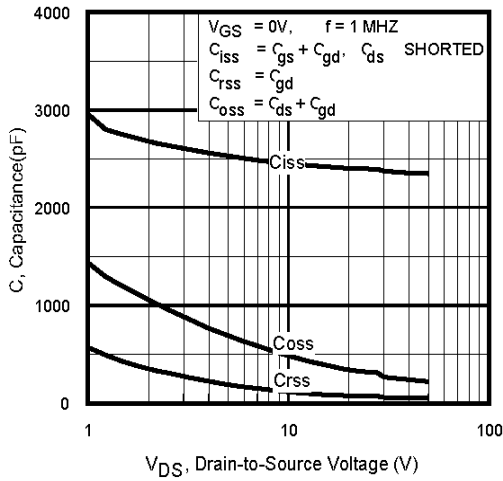
**Fig 2.** Typical Output Characteristics



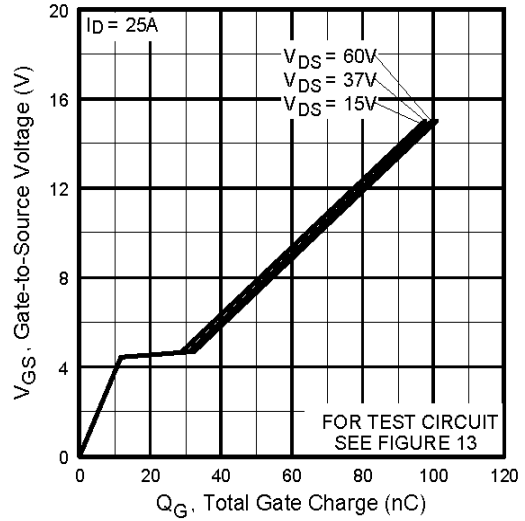
**Fig 3.** Typical Transfer Characteristics



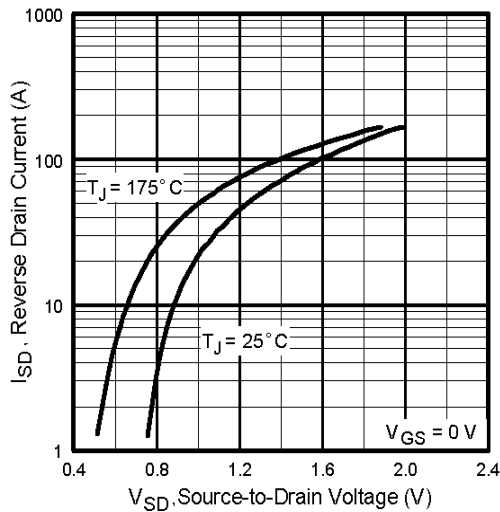
**Fig 4.** Normalized On-Resistance Vs. Temperature



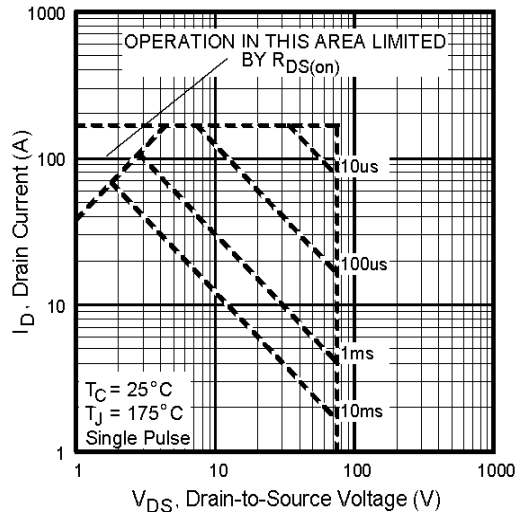
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



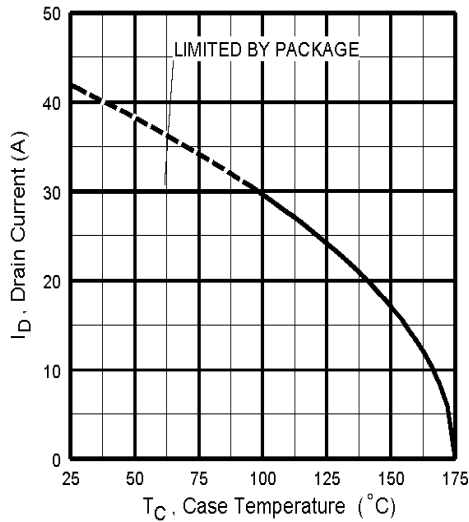
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



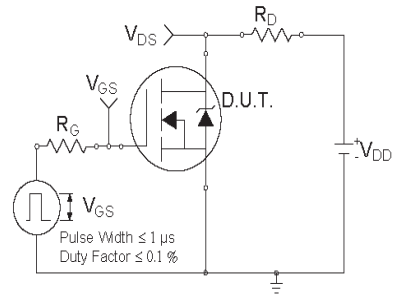
**Fig 7.** Typical Source-Drain Diode Forward Voltage



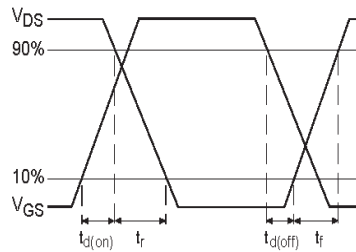
**Fig 8.** Maximum Safe Operating Area



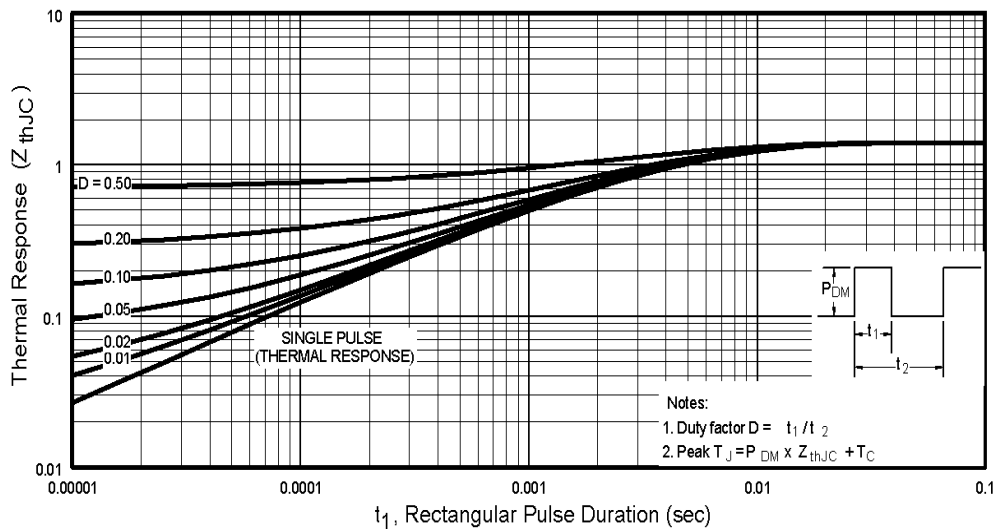
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

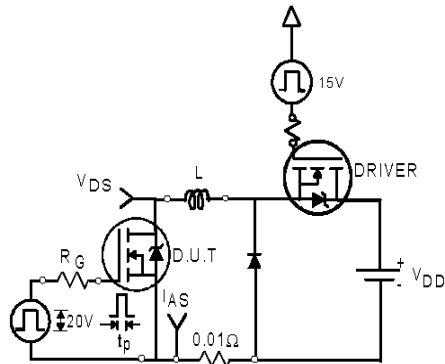


**Fig 10b.** Switching Time Waveforms

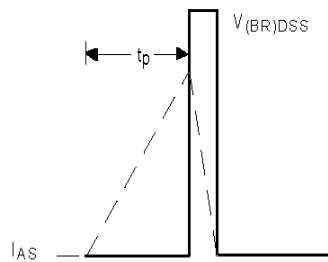


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

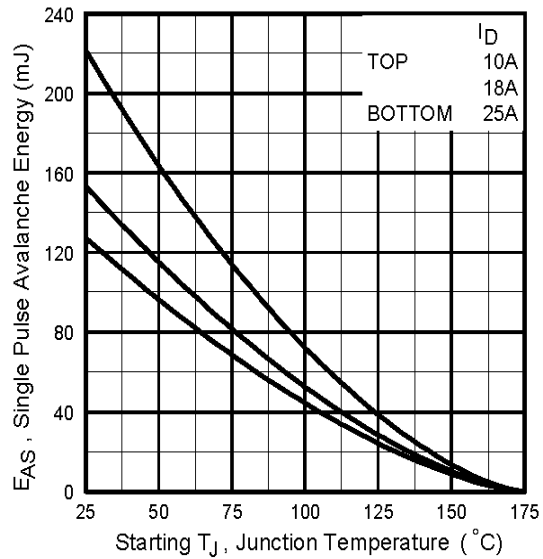
# IRFR/U2407PbF



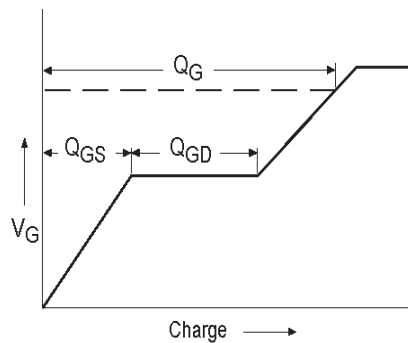
**Fig 12a.** Unclamped Inductive Test Circuit



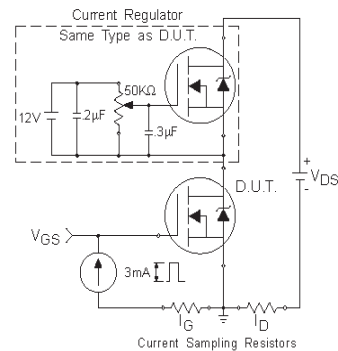
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

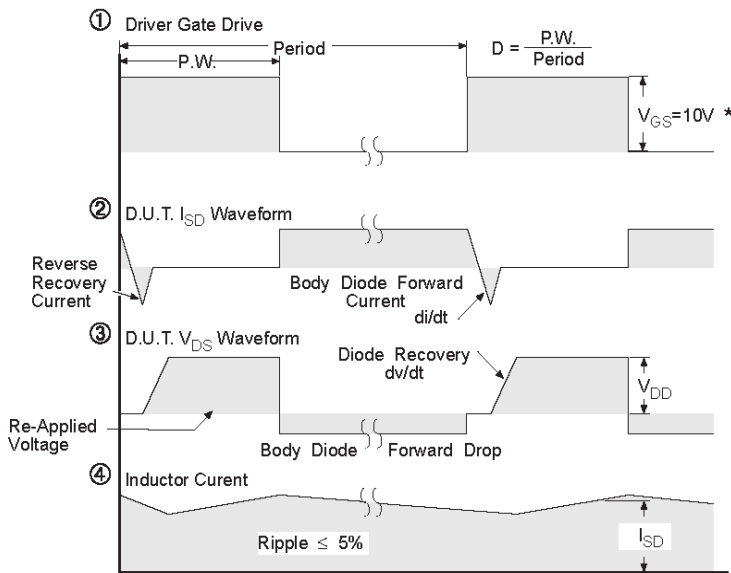
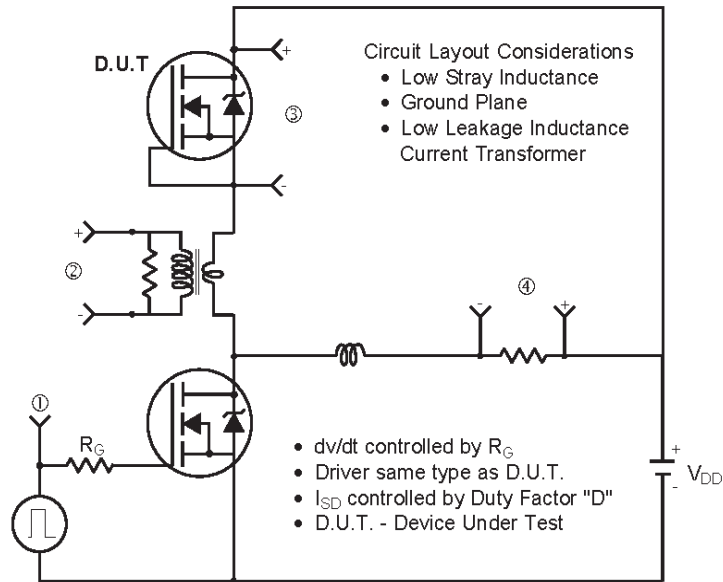


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



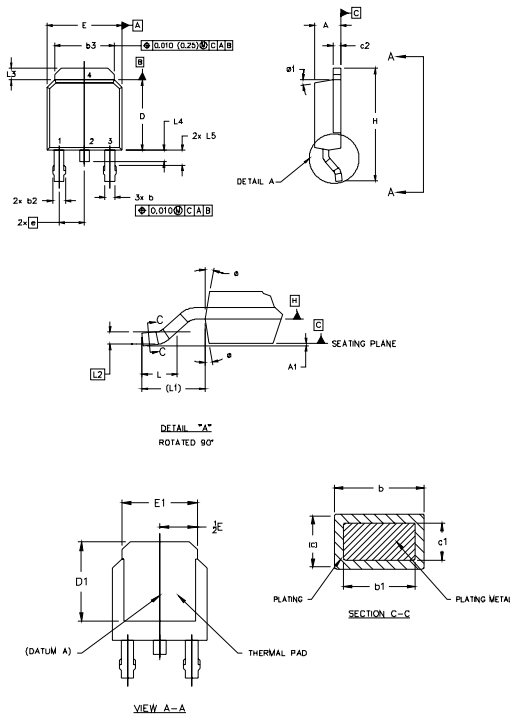
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRFR/U2407PbF

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
  - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
  - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.15		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.206	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	1.14	1.52	.045	.060	
L5	1.14	1.52	.045	.060	
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

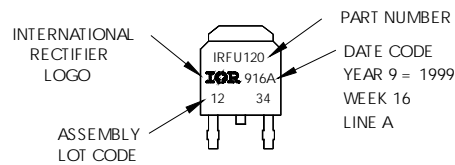
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

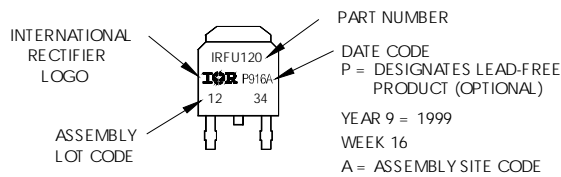
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"



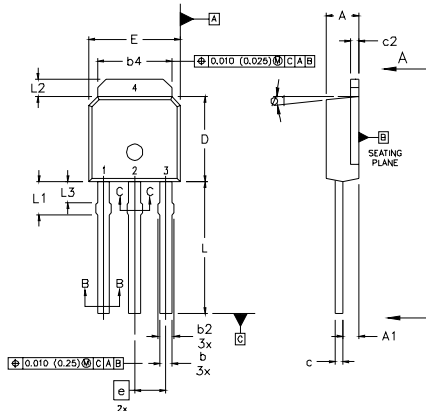
OR





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

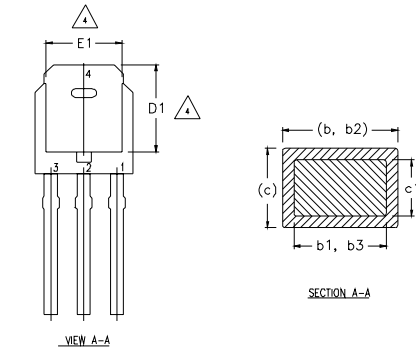


**NOTES:**

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

**LEAD ASSIGNMENTS**

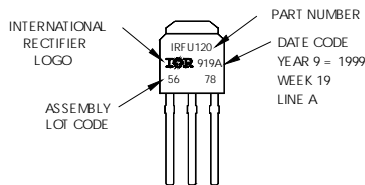
- HEXFET**
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN



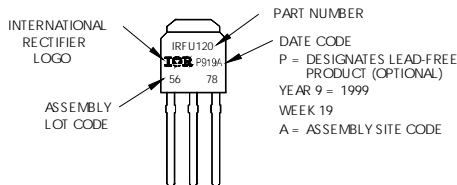
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	4
b4	5.00	5.46	0.195	0.215	
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	3, 4
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15°	Ø	15°	

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 1999 IN THE ASSEMBLY LINE "A"  
**Note:** "P" in assembly line position indicates "Lead-Free"



**OR**

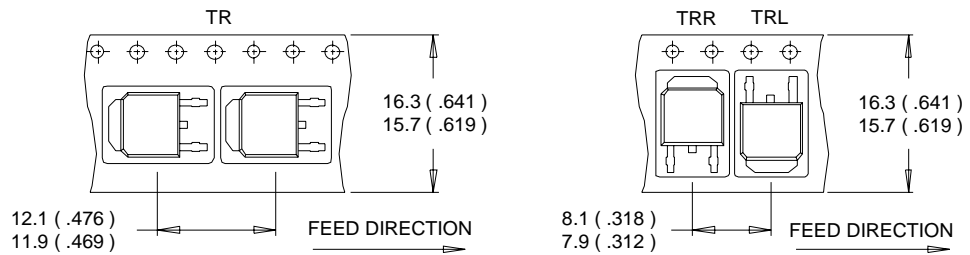


# IRFR/U2407PbF

International  
**IR** Rectifier

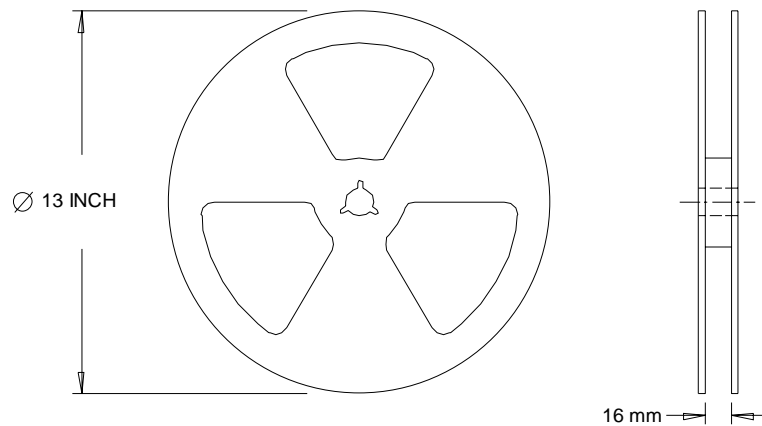
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International  
**IR** Rectifier

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TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>