

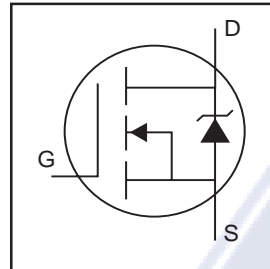
International  
**IR** Rectifier

PD - 91406

**IRFZ48N**

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

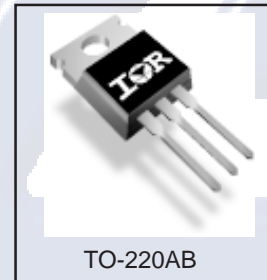


$V_{DSS} = 55V$   
 $R_{DS(on)} = 14m\Omega$   
 $I_D = 64A$

### Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	64	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	45	
$I_{DM}$	Pulsed Drain Current ①	210	
$P_D @ T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	0.83	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_{AR}$	Avalanche Current ①	32	A
$E_{AR}$	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.15	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

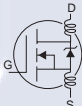
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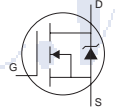
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## IRFZ48N

International  
IR RectifierElectrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	14	m $\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 32\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$
$g_{fs}$	Forward Transconductance	24	—	—	S	$V_{DS} = 25\text{V}$ , $I_D = 32\text{A}$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{DS} = 55\text{V}$ , $V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 44\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$Q_g$	Total Gate Charge	—	—	81	nC	$I_D = 32\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	—	19		$V_{DS} = 44\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	30		$V_{GS} = 10\text{V}$ , See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 28\text{V}$
$t_r$	Rise Time	—	78	—		$I_D = 32\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	34	—		$R_G = 0.85\Omega$
$t_f$	Fall Time	—	50	—		$V_{GS} = 10\text{V}$ , See Fig. 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1970	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	470	—		$V_{DS} = 25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	120	—		$f = 1.0\text{MHz}$ , See Fig. 5
$E_{AS}$	Single Pulse Avalanche Energy②	—	700⑤	190⑥		mJ

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	64	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)①	—	—	210		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = 32\text{A}$ , $V_{GS} = 0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	68	100	ns	$T_J = 25^\circ\text{C}$ , $I_F = 32\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	220	330	nC	$di/dt = 100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

## Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.37\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 32\text{A}$ . (See Figure 12)

- ③  $I_{SD} \leq 32\text{A}$ ,  $di/dt \leq 220\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$

- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

- ⑤ This is the destructive value not limited to the thermal limit.

- ⑥ This is the thermal limited value.

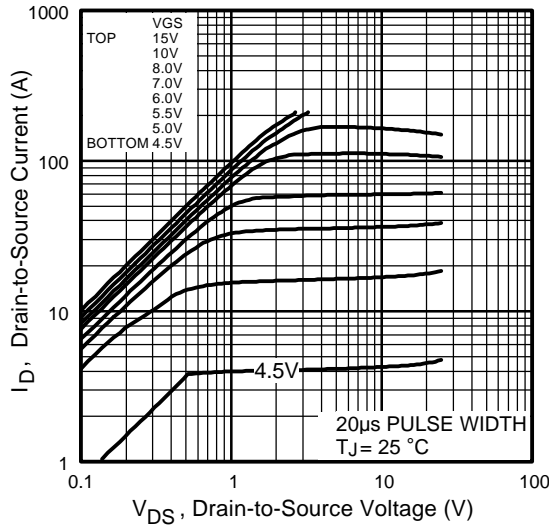


Fig 1. Typical Output Characteristics

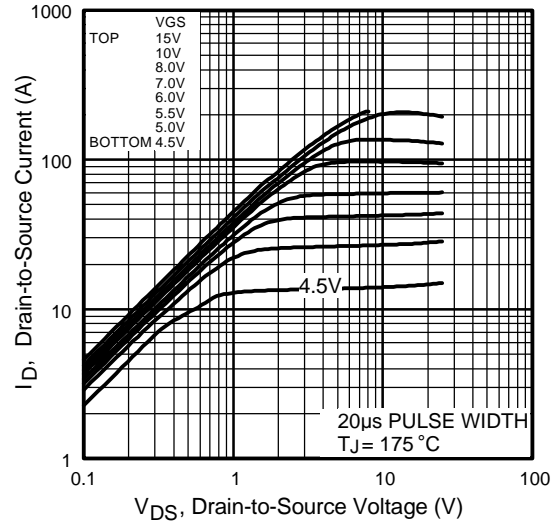


Fig 2. Typical Output Characteristics

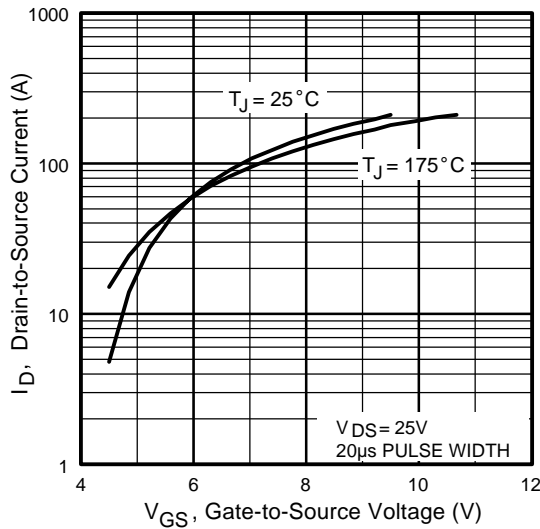


Fig 3. Typical Transfer Characteristics

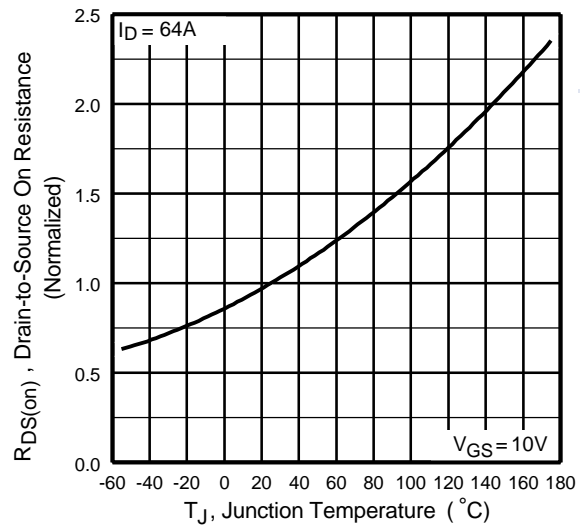
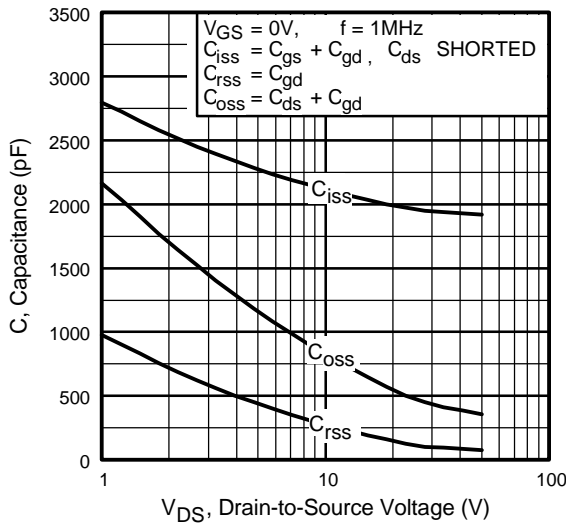


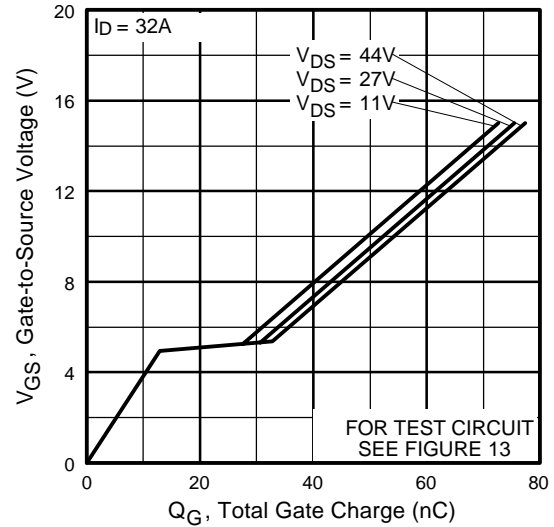
Fig 4. Normalized On-Resistance Vs. Temperature

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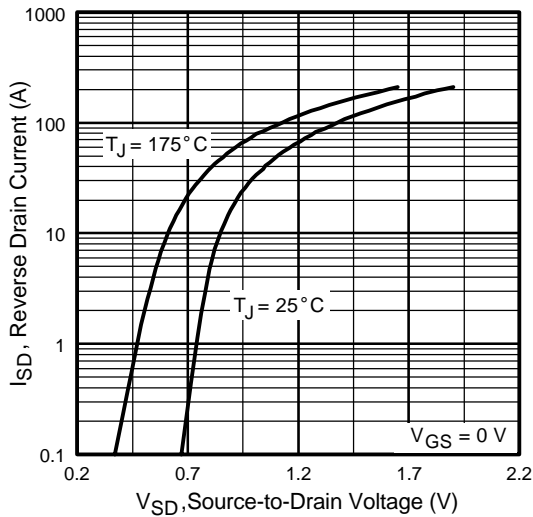
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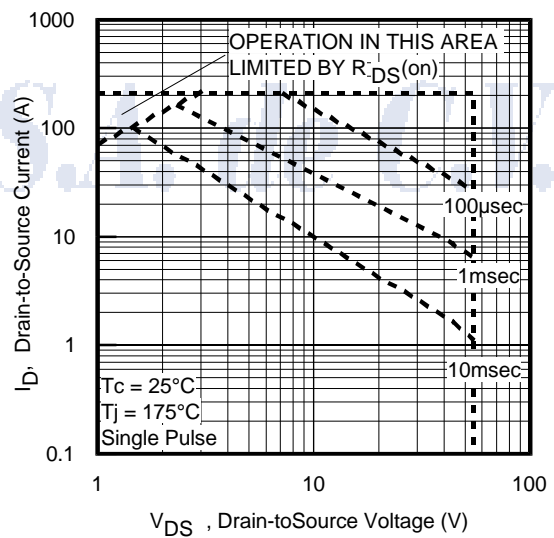
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



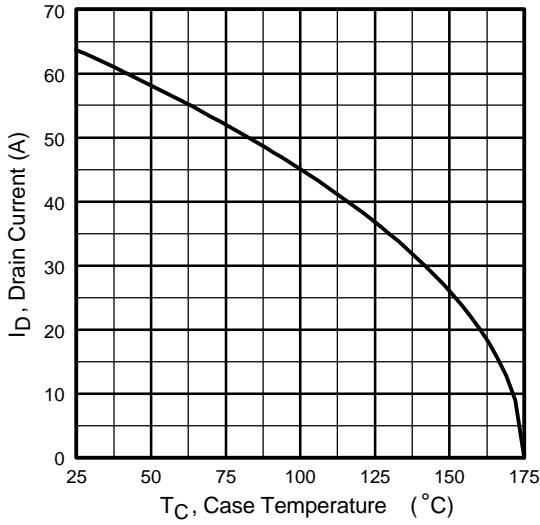
**Fig 7.** Typical Source-Drain Diode Forward Voltage



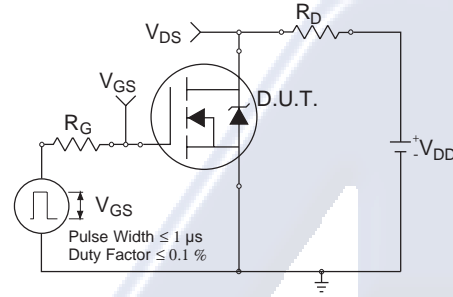
**Fig 8.** Maximum Safe Operating Area

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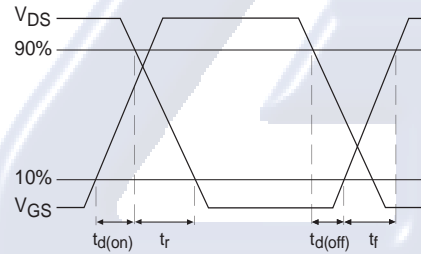
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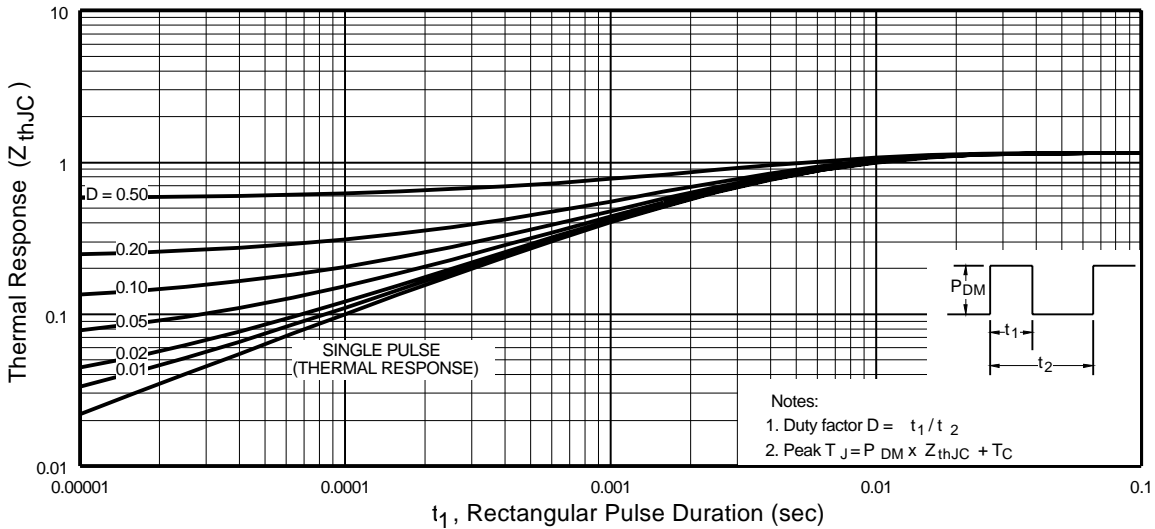
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



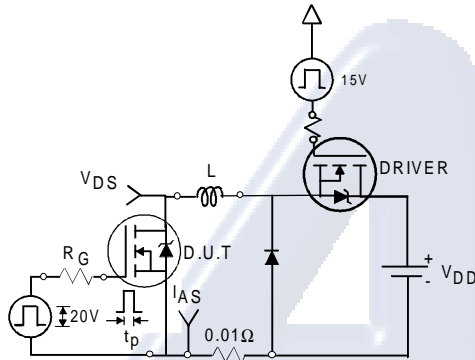
**Fig 10b.** Switching Time Waveforms



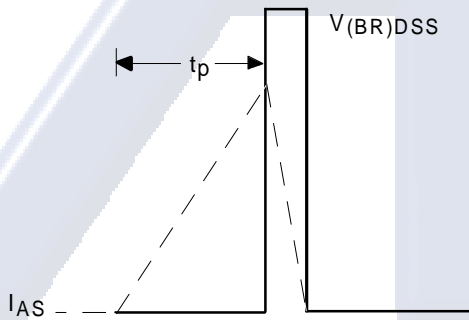
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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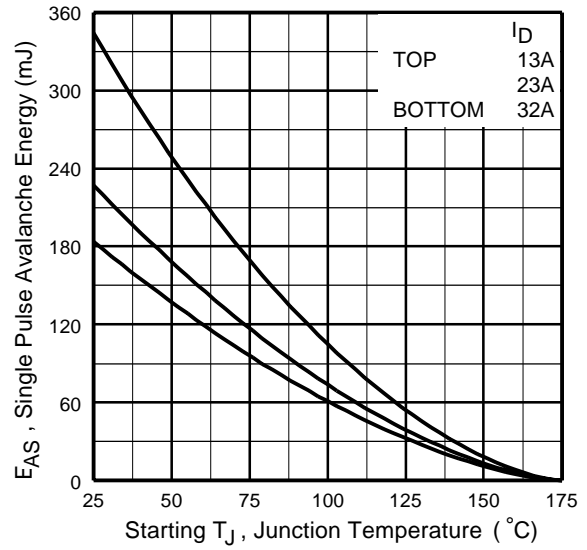
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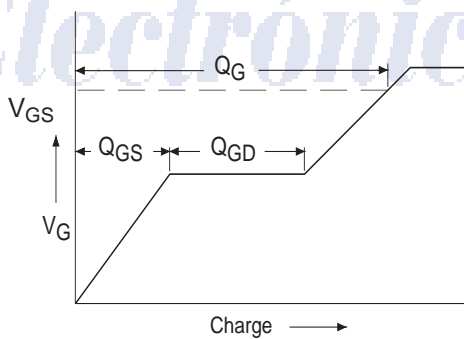
**Fig 12a.** Unclamped Inductive Test Circuit



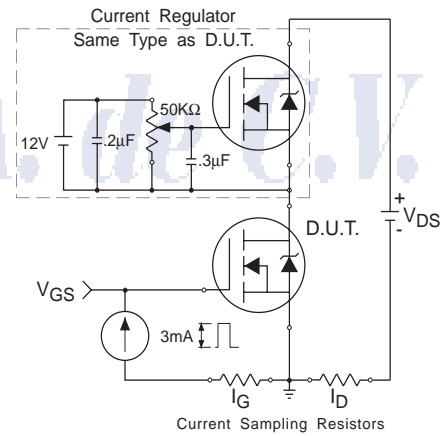
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

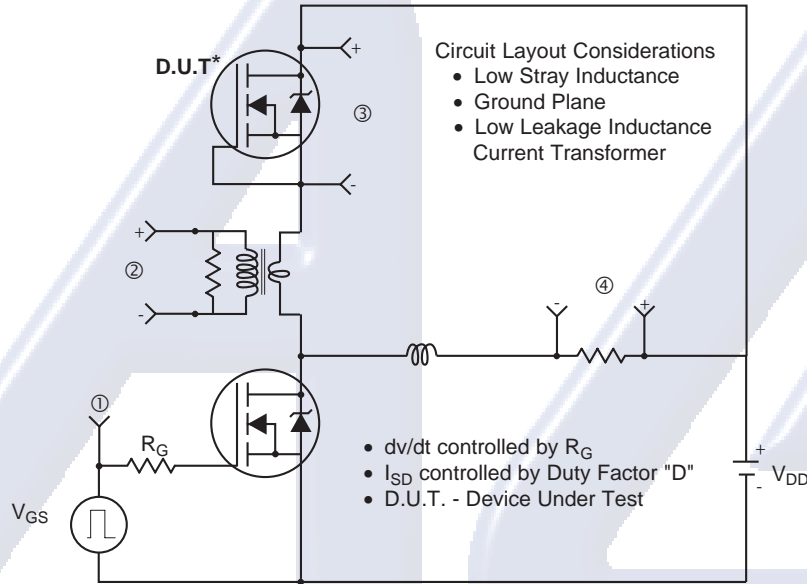


**Fig 13a.** Basic Gate Charge Waveform

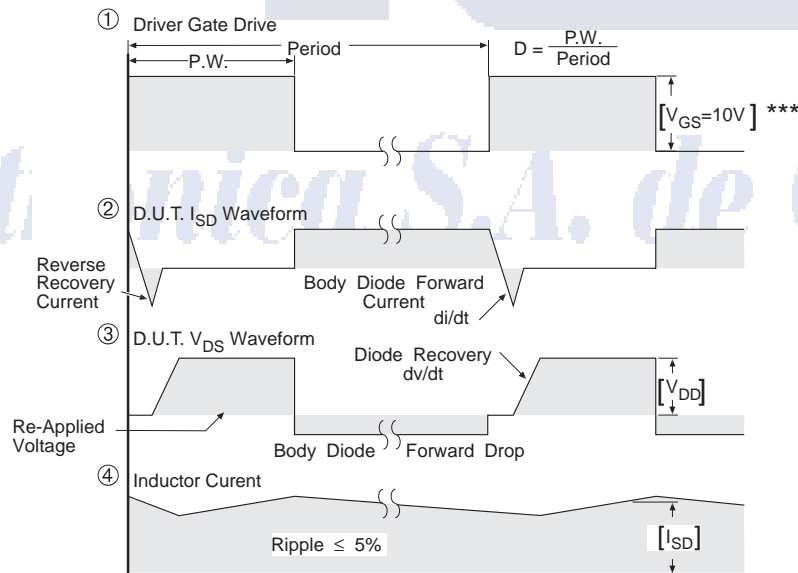


**Fig 13b.** Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

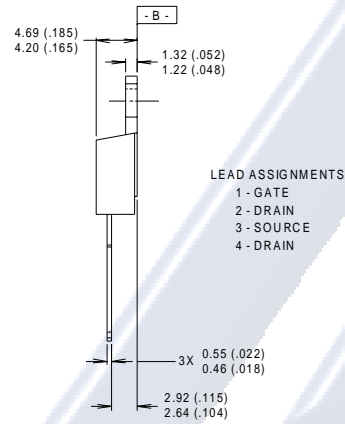
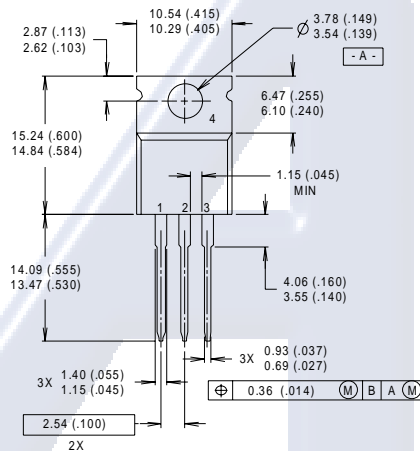
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## Package Outline

### TO-220AB

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS  
1 - GATE  
2 - DRAIN  
3 - SOURCE  
4 - DRAIN

NOTES:

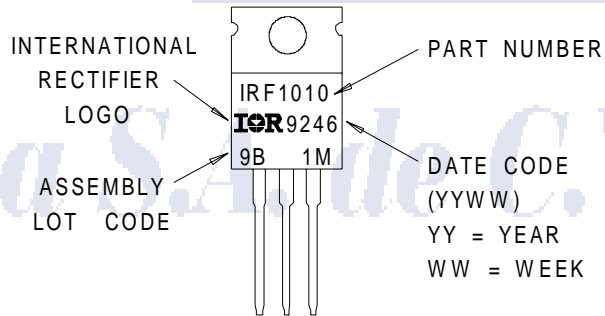
- 1 DIMENSIONING & TOLERANCING PER ANSII Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## Part Marking Information

### TO-220AB

EXAMPLE : THIS IS AN IRF1010  
WITH ASSEMBLY  
LOT CODE 9B1M



Data and specifications subject to change without notice.

This product has been designed and qualified for the Automotive [Q101] market.

Qualification Standards can be found on IR's Web site.

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