

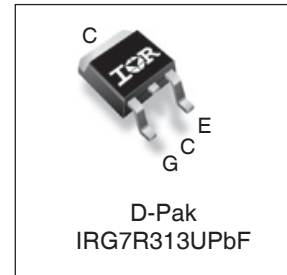
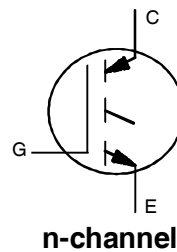
**PDP TRENCH IGBT**

# IRG7R313UPbF

**Features**

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low  $V_{CE(on)}$  and Energy per Pulse ( $E_{PULSE}^{TM}$ ) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	330	V
$V_{CE(ON)\ typ. @ I_C = 20A}$	1.35	V
$I_{RP\ max @ T_C = 25^\circ C}$	160	A
$T_J\ max$	150	$^\circ C$



G	C	E
Gate	Collector	Emitter

**Description**

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low  $V_{CE(on)}$  and low  $E_{PULSE}^{TM}$  rating per silicon area which improve panel efficiency. Additional features are 150 $^\circ C$  operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GE}$	Gate-to-Emitter Voltage	$\pm 30$	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	40	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	20	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	160	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	78	
$P_D @ T_C = 100^\circ C$	Power Dissipation	31	
	Linear Derating Factor	0.63	$W/^\circ C$
$T_J$	Operating Junction and	-40 to + 150	$^\circ C$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	1.6	$^\circ C/W$

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions		
$BV_{CES}$	Collector-to-Emitter Breakdown Voltage	330	—	—	V	$V_{GE} = 0V, I_{CE} = 250\mu A$		
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.4	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_{CE} = 1\text{mA}$		
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.21	1.45	V	$V_{GE} = 15V, I_{CE} = 12A$ ③		
		—	1.35	—		$V_{GE} = 15V, I_{CE} = 20A$ ③		
		—	1.75	—		$V_{GE} = 15V, I_{CE} = 40A$ ③		
		—	2.14	—		$V_{GE} = 15V, I_{CE} = 60A$ ③		
		—	1.41	—		$V_{GE} = 15V, I_{CE} = 20A, T_J = 150^\circ\text{C}$ ③		
$V_{GE(th)}$	Gate Threshold Voltage	2.2	—	4.7	V	$V_{CE} = V_{GE}, I_{CE} = 1.0\text{mA}$		
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10	—	mV/ $^\circ\text{C}$			
$I_{CES}$	Collector-to-Emitter Leakage Current	—	1.0	10	$\mu A$	$V_{CE} = 330V, V_{GE} = 0V$		
		—	25	150		$V_{CE} = 330V, V_{GE} = 0V, T_J = 125^\circ\text{C}$		
		—	75	—		$V_{CE} = 330V, V_{GE} = 0V, T_J = 150^\circ\text{C}$		
$I_{GES}$	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$		
	Gate-to-Emitter Reverse Leakage	—	—	-100		$V_{GE} = -30V$		
$g_{fe}$	Forward Transconductance	—	47	—	S	$V_{CE} = 25V, I_{CE} = 12A$		
$Q_g$	Total Gate Charge	—	33	—	nC	$V_{CE} = 240V, I_C = 12A, V_{GE} = 15V$ ③		
$Q_{gc}$	Gate-to-Collector Charge	—	12	—				
$t_{d(on)}$	Turn-On delay time	—	1.0	—				
$t_r$	Rise time	—	13	—	ns	$I_C = 12A, V_{CC} = 196V$ $R_G = 10\Omega, L = 210\mu H$ $T_J = 25^\circ\text{C}$		
$t_{d(off)}$	Turn-Off delay time	—	65	—				
$t_f$	Fall time	—	68	—				
$t_{d(on)}$	Turn-On delay time	—	11	—				
$t_{d(on)}$	Turn-On delay time	—	11	—	ns	$I_C = 12A, V_{CC} = 196V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150\text{nH}$ $T_J = 150^\circ\text{C}$		
		$t_r$	Rise time	—			14	—
		$t_{d(off)}$	Turn-Off delay time	—			86	—
		$t_f$	Fall time	—			190	—
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G = 5.1\Omega$		
$E_{PULSE}$	Energy per Pulse	—	480	—	$\mu J$	$L = 220\text{nH}, C = 0.20\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$		
		—	570	—		$L = 220\text{nH}, C = 0.20\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$		
ESD	Human Body Model	Class 1C (Per JEDEC standard JESD22-A114)						
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)						
$C_{ies}$	Input Capacitance	—	880	—	pF	$V_{GE} = 0V$		
$C_{oes}$	Output Capacitance	—	47	—		$V_{CE} = 30V$		
$C_{res}$	Reverse Transfer Capacitance	—	26	—		$f = 1.0\text{MHz}$		
$L_C$	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)		
$L_E$	Internal Emitter Inductance	—	7.5	—		from package and center of die contact		

### Notes:

- ① Half sine wave with duty cycle = 0.05,  $t_{on} = 2\mu\text{sec}$ .
- ②  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

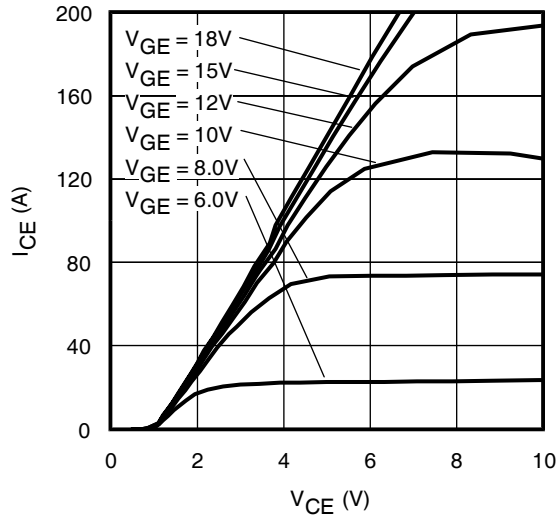


Fig 1. Typical Output Characteristics @ 25°C

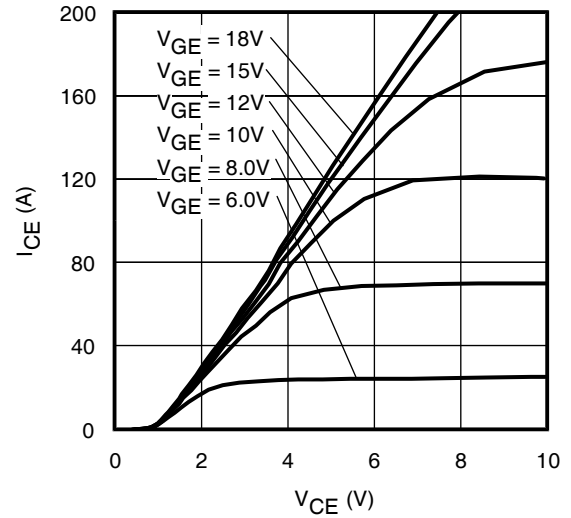


Fig 2. Typical Output Characteristics @ 75°C

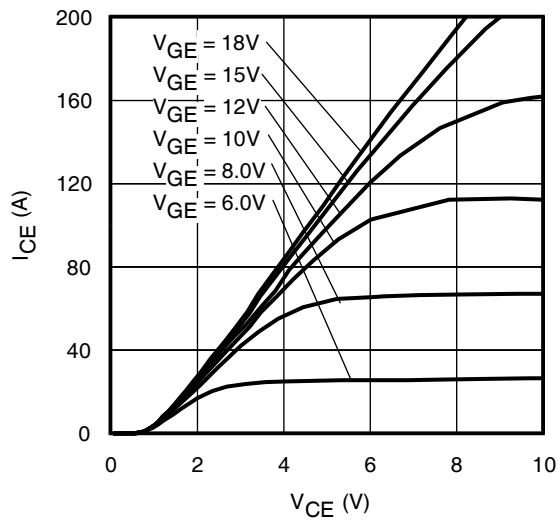


Fig 3. Typical Output Characteristics @ 125°C

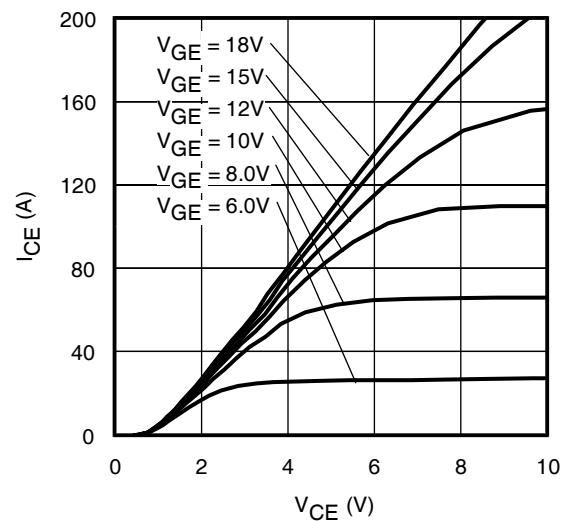


Fig 4. Typical Output Characteristics @ 150°C

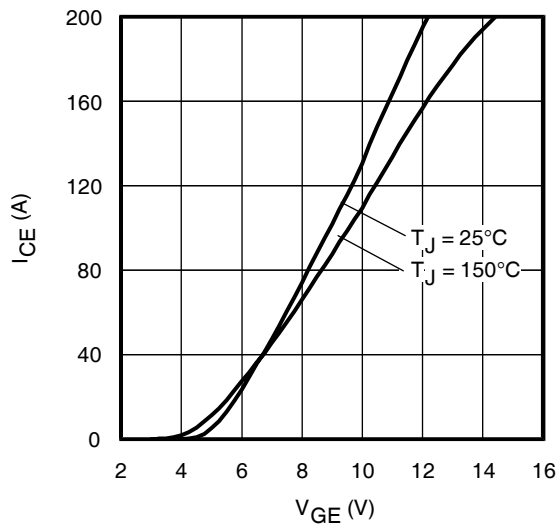


Fig 5. Typical Transfer Characteristics

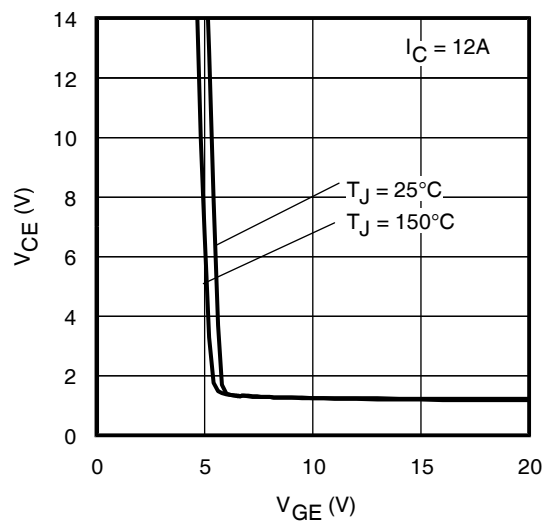


Fig 6.  $V_{CE(ON)}$  vs. Gate Voltage

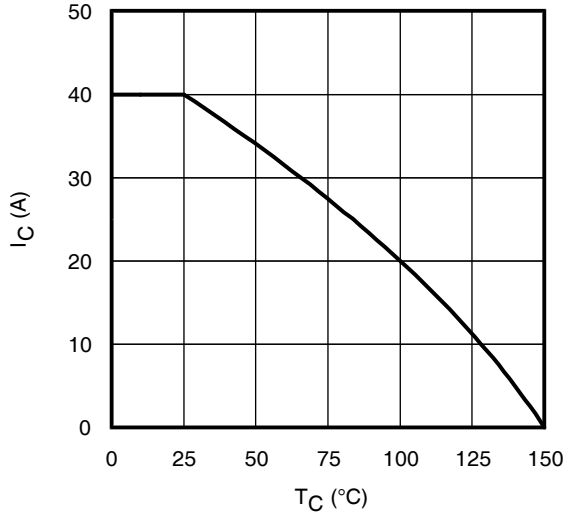


Fig 7. Maximum Collector Current vs. Case Temperature

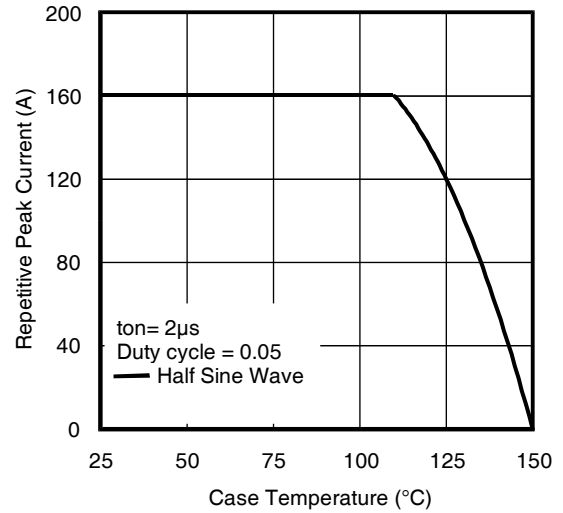


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

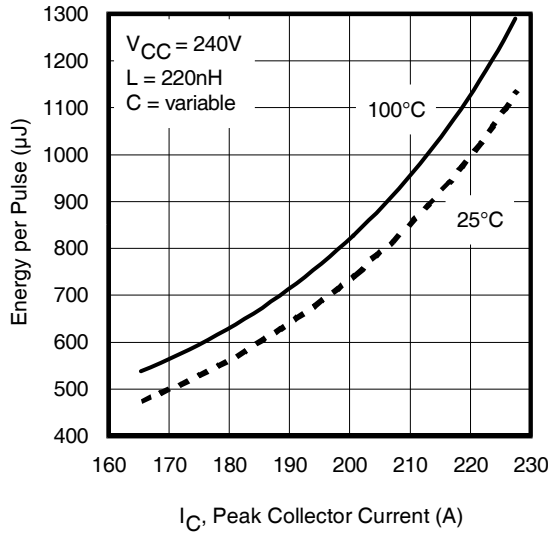


Fig 9. Typical  $E_{PULSE}$  vs. Collector Current

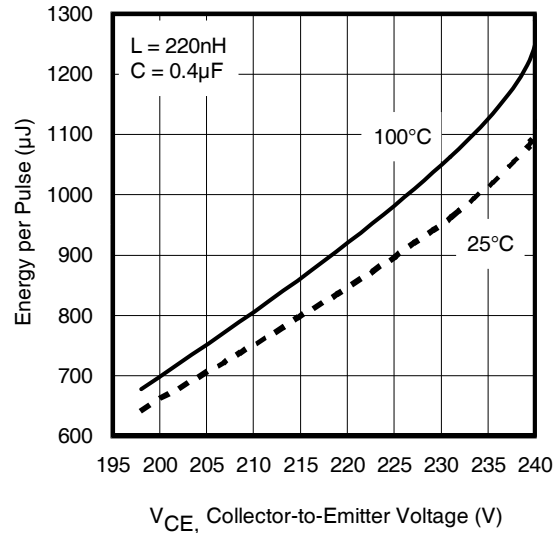


Fig 10. Typical  $E_{PULSE}$  vs. Collector-to-Emitter Voltage

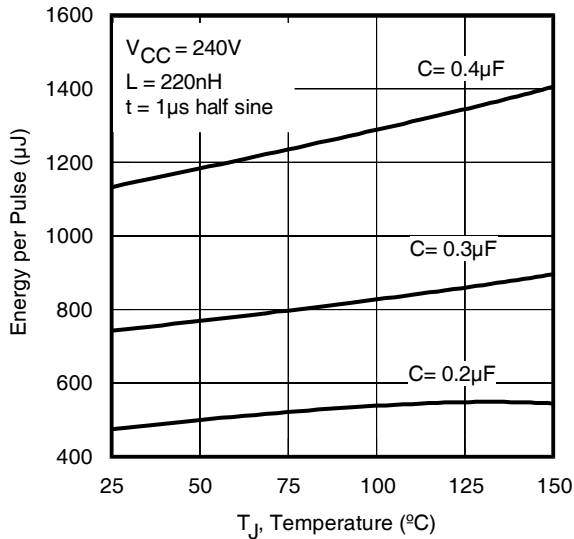


Fig 11.  $E_{PULSE}$  vs. Temperature

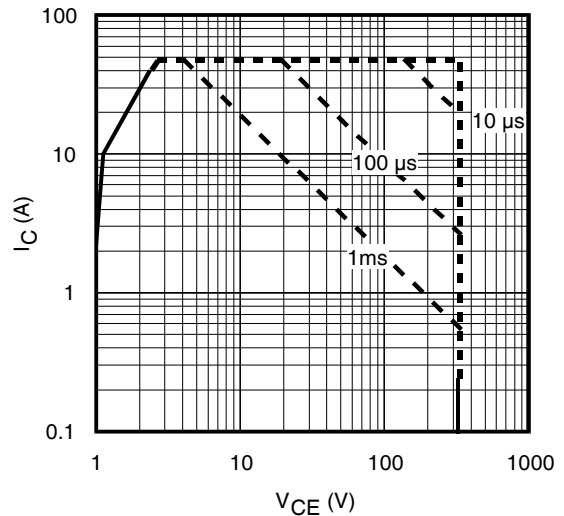


Fig 12. Forward Bias Safe Operating Area

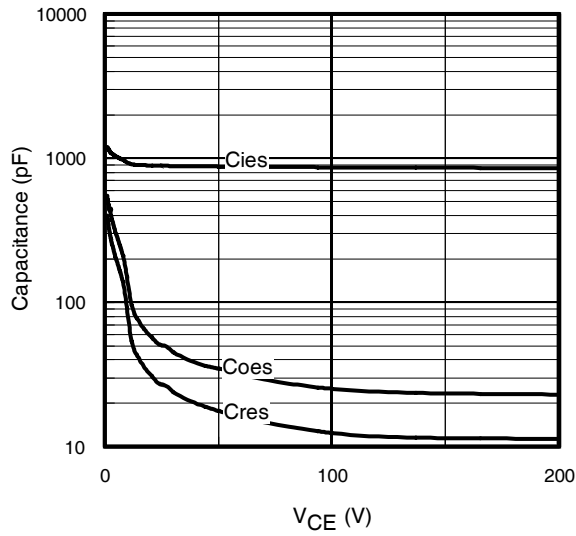


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

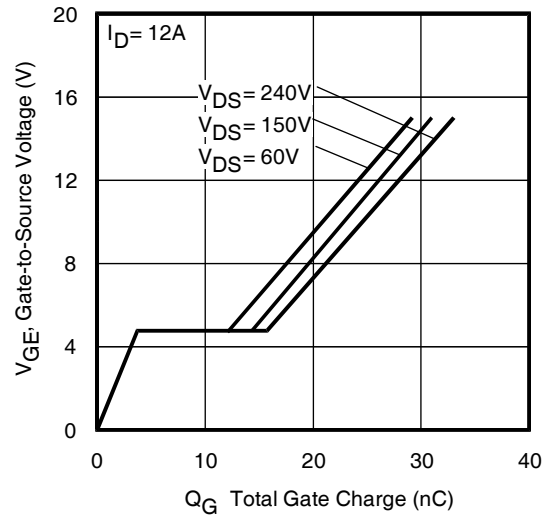


Fig 14. Typical Gate Charge vs. Gate-to-Source Voltage

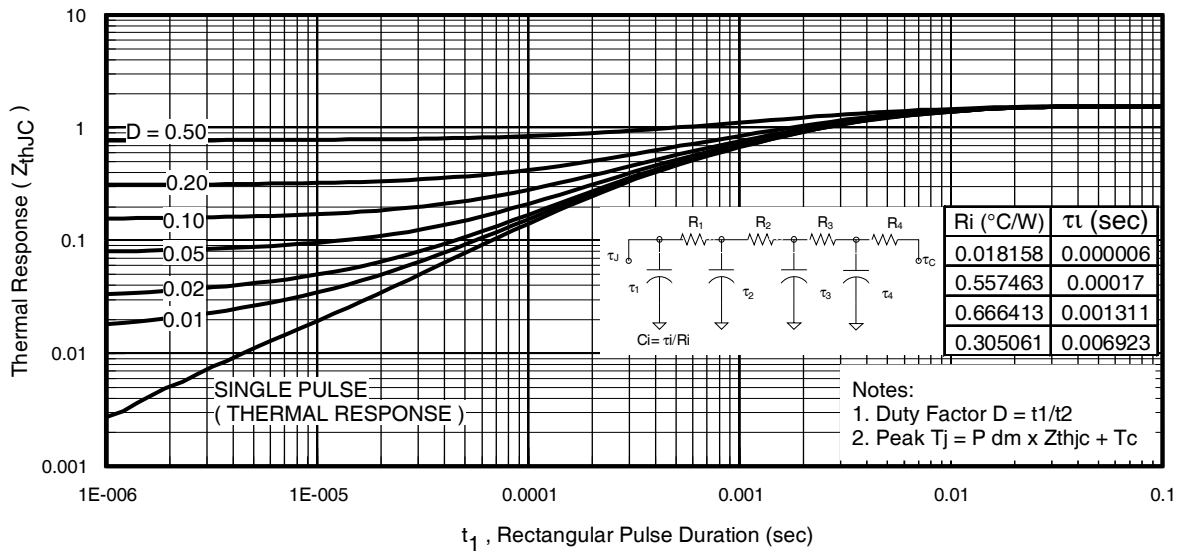
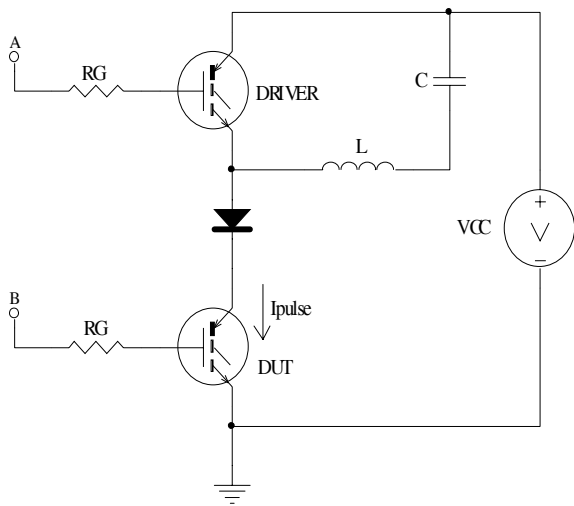
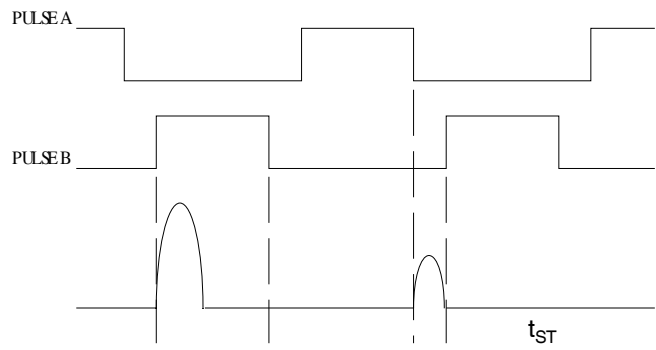


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 16a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



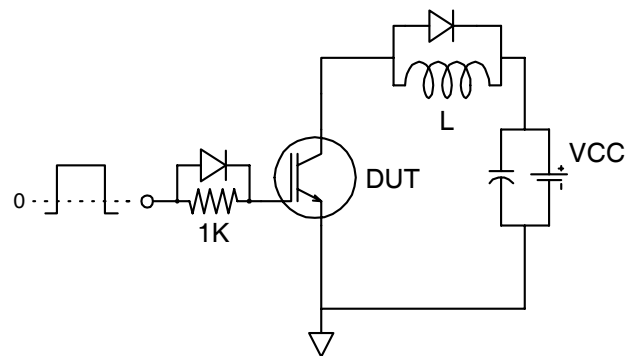
**Fig 16b.**  $t_{st}$  Test Waveforms

$V_{CE}$

Energy

$I_C$  Current

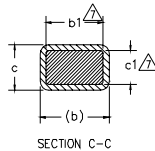
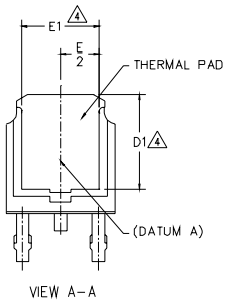
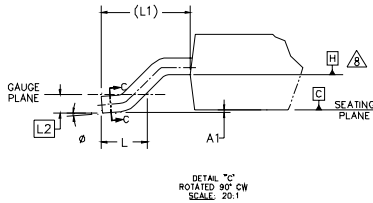
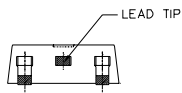
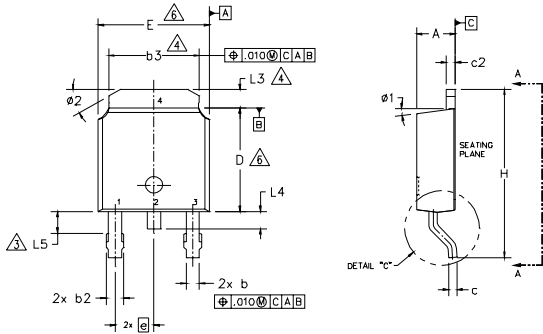
**Fig 16c.**  $E_{PULSE}$  Test Waveforms



**Fig. 17 -** Gate Charge Circuit (turn-off)

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- △ LEAD DIMENSION UNCONTROLLED IN L5.
- △ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- △ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
∅	0"	10"	0"	10"	
∅1	0"	15"	0"	15"	
∅2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

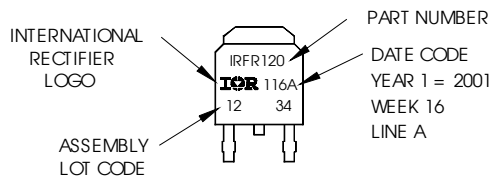
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

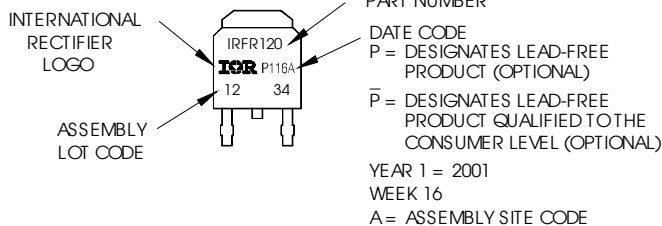
EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

"P" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level



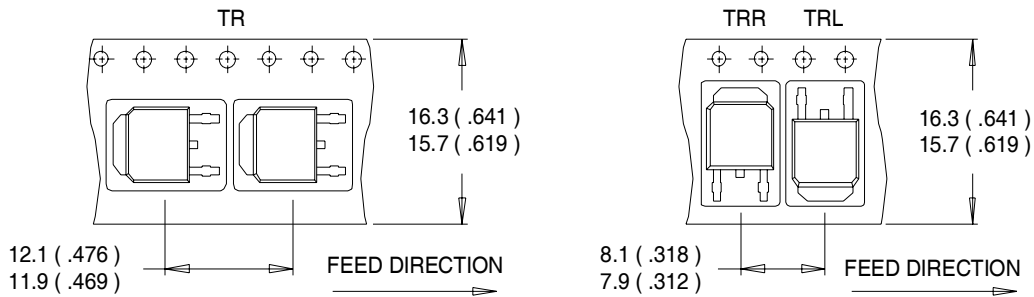
OR



# IRG7R313UPbF

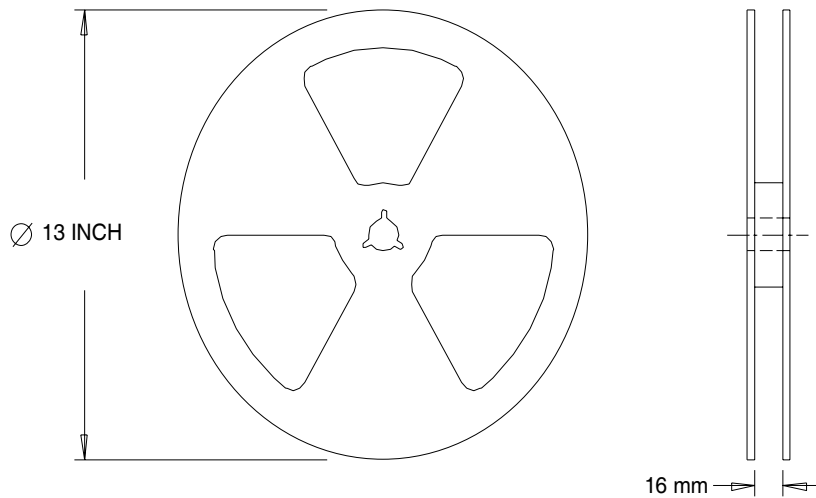
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.  
This product has been designed for the Industrial market.  
Qualification Standards can be found on IR's Web site.