



# SANYO Semiconductors

## DATA SHEET

# LA6261

Monolithic Linear IC  
For Optical Disk Drive  
6-Channel Driver  
(BTL: 4 channels, H bridge: 2 channels)

### Overview

The LA6261 is a 6-channel driver IC that incorporates 4 channels of BTL output and 2 channels of H-bridge output. It is optimal for the actuator driver for CDs, MDs, and other optical disk drives.

### Features

- Six power amplifier channels on a single chip (BTL: 4 channels, H-bridge: 2 channels)
- $I_O$  max: 700mA (Each channel)
- Built-in level shifter circuits (BTL amplifier)
- Built-in thermal protection (thermal shutdown) circuit
- Separate power supply for H-bridge (2 channels)
- Onchip 3.3V regulator controller (uses an external output transistor)
- Adjustment pin for the H-bridge output

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

| Parameter                     | Symbol       | Conditions                       | Ratings     | Unit             |
|-------------------------------|--------------|----------------------------------|-------------|------------------|
| Supply voltage                | $V_{CC}$ max |                                  | 14          | V                |
| Maximum output current        | $I_O$ max    | for each of the channel 1 to 6   | 0.7         | A                |
| Maximum input voltage         | $V_{INB}$    |                                  | 13          | V                |
| MUTE pin voltage              | $V_{MUTE}$   |                                  | 13          | V                |
| Allowable power dissipation   | $P_d$ max    | Independent IC                   | 0.8         | W                |
|                               |              | Mounted on the specified board * | 2           | W                |
| Operating ambient temperature | $T_{opr}$    |                                  | -30 to +85  | $^\circ\text{C}$ |
| Storage ambient temperature   | $T_{stg}$    |                                  | -55 to +150 | $^\circ\text{C}$ |

\* Mounted on a specified board: 76.1mm×114.1mm×1.6mm, glass epoxy.

### Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

| Parameter      | Symbol   | Conditions | Ratings   | Unit |
|----------------|----------|------------|-----------|------|
| Supply voltage | $V_{CC}$ |            | 5.6 to 13 | V    |

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**SANYO Semiconductor Co., Ltd.**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

# LA6261

**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = 8\text{V}$ ,  $V_{REF} = 1.65\text{V}$

| Parameter                            | Symbol               | Conditions                                                                                                                | Ratings |     |                      | Unit |
|--------------------------------------|----------------------|---------------------------------------------------------------------------------------------------------------------------|---------|-----|----------------------|------|
|                                      |                      |                                                                                                                           | min     | typ | max                  |      |
| All Blocks                           |                      |                                                                                                                           |         |     |                      |      |
| No-load current drain ON             | I <sub>CC</sub> -ON  | All outputs on *1, FWD=REV=0V                                                                                             |         | 30  | 50                   | mA   |
| V <sub>REF</sub> input voltage range | V <sub>REF</sub> -IN |                                                                                                                           | 0.5     |     | V <sub>CC</sub> -1.5 | V    |
| BTL AMP                              |                      |                                                                                                                           |         |     |                      |      |
| Output offset voltage                | V <sub>OFF</sub>     | BTL amplifier, the voltage difference between each channel outputs                                                        | -50     |     | +50                  | mV   |
| Input voltage range                  | V <sub>IN</sub>      | Applied to pins V <sub>IN</sub> 1 to V <sub>IN</sub> 4                                                                    | 0       |     | V <sub>CC</sub>      | V    |
| Output voltage                       | V <sub>O</sub>       | Voltage between V <sub>O</sub> + and V <sub>O</sub> - for each channel when R <sub>L</sub> =8Ω *2                         | 4       | 5   |                      | V    |
| Closed-circuit voltage gain          | V <sub>G</sub>       | The gain from the input to the output                                                                                     |         | 4   |                      | deg  |
| MUTE ON voltage                      | V <sub>MT</sub> ON   | *3                                                                                                                        | 2       |     | SV <sub>CC</sub>     | V    |
| MUTE OFF voltage                     | V <sub>MT</sub> OFF  | *3                                                                                                                        | 0       |     | 0.5                  | V    |
| Slew rate                            | SR                   | For the independent amplifier.<br>Times 2 when between outputs *4                                                         |         | 0.5 |                      | V/μs |
| H-bridge Block                       |                      |                                                                                                                           |         |     |                      |      |
| Output voltage                       | V <sub>O</sub> -LOAD | Voltage between V <sub>O</sub> + and V <sub>O</sub> - for each channel when R <sub>L</sub> =10Ω                           | 6.2     | 6.7 |                      | V    |
| Input low level                      | V <sub>IN</sub> -L   |                                                                                                                           | 0       |     | 1                    | V    |
| Input high level                     | V <sub>IN</sub> -H   |                                                                                                                           | 2       |     | SV <sub>CC</sub>     | V    |
| Output setting voltage               | V <sub>CONT</sub>    | Voltage between V <sub>O</sub> + and V <sub>O</sub> - for each channel when V <sub>CONT</sub> =3V and R <sub>L</sub> =10Ω |         | 2.8 |                      | V    |
| Regulator Block                      |                      |                                                                                                                           |         |     |                      |      |
| Output voltage                       | V <sub>reg</sub>     | I <sub>L</sub> =100mA                                                                                                     | 3.05    | 3.3 | 3.55                 | V    |
| Output load variation                | ΔV <sub>RL</sub>     | I <sub>L</sub> =0 to 200mA                                                                                                | -50     | 0   | 10                   | mV   |
| Supply voltage variation             | ΔV <sub>VCC</sub>    | V <sub>CC</sub> =6 to 12V, I <sub>L</sub> =100mA                                                                          | -15     | 21  | 60                   | mV   |

\*1: The total current dissipation for  $SV_{CC}$ ,  $PV_{CC1}$ , and  $PV_{CC2}$  with no load

\*2: Output in the saturated state

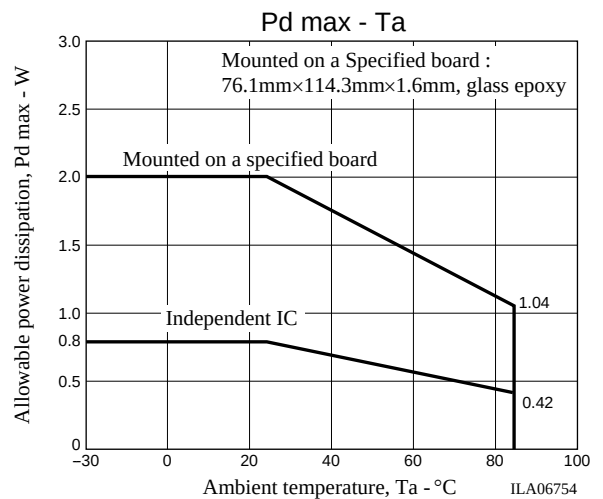
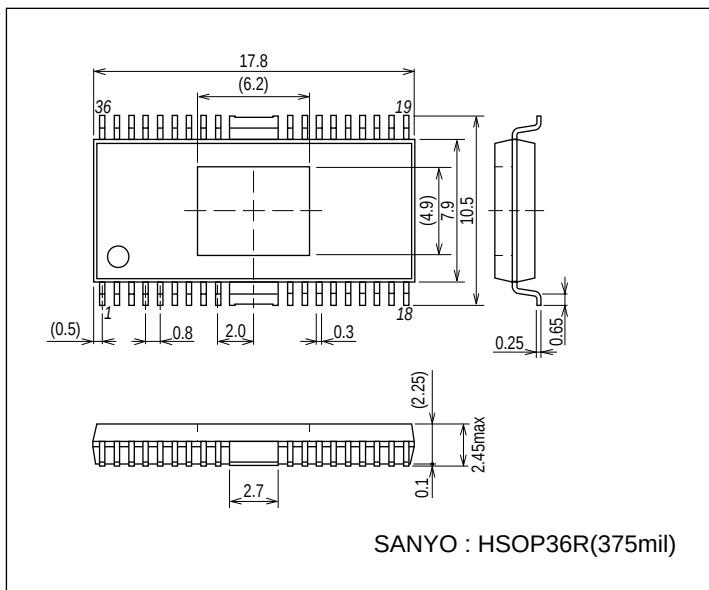
\*3: When the MUTE pin is high, the BTL output will be on, and when low, the BTL output will be OFF (HI impedance).

\*4: Design guarantee value

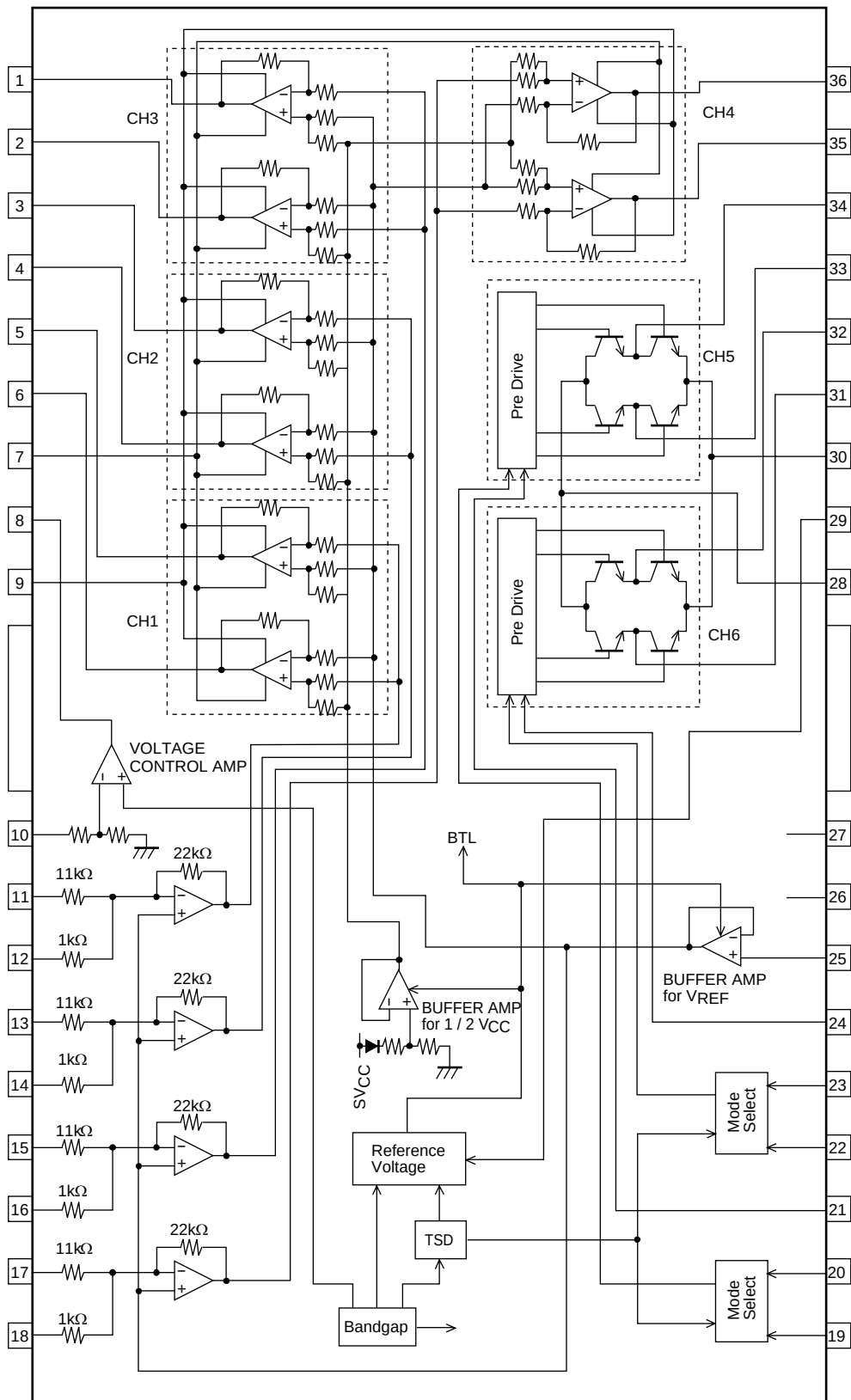
## Package Dimensions

unit : mm (typ)

3251



# Block Diagram



ILA06744

## Pin Description

| Pin No. | Pin Name          | Description                                                                        | Equivalent Circuit Diagram |
|---------|-------------------|------------------------------------------------------------------------------------|----------------------------|
| 1       | V <sub>O3+</sub>  | Channel 3 (BTL) output (+)                                                         |                            |
| 2       | V <sub>O3-</sub>  | Channel 3 (BTL) output (-)                                                         |                            |
| 3       | V <sub>O2+</sub>  | Channel 2 (BTL) output (+)                                                         |                            |
| 4       | V <sub>O2-</sub>  | Channel 2 (BTL) output (-)                                                         |                            |
| 5       | V <sub>O1+</sub>  | Channel 1 (BTL) output (+)                                                         |                            |
| 6       | V <sub>O1-</sub>  | Channel 1 (BTL) output (-)                                                         |                            |
| 7       | PGND              | Power system ground for channels 1 to 4 (BTL)                                      |                            |
| 9       | PV <sub>CC1</sub> | Power system power supply for channels 1 to 4 (BTL) (shorted to SV <sub>CC</sub> ) |                            |
| 35      | V <sub>O4+</sub>  | Channel 4 (BTL) output (+)                                                         |                            |
| 36      | V <sub>O4-</sub>  | Channel 4 (BTL) output (-)                                                         |                            |
| 8       | REGIN             | Regulator (to the base of the external PNP transistor)                             |                            |
| 10      | REGOUT            | Regulator (to the collector of the external PNP transistor)                        |                            |
| 11      | V <sub>IN1</sub>  | Channel 1 input                                                                    |                            |
| 12      | V <sub>IN1G</sub> | Channel 1 input (gain adjustment)                                                  |                            |
| 13      | V <sub>IN2</sub>  | Channel 2 input                                                                    |                            |
| 14      | V <sub>IN2G</sub> | Channel 2 input (gain adjustment)                                                  |                            |
| 15      | V <sub>IN3</sub>  | Channel 3 input                                                                    |                            |
| 16      | V <sub>IN3G</sub> | Channel 3 input (gain adjustment)                                                  |                            |
| 17      | V <sub>IN4</sub>  | Channel 4 input                                                                    |                            |
| 18      | V <sub>IN4G</sub> | Channel 4 input (gain adjustment)                                                  |                            |
| 19      | FWD5              | Channel 5 output direction switching (FWD), H-bridge logic input                   |                            |
| 20      | REV5              | Channel 5 output direction switching (REV), H-bridge logic input                   |                            |
| 22      | FWD6              | Channel 6 output direction switching (FWD), H-bridge logic input                   |                            |
| 23      | REV6              | Channel 6 output direction switching (REV), H-bridge logic input                   |                            |

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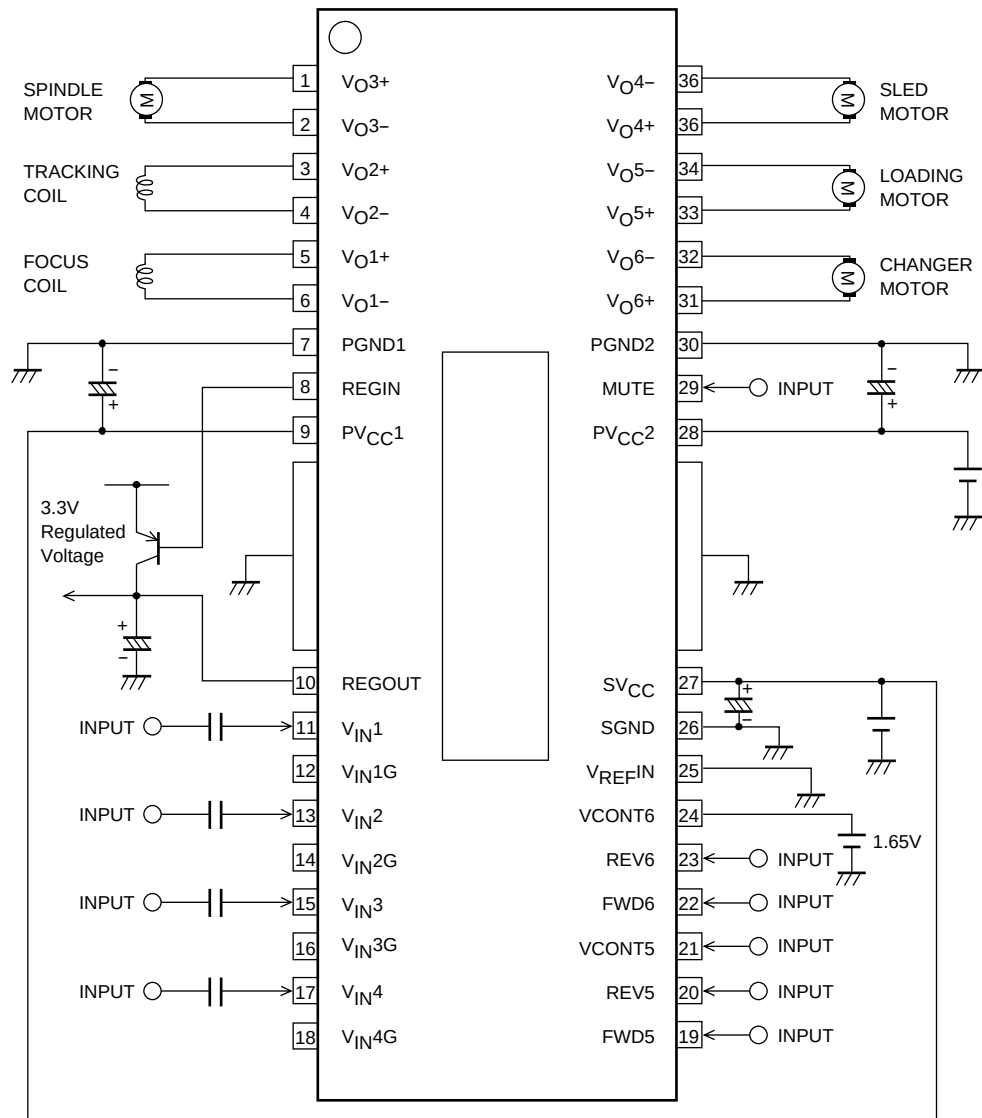
| Pin No.                          | Pin Name                                       | Description                                                                                                                                                                                                                                                      | Equivalent Circuit Diagram |
|----------------------------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|
| 21<br>24                         | VCONT5<br>VCONT6                               | Channel 5 output voltage setting<br>Channel 6 output voltage setting                                                                                                                                                                                             |                            |
| 25                               | VREFIN                                         | Reference voltage input                                                                                                                                                                                                                                          |                            |
| 28<br>30<br>31<br>32<br>33<br>34 | PVCC2<br>PGND2<br>VO6+<br>VO6-<br>VO5+<br>VO5- | Power system power supply for for channels 5 and 6 (H-bridge)<br>Power system ground for channels 5 and 6 (H-bridge)<br>Channel 6 (H-bridge) output (+)<br>Channel 6 (H-bridge) output (-)<br>Channel 5 (H-bridge) output (+)<br>Channel 5 (H-bridge) output (-) |                            |
| 29                               | MUTE                                           | BTL mute signal input                                                                                                                                                                                                                                            |                            |
| 26                               | SGND                                           | Signal system ground                                                                                                                                                                                                                                             |                            |
| 27                               | SVCC                                           | Signal system power supply (shorted to PVCC1)                                                                                                                                                                                                                    |                            |

## Truth Table

| INPUT   |         | OUTPUT  |         |
|---------|---------|---------|---------|
| FWD5(6) | REV5(6) | VO5(6)+ | VO5(6)- |
| L       | L       | Z       | Z       |
| L       | H       | H       | L       |
| H       | L       | L       | H       |
| H       | H       | L       | L       |

\*Z: HI-Impedance

# Sample Application Circuit



ILA06743

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