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Ordering number: EN 5897

Monolithic Linear IC

LA6541

4-channel Bridge Driver for Compact Discs

Overview

The LA6541 is a 4-channel bridge (BTL) driver with a 5 V power supply (uses an external PNP transistor) developed for compact discs.

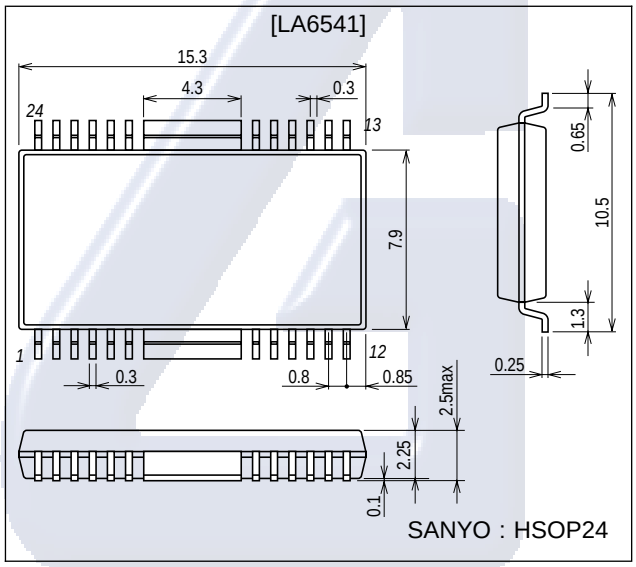
Functions and Features

- 4-channel bridge (BTL) power amplifier.
- I_O max. = 700 mA.
- With mute circuit
  (Affects all amplifier outputs, Amp 1 to Amp 8).
  (When the mute voltage is low, the outputs turn off; when the mute voltage is high, the outputs turn on).
- 5.0 V regulator built in (Uses external PNP transistor).
- Reset circuit built in (The reset output delay time can be adjusted through an external capacitor).

Package Dimensions

unit : mm

3227-HSOP24



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Maximum input voltage	V_{IN}B		13	V
Mute pin voltage	V_{Mute}		13	V
Allowable power dissipation	Pd max	When using standard board 114.3 × 76.1 × 1.5 mm (material: glass epoxy)	2.3	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	V_{CC}		5.6 to 13	V
Reset output source current	I_{ORH}		0 to 200	µA
Reset output sink current	I_{ORL}		0 to 2	mA

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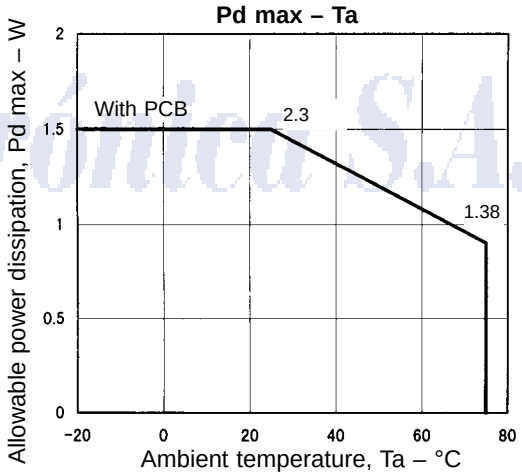
Electrical Characteristics at Ta = 25°C, V_{CC} = 8.0 V, V_{REF} = 2.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
No-load current drain	$I_{CC}1$	When all amplifier outputs are on (Mute high)		20	40	mA
	$I_{CC}2$	When all amplifier outputs are off (Mute low)		15	35	mA
Output offset voltage	$V_{OF}1$	Amplifier 1 to 2 (V_O1 to V_O2), Amplifier 3 to 4 (V_O3 to V_O4)	–50		+50	mV
	$V_{OF}2$	Amplifier 5 to 6 (V_O5 to V_O6), Amplifier 7 to 8 (V_O7 to V_O8)	–50		+50	mV
Buffer amplifier input voltage range	V_{BIN}		1.5		V_{CC}–1.5	V
Input voltage range	V_{IN}		1.0		V_{CC}–1.5	V
Output source voltage	V_O1	Note 1, when R_L = 8.0 Ω	5.0	5.6		V
Output sink voltage	V_O2	Note 2, when R_L = 8.0 Ω		1.8	2.4	V
Closed-circuit voltage gain	VG	Between bridge amplifiers		9		dB
Slew rate	SR			0.15		V/µs
Mute on voltage	V_{Mute}	Note 3		1.2		V
[Power Supply] (with 2SB632K connected externally)						
Output voltage	$V_{OUT}1$	I_O = 200 mA	4.75	5.0	5.25	V
Line regulation	$\Delta V_{OLN}1$	5.6 V ≦ $V_{IN}1$ ≦ 12 V		20	100	mV
Load regulation	$\Delta V_{OLD}1$	5 mA ≦ I_O ≦ 200 mA		50	150	mV
[Reset]						
High reset output voltage	V_{ORH}	I_{ORH} = 200 µA, Cd pin open	4.73	4.98	5.23	V
Low reset output voltage	V_{ORL}	I_{SRL} = 2 mA, Cd is shorted to GND		100	200	mV
Reset threshold voltage	V_{RT}	Note 4		4.3		V
Reset hysteresis voltage	Vhys	Note 5	40	100	200	mV
Reset output delay time	t_d	Cd = 0.1 µF		10		ms

Notes:

1. Source voltage to ground when an 8 Ω load is connected between bridge amplifier outputs.
2. Sink voltage to ground when an 8 Ω load is connected between bridge amplifier outputs.
3. When the mute signal is high, all amplifier outputs turn on, and when low, all amplifier outputs turn off. When the mute signal is low, amplifier output is undefined.
4. 5 V supply voltage when the reset output goes low.
5. Potential difference from the 5 V supply voltage when the reset output goes low and when it goes high.



Truth Table

Input	MUTE	CH1		CH2		CH3		CH4	
		V_O1 (Amp1)	V_O2 (Amp2)	V_O3 (Amp3)	V_O4 (Amp4)	V_O5 (Amp5)	V_O6 (Amp6)	V_O7 (Amp7)	V_O8 (Amp8)
H	H	H	L	L	H	H	L	L	H
	L	—	—	—	—	—	—	—	—
L	H	L	H	H	L	L	H	H	L
	L	—	—	—	—	—	—	—	—

* The "—" symbol means "amplifier output is OFF."

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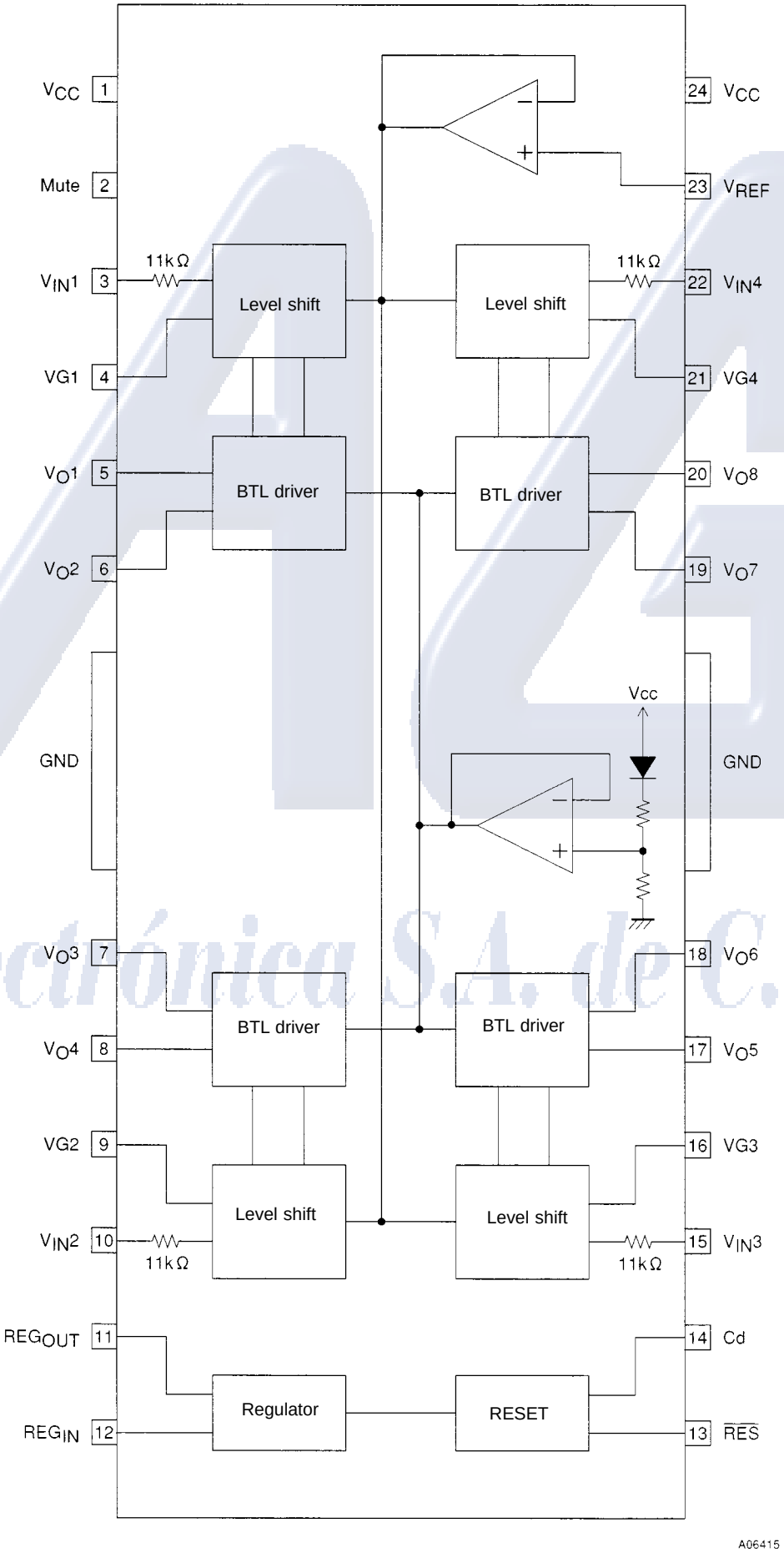
Block Diagram



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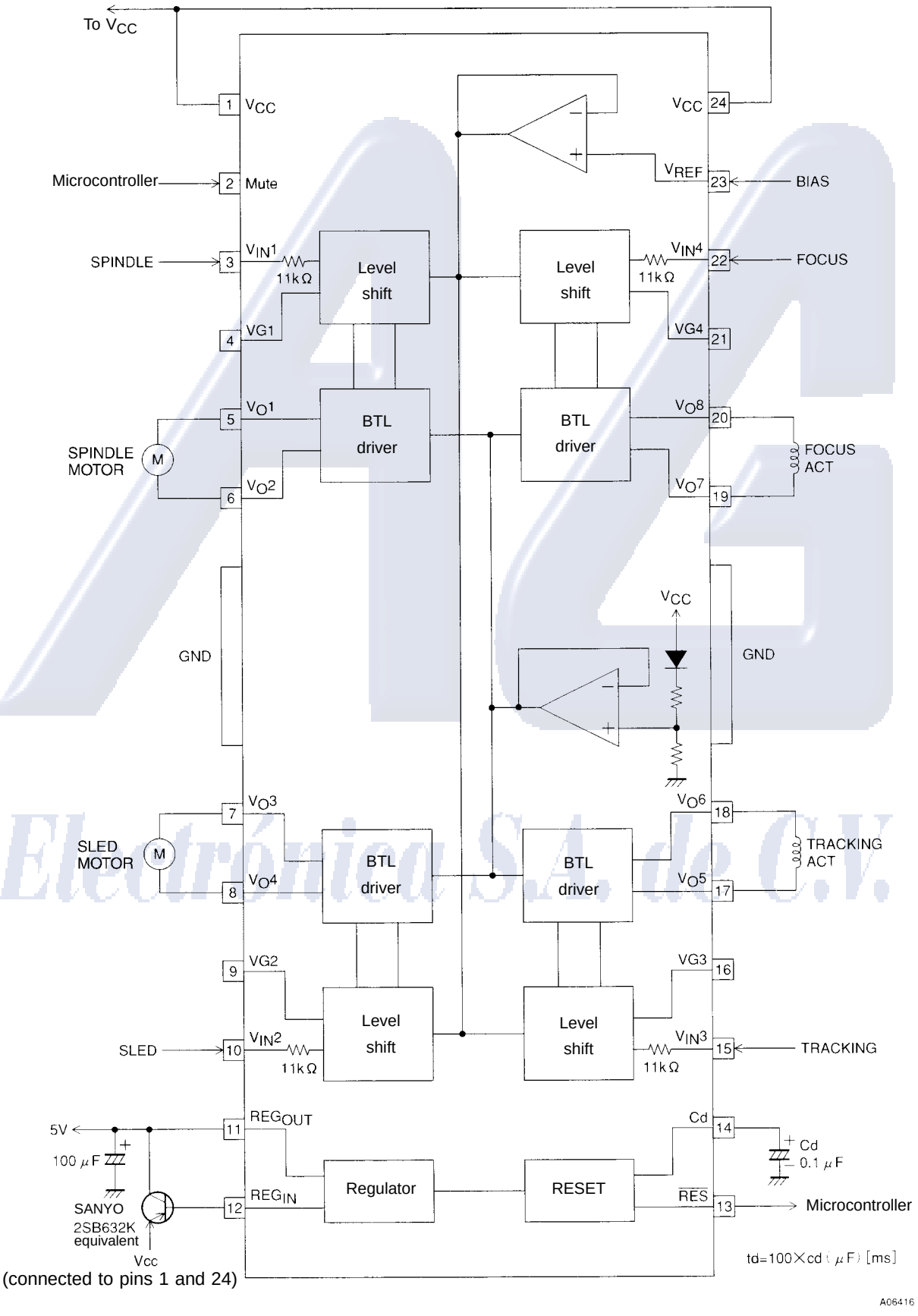
Sample Application Circuit



Note: Use a delay capacitor (Cd) whose capacitance does not change much according to the temperature.

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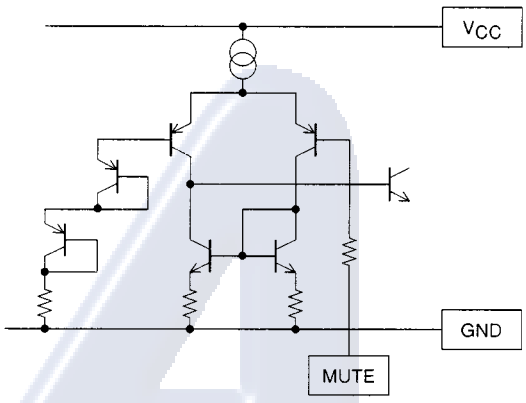
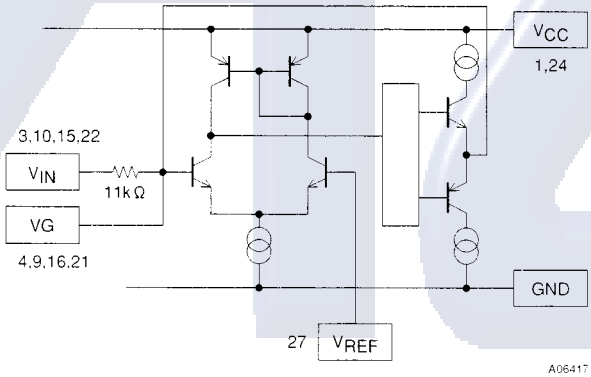
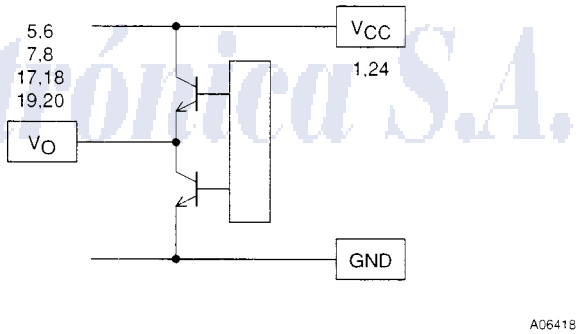
Pin Functions

Pin No.	Pin Name	Equivalent Circuit	Description
1	V_{CC}		Power supply (shorted with pin 24)
2	Mute		ON/OFF control for all BTL AMP outputs
3	$V_{IN}1$		BTL AMP 1 input
4	VG1		BTL AMP 1 input (for gain control)
9	VG2		BTL AMP 2 input (for gain control)
10	$V_{IN}2$		BTL AMP 2 input
15	$V_{IN}3$		BTL AMP 3 input
16	VG3		BTL AMP 3 input (for gain control)
21	VG4		BTL AMP 4 input (for gain control)
22	$V_{IN}4$		BTL AMP 4 input
5	V_O1		BTL AMP 1 output (non-inverting side)
6	V_O2		BTL AMP 1 output (inverting side)
7	V_O3		BTL AMP 2 output (inverting side)
8	V_O4		BTL AMP 2 output (non-inverting side)
17	V_O5		BTL AMP 3 output (non-inverting side)
18	V_O6		BTL AMP 3 output (inverting side)
19	V_O7		BTL AMP 4 output (inverting side)
20	V_O8		BTL AMP 4 output (non-inverting side)
11	REG_{OUT}		Connection for collector of external transistor (PNP); 5 V supply output
12	REG_{IN}		Connection for base of external transistor (PNP)
13	$\overline{RES}$		Reset output
14	Cd		Reset output delay time setting (with capacitor)
23	V_{REF}		Reference voltage input for level shift circuit
24	V_{CC}		Power supply (shorted with pin 1)

Note: GND (minimum electrical potential) should be connected to the center frame of the pin.

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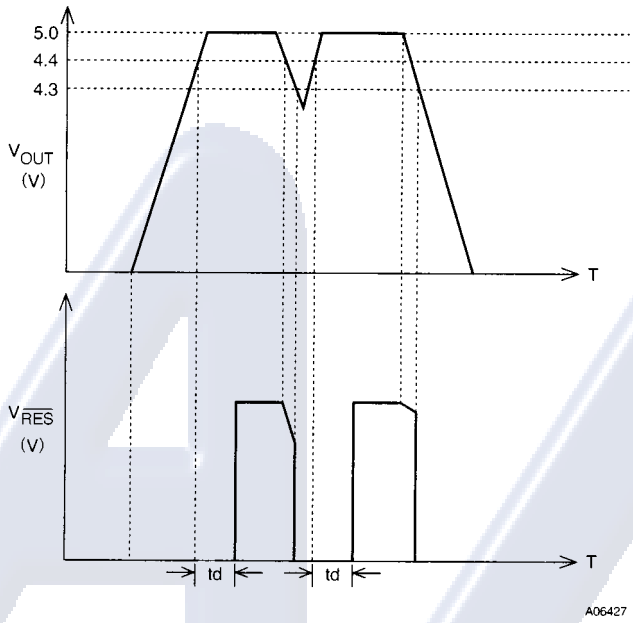
Reset Operation



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