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Ordering number : EN4973A

CMOS LSI

LC72130, 72130M

AM/FM PLL Frequency Synthesizer

Overview

The LC72130 and LC72130M are PLL frequency synthesizers for use in tuners in radio cassette recorders and other products.

Applications

PLL frequency synthesizer

Functions

- High-speed programmable dividers
  - FMIN: 10 to 160 MHz .....pulse swallower (built-in divide-by-two prescaler)
  - AMIN: 2 to 40 MHz .....pulse swallower
    0.5 to 10 MHz .....direct division
- IF counter
  - IFIN: 0.4 to 12 MHz .....AM/FM IF counter
- Reference frequencies
  - Twelve selectable frequencies (4.5 or 7.2 MHz crystal)
    1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 15, 25, 50 and 100 kHz
- Phase comparator
  - Dead zone control
  - Unlock detection
  - Deadlock clear circuit
- Built-in MOS transistor for implementing an active low-pass filter (two systems)
- Inputs and outputs
  - Dedicated output ports: five pins
  - Input or output ports: two pins
  - Clock time base output available
- Serial data I/O
  - Supports CCB format communication with the system controller.
- Operating ranges
  - Supply voltage.....4.5 to 5.5 V
  - Operating temperature.....–40 to +85°C
- Packages
  - DIP24S, MFP24S

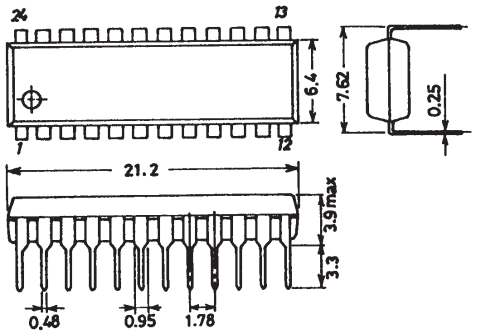
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

unit: mm

3067-DIP24S

[LC72130]

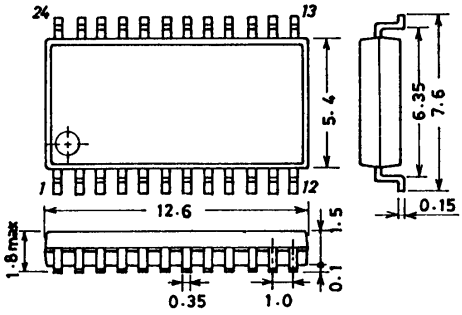


SANYO: DIP24S

unit: mm

3112-MFP24S

[LC72130M]



SANYO: MFP24S

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

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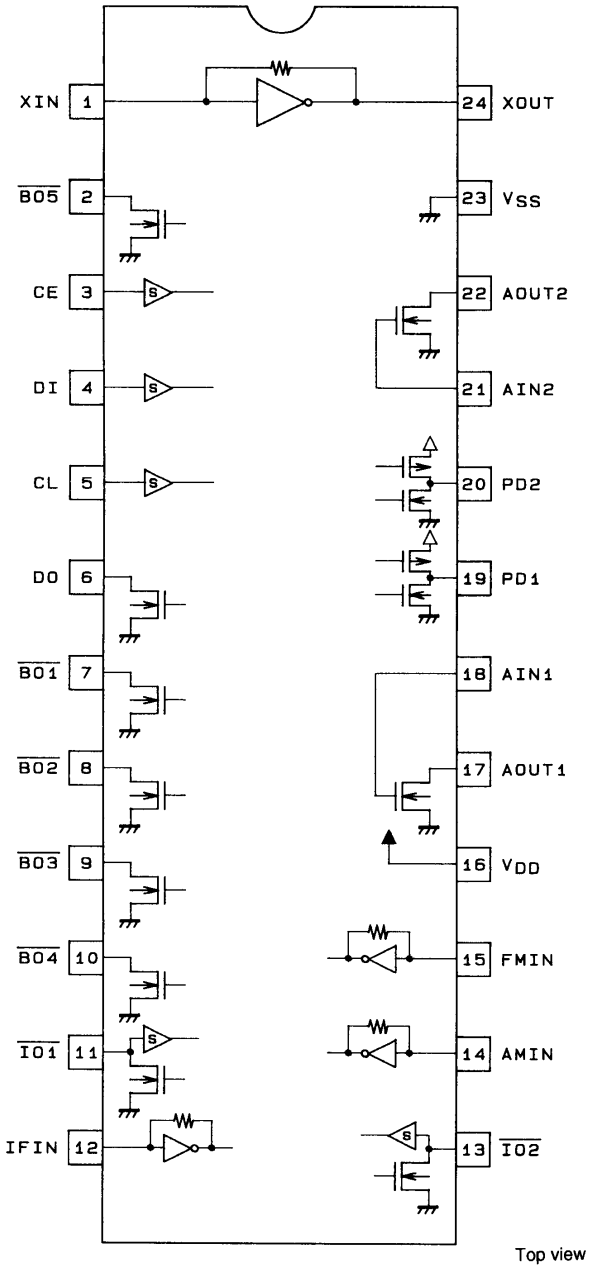
Pin Assignment



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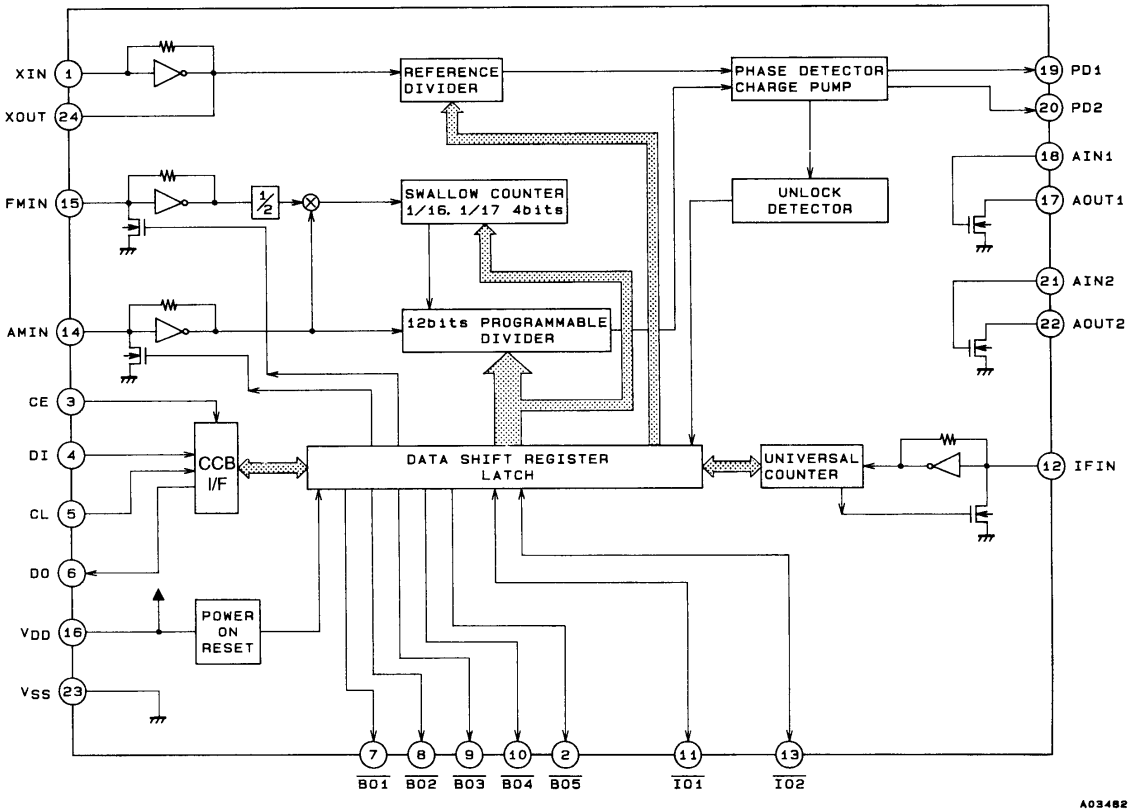
Block Diagram



Electrónica S.A. de C.V.

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

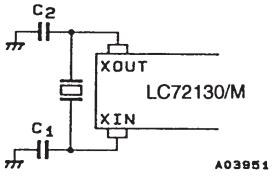
Parameter	Symbol	Pins	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CL, DI, AIN1, AIN2	–0.3 to +7.0	V
	$V_{IN}2$ max	XIN, FMIN, AMIN, IFIN	–0.3 to V_{DD} + 0.3	V
	$V_{IN}3$ max	$\overline{IO1}$, $\overline{IO2}$	–0.3 to +15	V
Maximum output voltage	V_O1 max	DO	–0.3 to +7.0	V
	V_O2 max	XOUT, PD1, PD2	–0.3 to V_{DD} + 0.3	V
	V_O3 max	$\overline{BO1}$ to $\overline{BO5}$, $\overline{IO1}$, $\overline{IO2}$, AOUT1, AOUT2	–0.3 to +15	V
Maximum output current	I_O1 max	$\overline{BO1}$	0 to 3.0	mA
	I_O2 max	DO, AOUT1, AOUT2	0 to 6.0	mA
	I_O3 max	$\overline{BO2}$ to $\overline{BO5}$, $\overline{IO1}$, $\overline{IO2}$	0 to 10.0	mA
Allowable power dissipation	Pd max	Ta ≤ 85°C	DIP24S: 350 MFP24S: 200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}		4.5		5.5	V
Input high level voltage	$V_{IH}1$	CE, CL, DI		0.7 V_{DD}		6.5	V
	$V_{IH}2$	$\overline{IO1}$, $\overline{IO2}$		0.7 V_{DD}		13	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{IO1}$, $\overline{IO2}$		0		0.3 V_{DD}	V
Output voltage	V_O1	DO		0		6.5	V
	V_O2	$\overline{BO1}$ to $\overline{BO5}$, $\overline{IO1}$, $\overline{IO2}$, AOUT1, AOUT2		0		13	V
Input frequency	$f_{IN}1$	XIN	$V_{IN}1$	1		8	MHz
	$f_{IN}2$	FMIN	$V_{IN}2$	10		160	MHz
	$f_{IN}3$	AMIN	$V_{IN}3$, SNS = 1	2		40	MHz
	$f_{IN}4$	AMIN	$V_{IN}4$, SNS = 0	0.5		10	MHz
	$f_{IN}5$	IFIN	$V_{IN}5$	0.4		12	MHz
Input amplitude	$V_{IN}1$	XIN	$f_{IN}1$	400		1500	mVrms
	$V_{IN}2$-1	FMIN	f = 10 to 130 MHz	40		1500	mVrms
	$V_{IN}2$-2	FMIN	f = 130 to 160 MHz	70		1500	mVrms
	$V_{IN}3$	AMIN	$f_{IN}3$, SNS = 1	40		1500	mVrms
	$V_{IN}4$	AMIN	$f_{IN}4$, SNS = 0	40		1500	mVrms
	$V_{IN}5$	IFIN	$f_{IN}5$, IFS = 1	40		1500	mVrms
	$V_{IN}6$	IFIN	$f_{IN}6$, IFS = 0	70		1500	mVrms
Oscillation-guaranteed crystal resonator	Xtal	XIN, XOUT	*	4.0		8.0	MHz

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Note: * Recommended crystal oscillator CI values:
CI ≤ 120Ω (For a 4.5 MHz crystal)
CI ≤ 70Ω (For a 7.2 MHz crystal)
However, since the oscillator circuit characteristics depend on the printed circuit board and component values actually used, we recommend requesting a circuit evaluation from the manufacturer of the crystal used.

<Sample Ocsillator Circuit>
Crystal oscillator: HC-49/U (manufactured by Kinseki, Ltd.), CL = 12 pF
C1 = C2 = 15 pF
The circuit constants for the crystal oscillator circuit depend on the crystal used, the printed circuit board pattern, and other items. Therefore we recommend consulting with the manufacturer of the crystal for evaluation and reliability.



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Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Built-in feedback resistance	Rf1	XIN			1.0		MΩ
	Rf2	FMIN			500		kΩ
	Rf3	AMIN			500		kΩ
	Rf4	IFIN			250		kΩ
Built-in pull-down resistor	Rpd1	FMIN			200		kΩ
	Rpd2	AMIN			200		kΩ
Hysteresis	V_{HIS}	CE, CL, DI, $\overline{IO1}$, $\overline{IO2}$			0.1 V_{DD}		V
Output high level voltage	$V_{OH}1$	PD1, PD2	IO = –1 mA	V_{DD} – 1.0			V
Output low level voltage	$V_{OL}1$	PD1, PD2	IO = 1 mA			1.0	V
	$V_{OL}2$	$\overline{BO1}$	IO = 0.5 mA			0.5	V
			IO = 1 mA			1.0	V
	$V_{OL}3$	DO	IO = 1 mA			0.2	V
			IO = 5 mA			1.0	V
	$V_{OL}4$	$\overline{BO2}$ to $\overline{BO5}$, $\overline{IO1}$, $\overline{IO2}$	IO = 1 mA			0.2	V
			IO = 5 mA			1.0	V
			IO = 8 mA			1.6	V
	$V_{OL}5$	AOUT1, AOUT2	IO = 1 mA, AIN = 1.3 V			0.5	V
Input high level current	$I_{IH}1$	CE, CL, DI	V_I = 6.5 V			5.0	V
	$I_{IH}2$	$\overline{IO1}$, $\overline{IO2}$	V_I = 13 V			5.0	µA
	$I_{IH}3$	XIN	$V_I = V_{DD}$	2.0		11	µA
	$I_{IH}4$	FMIN, AMIN	$V_I = V_{DD}$	4.0		22	µA
	$I_{IH}5$	IFIN	$V_I = V_{DD}$	8.0		44	µA
	$I_{IH}6$	AIN1, AIN2	V_I = 6.5 V			200	nA
Input low level current	$I_{IL}1$	CE, CL, DI	V_I = 0 V			5.0	µA
	$I_{IL}2$	$\overline{IO1}$, $\overline{IO2}$	V_I = 0 V			5.0	µA
	$I_{IL}3$	XIN	V_I = 0 V	2.0		11	µA
	$I_{IL}4$	FMIN, AMIN	V_I = 0 V	4.0		22	µA
	$I_{IL}5$	IFIN	V_I = 0 V	8.0		44	µA
	$I_{IL}6$	AIN1, AIN2	V_I = 0 V			200	nA
Output off leakage current	$I_{OFF}1$	$\overline{BO1}$ to $\overline{BO5}$, AOUT1, AOUT2, $\overline{IO1}$, $\overline{IO2}$	V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO	V_O = 6.5 V			5.0	µA
High level three-state off leakage current	I_{OFFH}	PD1, PD2,	$V_O = V_{DD}$		0.01	200	nA
Low level three-state off leakage current	I_{OFFL}	PD1, PD2	V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN			6		pF
Current drain	$I_{DD}1$	V_{DD}	Xtal = 7.2 MHz, $f_{IN}2$ = 130 MHz, $V_{IN}2$-1= 40 mVrms		5	10	mA
	$I_{DD}2$	V_{DD}	PLL block stopped (PLL INHIBIT), Xtal oscillator operating (Xtal = 7.2 MHz)		0.5		mA
	$I_{DD}3$	V_{DD}	PLL block stopped Xtal oscillator stopped			10	µA

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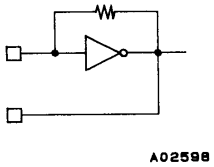
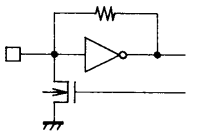
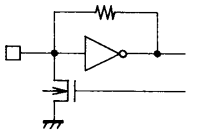
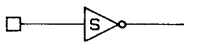
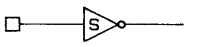
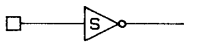
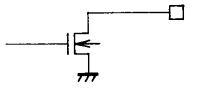
Pin Functions

Symbol	Pin No.	Type	Functions	Circuit configuration
XIN XOUT	1 24	X'tal OSC	• Crystal resonator connection (4.5/7.2 MHz)	 A02598
FMIN	15	Local oscillator signal input	• Serial data input: FMIN is selected when DVS is set to 1. • The input frequency range is from 10 to 160 MHz. • The signal is passed through a built-in divide-by-two prescaler and then supplied to the swallow counter. • Although the range of divisor settings is from 272 to 65,535, the actual divisor is twice the setting since there is also a built-in divide-by-two prescaler.	 A02599
AMIN	14	Local oscillator signal input	• Serial data input: AMIN is selected when DVS is set to 0. • Serial data input: When SNS is set to 1: — The input frequency range is from 2 to 40 MHz. — The signal is supplied directly to the swallow counter. — The range of divisor settings is from 272 to 65,535 and the actual divisor will be the value set. • Serial data input: When SNS is set to 0: — The input frequency range is from 0.5 to 10 MHz. — The signal is supplied directly to a 12-bit programmable divider. — The range of divisor settings is from 4 to 4,095 and the actual divisor will be the value set.	 A02599
CE	3	Chip enable	• Must be set high when serial data is input to the LC72130 (DI), or when serial data is output (DO).	 A02600
CL	5	Clock	• Used as the synchronization clock when serial data is input to the LC72130 (DI), or when serial data is output (DO).	 A02600
DI	4	Data input	• Inputs serial data sent from the controller to the LC72130.	 A02600
DO	6	Data output	• Outputs serial data sent from the LC72130 to the controller. The content of the output data is determined by the serial data DOC0 to DOC2.	 A02601
V_{DD}	16	Power supply	• The LC72130 power supply (V_{DD} = 4.5 to 5.5 V) • The power on reset circuit operates when power is first applied.	-

Continued on next page.

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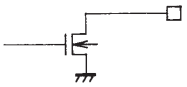
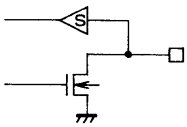
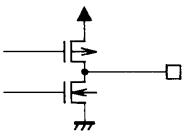
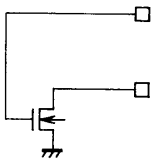
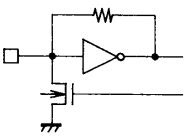
Continued from preceding page.

Symbol	Pin No.	Type	Functions	Circuit configuration
V_{SS}	23	Ground	• The LC72130 ground	—
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$ $\overline{BO5}$	7 8 9 10 2	Output port	• Dedicated output pins • The output states are determined by BO1 to BO5 in the serial data. Data: 0 = open, 1 = low • These pins go to the open state after the power on reset. • An 8 Hz time base signal can be output from $\overline{BO1}$ when TBC in the serial data is set to 1. • Note that the ON impedance of the $\overline{BO1}$ pin is higher than that of the other pins ($\overline{BO2}$ to $\overline{BO5}$).	 A02601
$\overline{IO1}$ $\overline{IO2}$	11 13	I/O port	• Pins used for both input and output • The input or output state is determined by bits IOC1 and IOC2 in the serial data. Data: 0 = input port, 1 = output port • When specified for use as an input port: The input state is transmitted to the controller through the DO pin. Input state: Low → data value = 0 High → data value = 1 • When specified for use as an output port: The output state is determined by bits IO1 and IO2 in the serial data. Data: 0 = open, 1 = low • These pins go to the input port state after the power ON reset.	 A02602
PD1 PD2	19 20	Charge pump output	• PLL charge pump output When the frequency generated by dividing the local oscillator frequency by N is higher than the reference frequency, a high level will be output from the PD pin. Similarly, when that frequency is lower, a low level will be output. The PD pin goes to the high impedance state when the frequencies agree.	 A02603
AIN1 AOUT1 AIN2 AOUT2	18 17 21 22	LPF amplifier transistor	• The MOS transistor used for the PLL active low-pass filter.	 A02604
IFIN	12	IF counter	• The input frequency range is from 0.4 to 12 MHz. • The signal is supplied directly to the IF counter. • The result from the IF counter MSB is output through the DO pin. • There are four measurement periods: 4, 8, 32, or 64 ms.	 A02599

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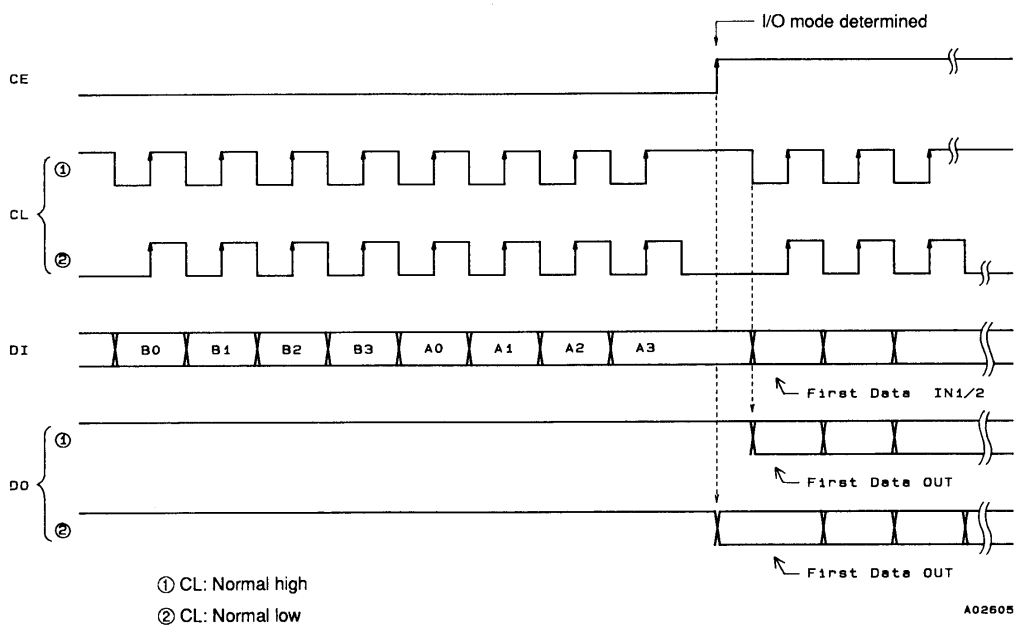
Serial Data I/O Methods

The LC72130 uses Sanyo's audio LSI serial bus format, the CCB (computer control bus) format, for data I/O. This LSI adopts an 8-bit address version of the CCB format.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	• This is a control data input (serial data input) mode. • 24 bits of data are input. • See the "DI Control Data (Serial Data Input)" item for a description of the contents of the input data.
2	IN2 (92)	1	0	0	1	0	1	0	0	• This is a control data input (serial data input) mode. • 24 bits of data are input. • See the "DI Control Data (Serial Data Input)" item for a description of the contents of the input data.
3	OUT (A2)	0	1	0	1	0	1	0	0	• This is a data output (serial data output) mode. • The number of bits output is equal to the number of clock cycles. • See the "DO Control Data (Serial Data Output)" item for a description of the content of the output data.



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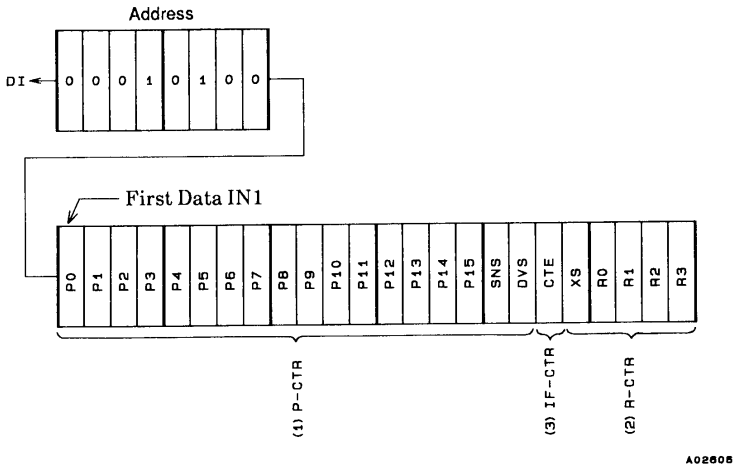
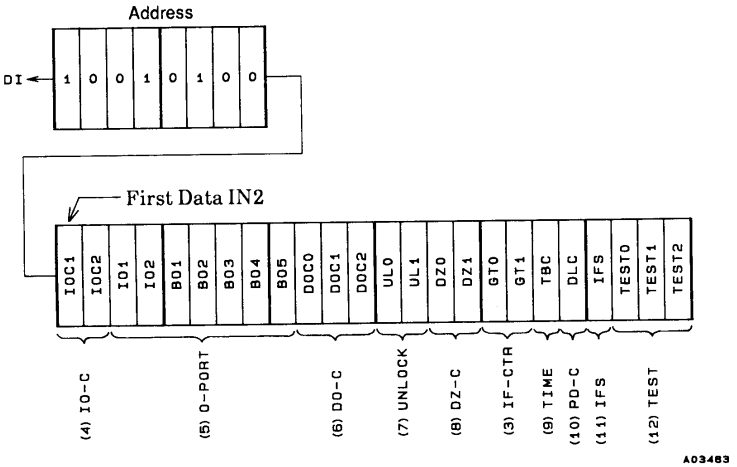
1. DI Control Data (Serial Data Input)

• IN1 Mode



• IN2 Mode



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2. DI Control Data Functions

<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15

DVS, SNS</td><td>• Sets the programmable divider divisor.
This value is a binary value whose MSB is P15. The position of the LSB varies depending on DVS and SNS. (*: don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr>
</table>
Note: P0 to P3 are ignored when P4 is the LSB.
• These bits select the signal input pin for the programmable divider and switch the input frequency range. (*: don’t care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160 MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
Note: See the “Programmable Divider” item for more information.</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data
R0 to R3

XS</td><td>• Selects the reference frequency (fref).
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X’tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
Note: PLL INHIBIT
The programmable divider block and the IF counter block are stopped, the FMIN, AMIN, and IFIN pins are set to the pull-down state (ground), and the charge pump goes to the high impedance state.
• Crystal resonator selection
XS = 0: 4.5 MHz
XS = 1: 7.2 MHz
The 7.2 MHz frequency is selected after the power ON reset.</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data
CTE

GT0, GT1</td><td>• IF counter measurement start data
CTE = 1: Counter start
CTE = 0: Counter reset
• Determines the IF counter measurement period.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th><th>Wait time (ms)</th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
Note: See the “IF Counter” item for more information.</td><td>IFS</td></tr>
<tr><td>(4)</td><td>I/O port specification data
IOC1, IOC2</td><td>• Specifies the I/O direction for the bidirectional pins $\overline{IO1}$ and $\overline{IO2}$.
Data: 0 = input mode, 1 = output mode</td><td></td></tr>
<tr><td>(5)</td><td>Output port data
BO1 to BO5, IO1, IO2</td><td>• Data that determines the output from the $\overline{BO1}$ to $\overline{BO5}$, $\overline{IO1}$ and $\overline{IO2}$ output ports
Data: 0 = open, 1 = low
• The data = 0 (open) state is selected after the power ON reset.</td><td>IOC1
IOC2</td></tr>
</table>

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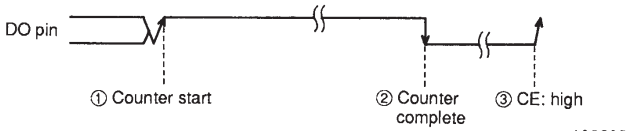
<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(6)</td><td>DO pin control data
DOC0, DOC1, DOC2</td><td>
• Data that determines the DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC*1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>The $\overline{IO1}$ pin state*2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The IO2 pin state*2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
The open state is selected after the power ON reset.
Note: 1. end-UC: Check for IF counter measurement completion


① When end-UC is set and the IF counter is started (i.e., when CTE is changed from zero to one), The DO pin automatically goes to the open state.
② When the IF counter measurement completes, the DO pin goes low to indicate the measurement completion state.
③ Depending on serial data I/O (CE: high) the DO pin goes to the open state.
2. Goes to the open state if the I/O pin is specified to be an output port.
Caution: The state of the DO pin during a data input period (an IN1 or IN2 mode period with CE high) will be open, regardless of the state of the DO control data (DOC0 to DOC2). Also, the DO pin during a data output period (an OUT mode period with CE high) will output the contents of the internal DO serial data in synchronization with the CL pin signal, regardless of the state of the DO control data (DOC0 to DOC2).
</td><td>UL0, UL1,
CTE,
IOC1, IOC2</td></tr>
<tr><td>(7)</td><td>Unlock detection data
UL0, UL1</td><td>
• Selects the phase error (øE) detection width for checking PLL lock.
A phase error in excess of the specified detection width is seen as an unlocked state.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detector output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr>
<tr><td>1</td><td>0</td><td>±0.55 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
<tr><td>1</td><td>1</td><td>±1.11 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
</table>
Note: In the unlocked state the DO pin goes low and the UL bit in the serial data becomes zero.
</td><td>DOC0,
DOC1,
DOC2</td></tr>
<tr><td>(8)</td><td>Phase comparator control data
DZ0, DZ1</td><td>
• Controls the phase comparator dead zone.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead zone widths: DZA < DZB < DZC < DZD
</td><td></td></tr>
<tr><td>(9)</td><td>Clock time base
TBC</td><td>Setting $\overline{TBC}$ to one causes an 8 Hz, 40% duty clock time base signal to be output from the $\overline{BO1}$ pin. (BO1 data is invalid in this mode.)</td><td>BO1</td></tr>
<tr><td>(10)</td><td>Charge pump control data
DLC</td><td>
• Forcibly controls the charge pump output.
<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Forced low</td></tr>
</table>
Note: If deadlock occurs due to the VCO control voltage (Vtune) going to zero and the VCO oscillator stopping, deadlock can be cleared by forcing the charge pump output to low and setting Vtune to V_{CC}. (This is the deadlock clearing circuit.)
</td><td></td></tr>
</table>

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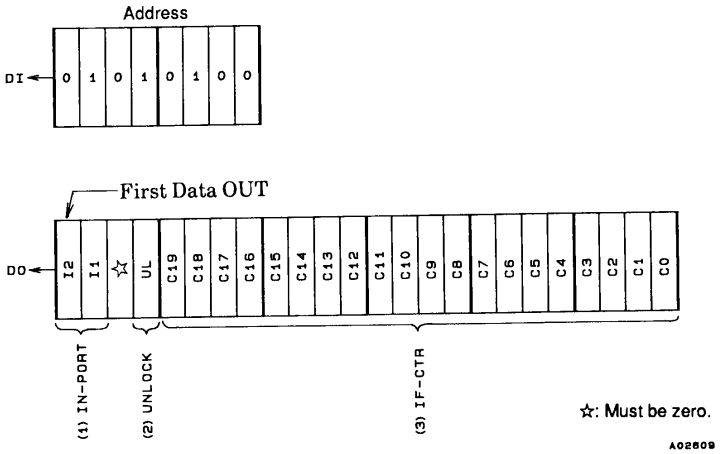
No.	Control block/data	Functions	Related data
(11)	IF counter control data	• Note that if this value is set to zero the system enters input sensitivity degradation mode, and the sensitivity is reduced to 10 to 30 mV rms. * See the “IF Counter Operation” item for details.	
(12)	LSI test data TEST 0 to TEST2	• LSI test data TEST0 TEST1 TEST2 } These values must all be set to 0. These test data are set to 0 automatically after the power ON reset.	

3. DO Output Data (Serial Data Output)

- OUT Mode



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4. DO Output Data

No.	Control block/data	Functions	Related data
(1)	I/O port data I2, I1	• Latched from the pin states of the $\overline{IO1}$ and $\overline{IO2}$ I/O ports. • These values follow the pin states regardless of the input or output setting. • Data is latched at the point where the circuit enters data output mode (OUT mode) I1 ← $\overline{IO1}$ pin state } High: 1 I2 ← $\overline{IO2}$ pin state } Low: 0	IOC1, IOC2
(2)	PLL unlock data UL	• Latched from the state of the unlock detection circuit. UL ← 0: Unlocked UL ← 1: Locked or detection stopped mode	UL0, UL1
(3)	IF counter binary data C19 to C0	• Latched from the value of the IF counter (20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE, GT0, GT1

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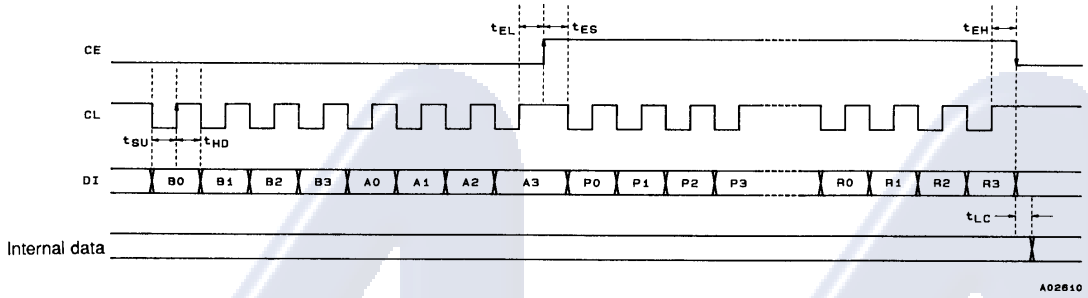
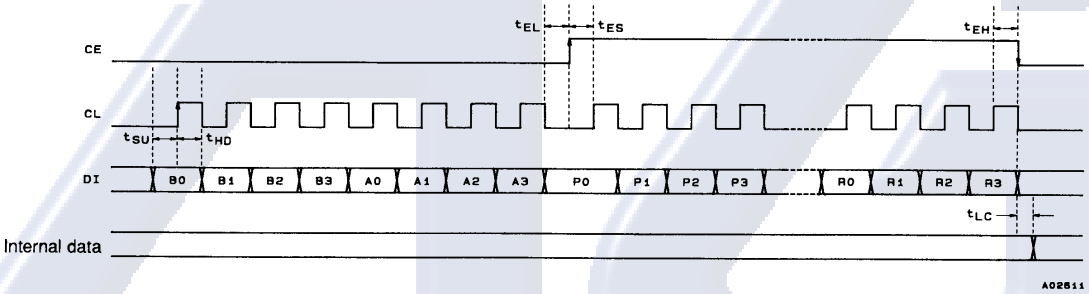
5. Serial Data Input (IN1/IN2) t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.75$ µs, $t_{LC} \leq 0.75$ µs

① CL: Normal high

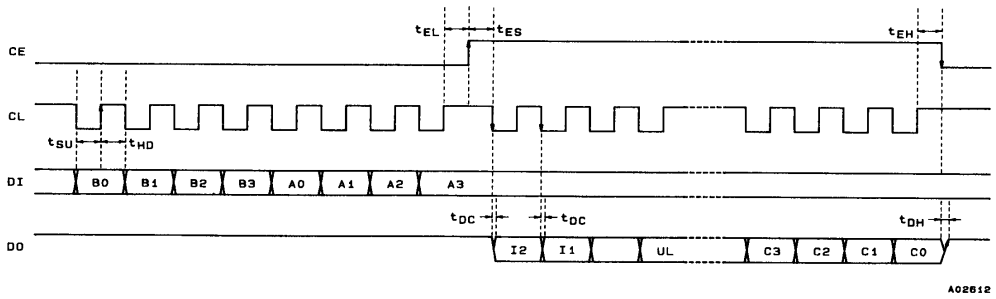


② CL: Normal low

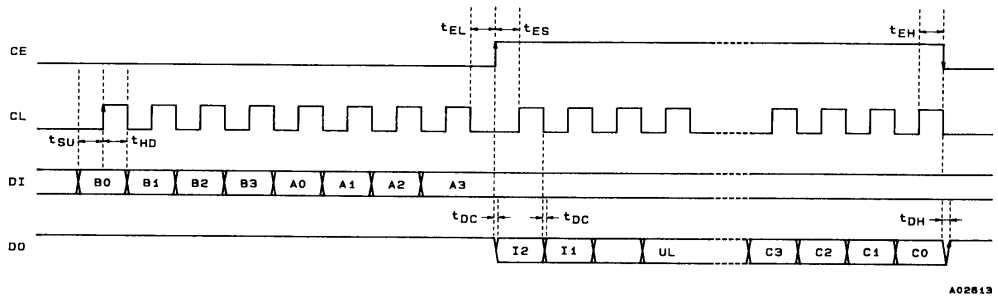


6. Serial Data Output (OUT) t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.75$ µs, t_{DC}, $t_{DH} \leq 0.35$ µs

① CL: Normal high



② CL: Normal low



Note: Since the DO pin is an n-channel open drain pin, the time for the data to change (t_{DC} and t_{DH}) will differ depending on the value of the pull-up resistor and printed circuit board capacitance.

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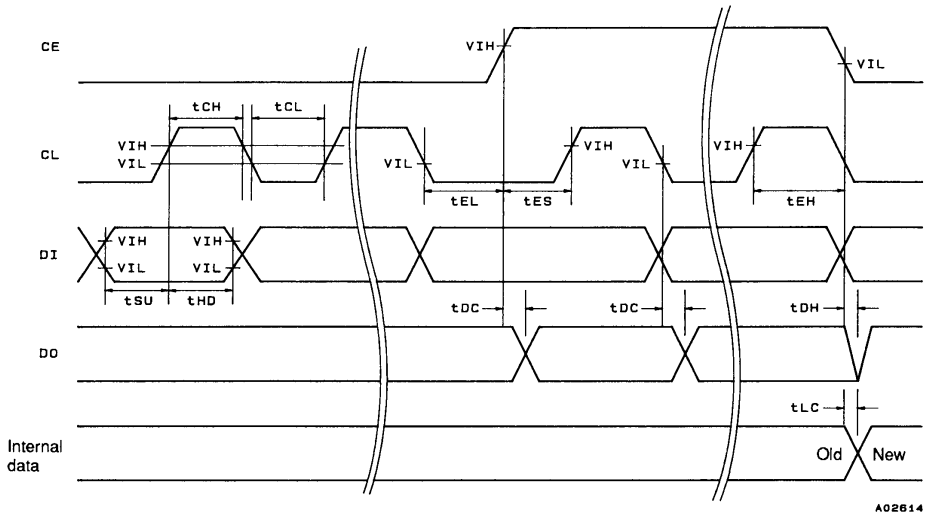
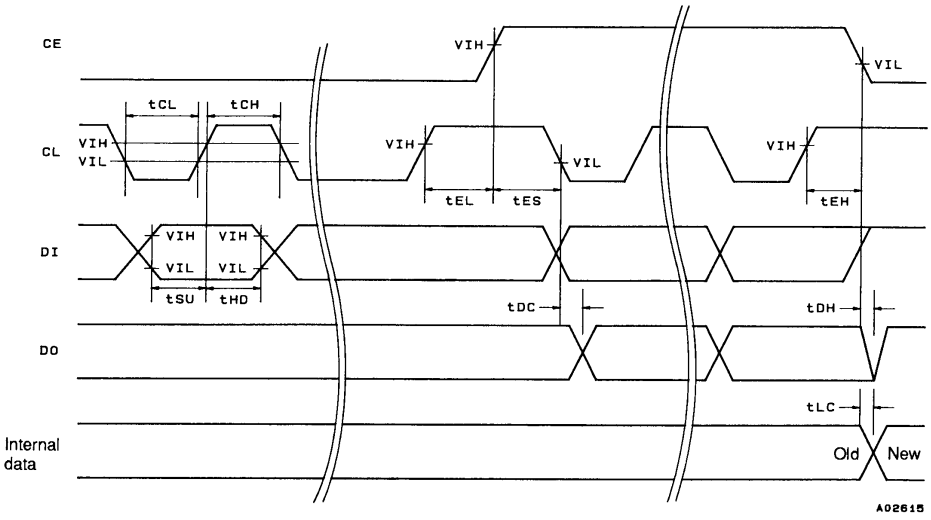
7. Serial Data Timing



When stopped with CL low



When stopped with CL high

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Data setup time	t_{SU}	DI, CL		0.75			µs
Data hold time	t_{HD}	DI, CL		0.75			µs
Clock low-level time	t_{CL}	CL		0.75			µs
Clock high-level time	t_{CH}	CL		0.75			µs
CE wait time	t_{EL}	CE, CL		0.75			µs
CE setup time	t_{ES}	CE, CL		0.75			µs
CE hold time	t_{EH}	CE, CL		0.75			µs
Data latch change time	t_{LC}					0.75	µs
Data output time	t_{DC}	DO, CL	Differs depending on the value of the pull-up resistor and the printed circuit board capacitance.			0.35	µs
	t_{DH}	DO, CE					

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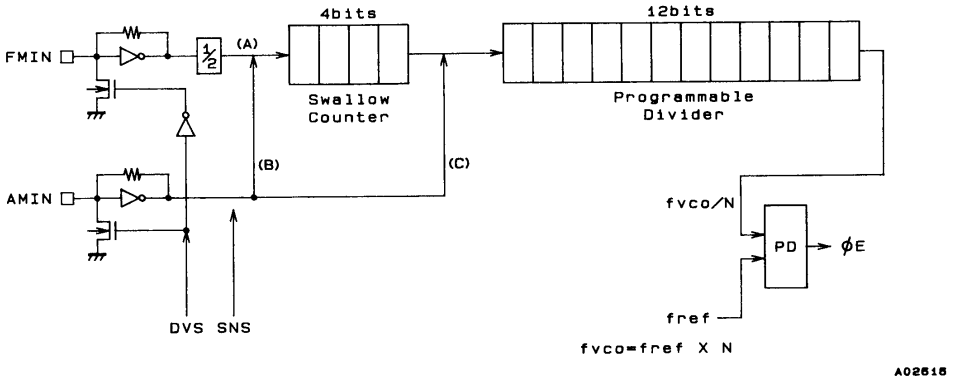
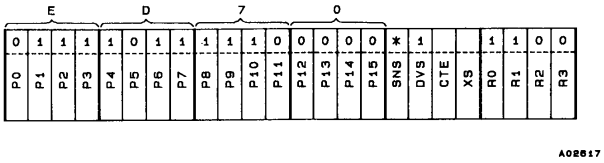
Programmable Divider



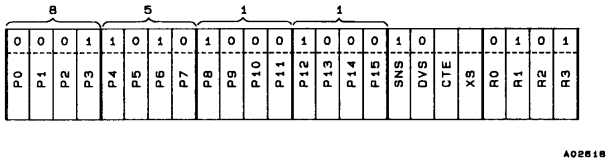
	DVS	SNS	Input pin	Set divisor	Actual divisor: N	Input frequency range (MHz)
A	1	*	FMIN	272 to 65535	Twice the set value	10 to 160
B	0	1	AMIN	272 to 65535	The set value	2 to 40
C	0	0	AMIN	4 to 4095	The set value	0.5 to 10

Note: * Don't care.

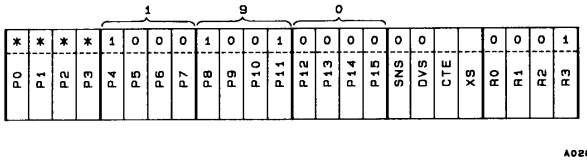
1. Programmable Divider Calculation Examples
   - FM, 50 kHz steps (DVS = 1, SNS = *, FMIN selected)
     FM RF = 90.0 MHz (IF = +10.7 MHz)
     FM VCO = 100.7 MHz
     PLL fref = 25 kHz (R0 to R1 = 1, R2 to R3 = 0)
     100.7 MHz (FM VCO) ÷ 25 kHz (fref) ÷ 2 (FMIN: divide-by-two prescaler) = 2014 → 07DE (HEX)



   - SW, 5 kHz steps (DVS = 0, SNS = 1, AMIN high speed side selected)
     SW RF = 21.75 MHz (IF = +450 kHz)
     SW VCO = 22.20 MHz
     PLL fref = 5 kHz (R0 = R2 = 0, R1 = R3 = 1)
     22.2 MHz (SW VCO) ÷ 5 kHz (fref) = 4440 → 1158 (HEX)



   - MW, 10 kHz steps (DVS = 0, SNS = 0, AMIN low-speed side selected)
     MW RF = 1000 kHz (IF = +450 kHz)
     MW VCO = 1450 kHz
     PLL fref = 10 kHz (R0 to R2 = 0, R3 = 1)
     1450 kHz (MW VCO) ÷ 10 kHz (fref) = 145 → 091 (HEX)



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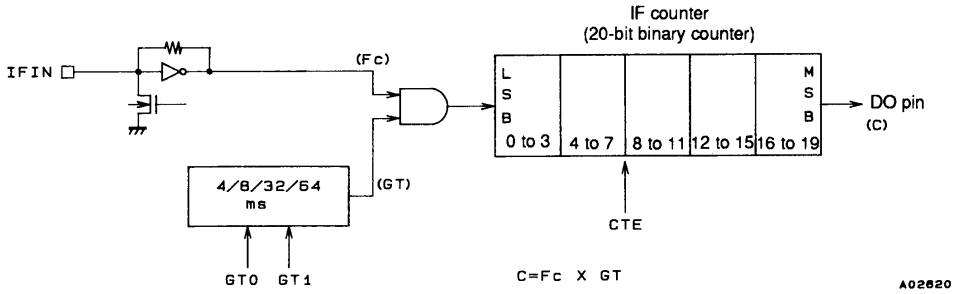
IF Counter

The LC72130 IF counter is a 20-bit binary counter. The result, i.e., the counter's msb, can be read serially from the DO pin.



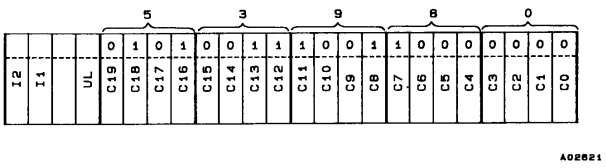
GT1	GT0	Measurement time	
		Measurement period (GT) (ms)	Wait time (twu) (ms)
0	0	4	3 to 4
0	1	8	3 to 4
1	0	32	7 to 8
1	1	64	7 to 8

The IF frequency (Fc) is measured by determining how many pulses were input to an IF counter in a specified measurement period, GT.

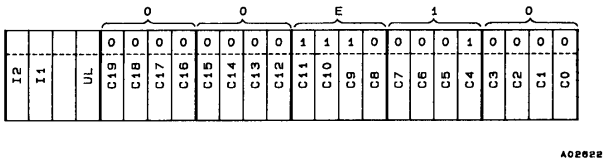
$$Fc = \frac{C}{GT} \qquad (C = Fc \times GT) \qquad C: \text{Count value (number of pulses)}$$

1. IF Counter Frequency Calculation Examples

- When the measurement period (GT) is 32 ms, the count (C) is 53980 hexadecimal (342400 decimal):
  IF frequency (Fc) = 342400 ÷ 32 ms = 10.7 MHz



- When the measurement period (GT) is 8 ms, the count (C) is E10 hexadecimal (3600 decimal):
  IF frequency (Fc) = 3600 ÷ 8 ms = 450 kHz



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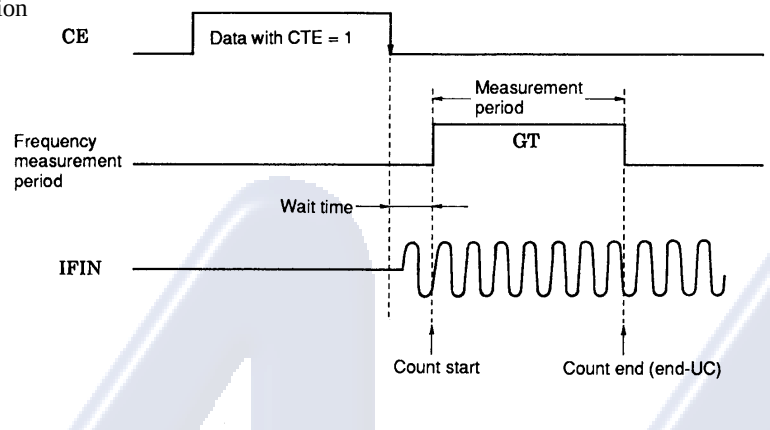
2. IF Counter Operation



Prior to starting the IF counter, reset the IF counter in advance by setting CTE in the serial data to zero.

The IF counter is started by changing the value of CTE in the serial data from zero to one. The serial data is latched when the CE pin is dropped from high to low. The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest. Next, the value of the IF counter at the end of the measurement period must be read out during the period that CTE is 1. This is because the IF counter is reset when CTE is set to 0.

Note: When operating the IF counter, the control microprocessor must check for the presence of the IF-IC SD (station detect signal) and, must turn on the IF buffer output and operate the counter only if the SD signal is present. Autosearch techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

IFIN minimum input sensitivity standard

f (MHz)

IFS	0.4 ≤ f < 0.5	0.5 ≤ f < 8	8 ≤ f ≤ 12
1: Normal mode	40 mVrms (0.1 to 3 mVrms)	40 mVrms	40 mVrms (1 to 10 mVrms)
0: Degradation mode	70 mVrms (10 to 15 mVrms)	70 mVrms	70 mVrms (30 to 40 mVrms)

( ): Actual values (reference data)

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Unlock Detection Timing

1. Unlock Detection Determination Timing

Unlocked state detection is performed in the reference frequency (fref) period (interval). Therefore, in principle, this determination must be performed over a period no less than the reference frequency period. However, directly following a change to the (frequency) divisor N, that determination must be performed after at least two reference frequency periods have passed.

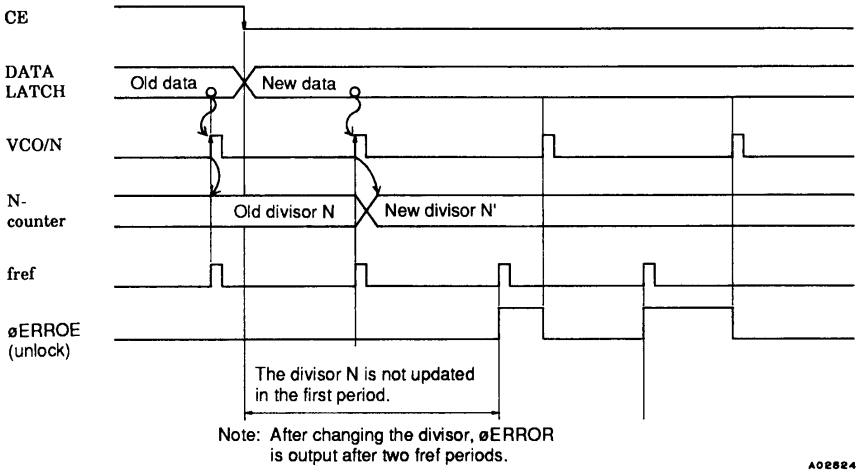

Figure 1 Unlocked State Detection Timing

For example, if fref is 1 kHz, i.e., the period is 1 ms, after the divisor N is changed, unlocked state determination must be performed after waiting 2 ms.

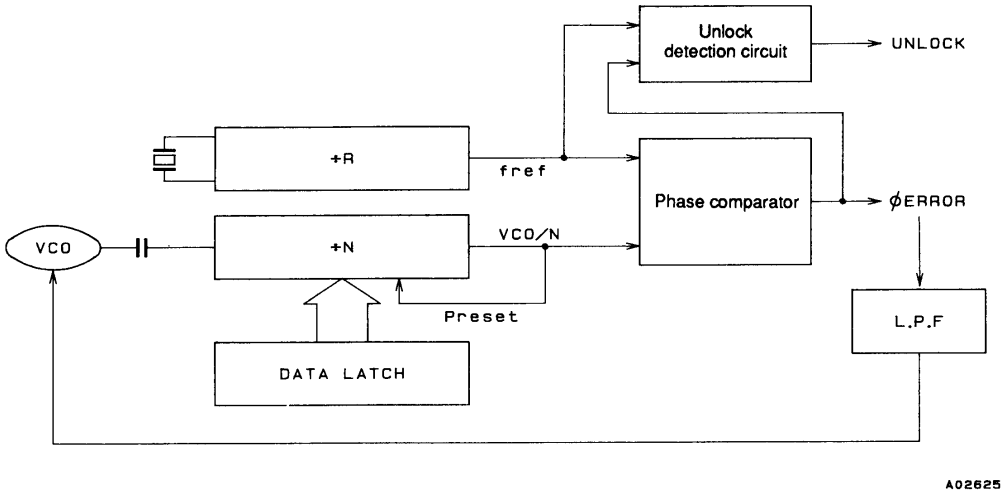

Figure 2 Circuit Structure

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2. Unlock Determination Software Integration Method

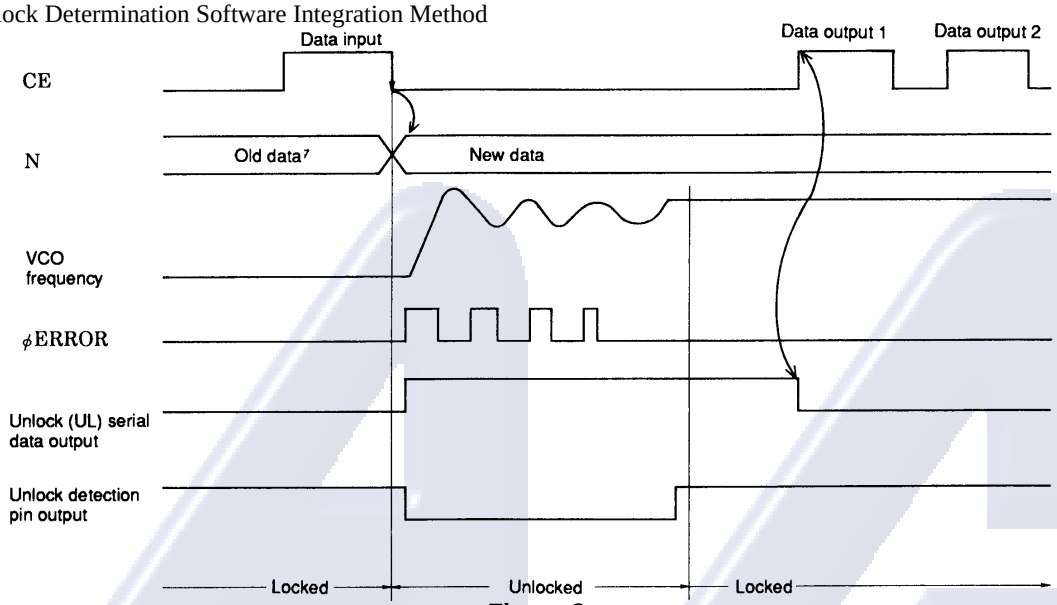
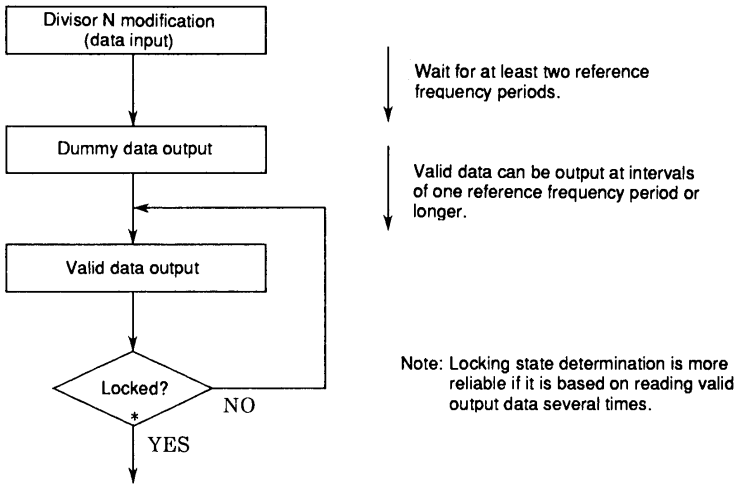


Figure 3

3. Unlocked State Data Output Using Serial Data Output

In the LC72130, once an unlocked state occurs, the unlocked state serial data (UL) will not be reset until a data input (or output) operation is performed. At the data output 1 point in Figure 3, although the VCO frequency has stabilized (locked), since no data output has been performed since the divisor N was changed the unlocked state data remains in the unlocked state. As a result, even though the frequency has stabilized (locked), the system remains (from the standpoint of the data) in the unlocked state.

Therefore, the unlocked state data acquired at data output 1, which occurs immediately after the divisor N was changed, should be treated as a dummy data output and ignored. The second data output (data output 2) and following outputs are valid data.



Locked State Determination Flowchart

4. Directly Outputting Unlocked State Data from the DO Pin (Set by the DO pin control data)

Since the locking state (high = locked, low = unlocked) is output directly from the DO pin, the dummy data processing described in section 3 above is not required. After changing the divisor N, the locking state can be checked after waiting at least two reference frequency periods.

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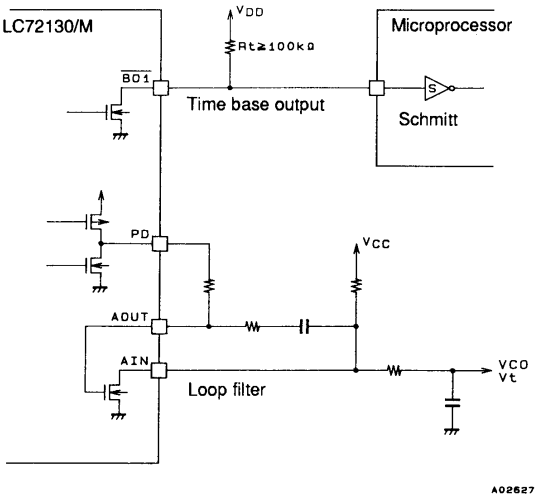
Clock Time Base Usage Notes

The pull-up resistor used on the clock time base output pin ($\overline{BO1}$) should be at least 100 kΩ. Also, to prevent chattering we recommend using a Schmitt input at the controller (microprocessor) that receives this signal.

This is to prevent degrading the VCO C/N characteristics when a loop filter is formed using the built-in low-pass filter transistor. Since the clock time base output pin and the low-pass filter have a common ground internal to the IC, it is necessary to minimize the time base output pin current fluctuations and to suppress their influence on the low-pass filter.



Other Items

1. Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	– –0 s
0	1	DZB	ON/ON	–0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	+ +0 s

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.

- Side band generation due to reference frequency leakage
- Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/OFF) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/R ratio in excess of 90 to 100 dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

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Dead Zone

The phase comparator compares fp to a reference frequency (fr) as shown in Figure 4. Although the characteristics of this circuit (see Figure 5) are such that the output voltage is proportional to the phase difference ø (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.

However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularly-priced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

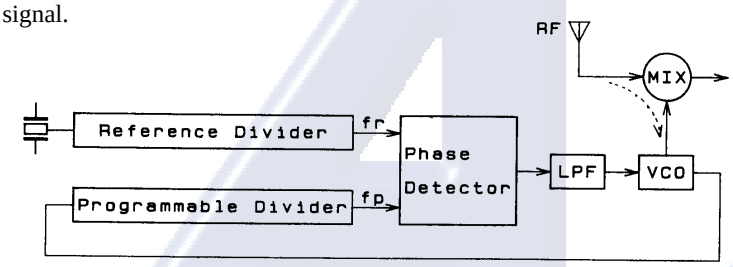

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Figure 4

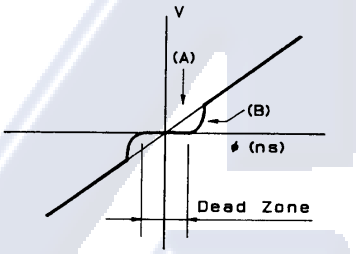

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Figure 5

2. Notes on the FMIN, AMIN, and IFIN Pins

   Coupling capacitors must be placed as close as possible to their respective pin. A capacitance of about 100 pF is desirable. In particular, if a capacitance of 1000 pF or over is used for the IF pin, the time to reach the bias level will increase and incorrect counting may occur due to the relationship with the wait time.

3. Notes on IF Counting → SD must be used in conjunction with the IF counting time

   When using IF counting, always implement IF counting by having the microprocessor determine the presence of the IF-IC SD (station detect) signal and turn on the IF counter buffer only if the SD signal is present. Schemes in which auto-searches are performed with only IF counting are not recommended, since they can stop at points where there is no signal due to leakage output from the IF counter buffer.

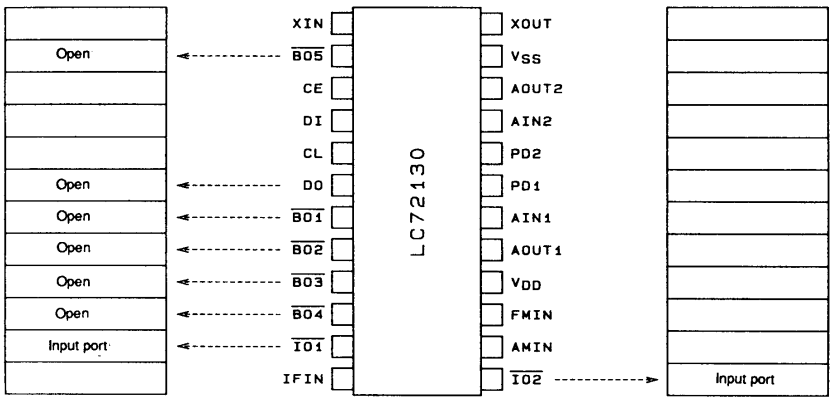
4. DO Pin Usage Techniques

   In addition to data output mode times, the DO pin can also be used to check for IF counter count completion and for unlock detection output. Also, an input pin state can be output unchanged through the DO pin and input to the controller.

5. Power Supply Pins

   A capacitor of at least 2000 pF must be inserted between the power supply V_{DD} and V_{SS} pins for noise exclusion. This capacitor must be placed as close as possible to the V_{DD} and V_{SS} pins.

Pin States After the Power ON Reset



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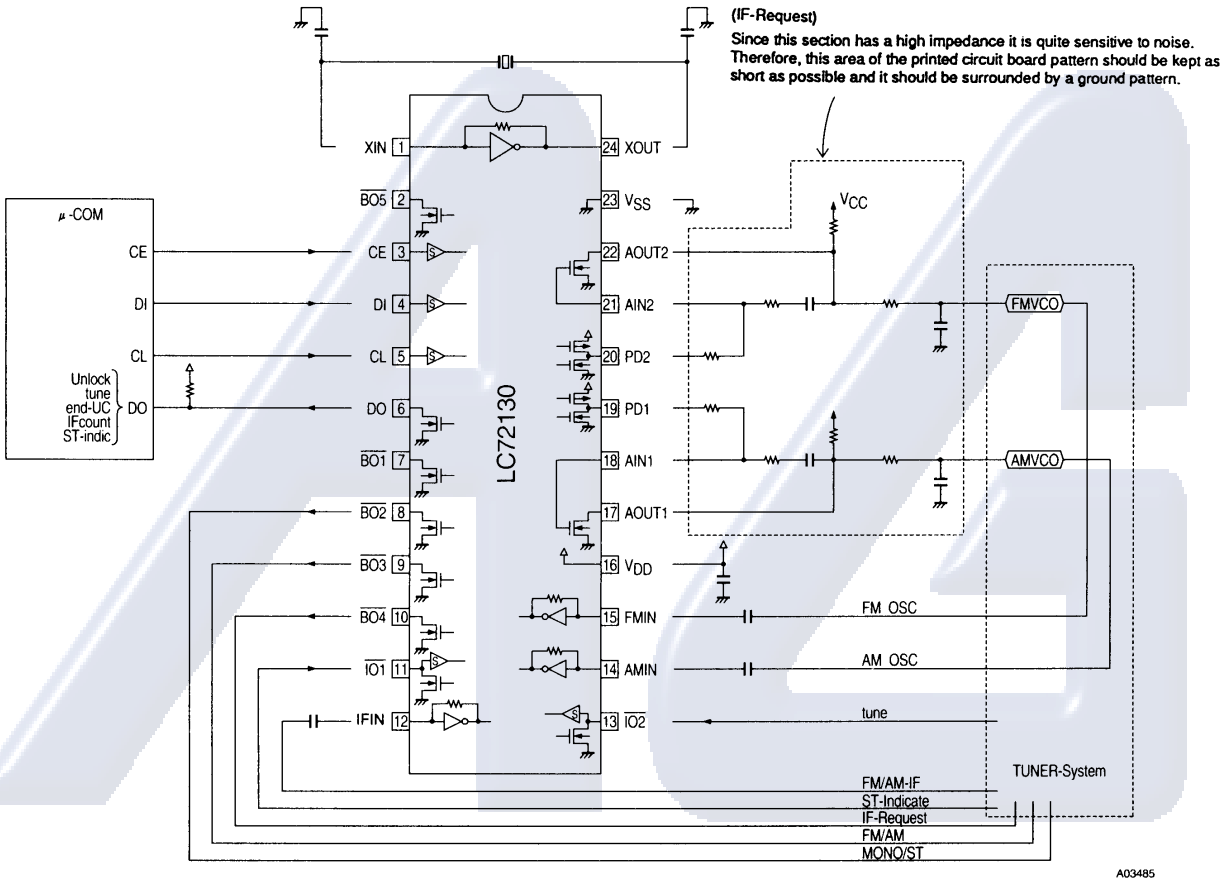
Sample Application System



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