

Ordering number : EN5466

CMOS LSI

SANYO**LC75394NE****Single-Chip Electronic Volume Control System****Overview**

The LC75394NE is an electronic volume control system providing control over volume, balance, 5-band equalizer, and input switching based on serial inputs.

Functions

• Volume control:

The chip provides 25 levels of volume attenuation: in 2-dB steps between 0 dB and -20 dB, 3-dB steps between -20 dB and -32 dB, 4-dB steps between -32 dB and -52 dB, 4.5-dB steps between -52 dB and -70 dB, and -∞. Independent control over left and right channels provides balance control.

• Equalizer:

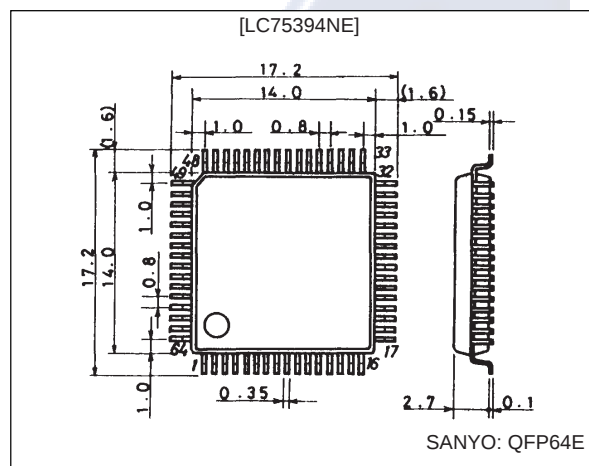
The chip provides control in 2-dB steps over the range between +10 dB and -10 dB. Four of the five bands have peaking equalization; the remaining one, shelving equalization.

• Selector:

The left and right channels each offer a choice of four inputs. An external constant determines the amplification for the input signal.

Package Dimensions

unit: mm

3159-QFP64E**Features**

- Built-in buffer amplifiers reduce the number of external parts necessary.
- Silicon gate CMOS reduces switching noise.
- Serial data input
 - Supports CCB* format communication with the system controller.
- A built-in reference voltage circuit divides the supply voltage (V_{DD}) in half.

*

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Specifications**Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	12	V
Maximum input voltage	$V_{IN\text{ max}}$	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 85^\circ\text{C}$	310	mW
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

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91096HA (OT)/81095HA (OT) No. 5466-1/17

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Allowable Operating Ranges at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		11.0	V
Input high level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, L1 to L4, R1 to R4, LTIN, RTIN, LVRIN, RVRIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	t_{PW}	CL	1.0			μs
Setup time	t_{SETUP}	CL, DI, CE	1.0			μs
Hold time	t_{HOLD}	CL, DI, CE	1.0			μs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 10\text{ V}$, $V_{SS} = 0\text{ V}$

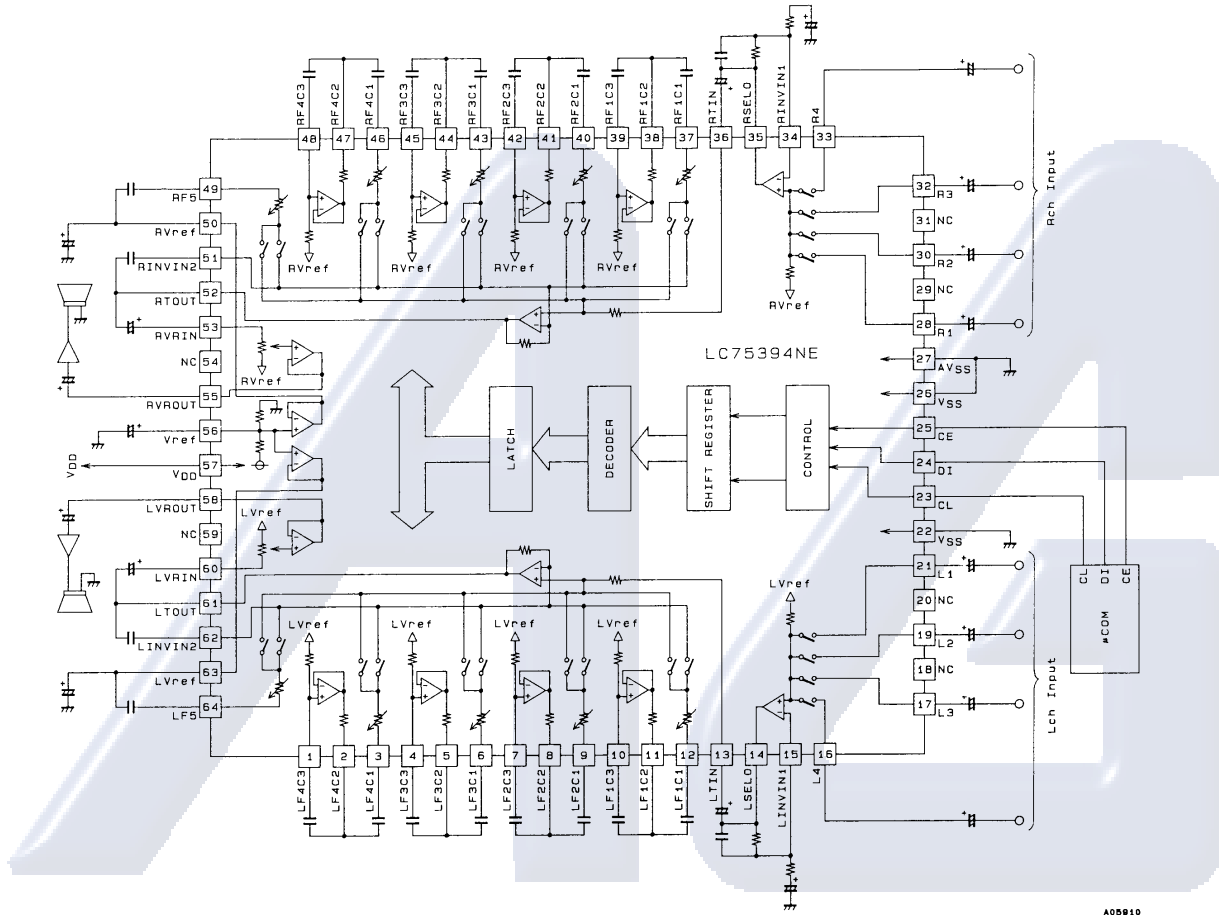
Parameter	Symbol	Conditions	min	typ	max	Unit
[Input block]						
Input resistance	R_{in}	L1 to L4, R1 to R4		1		M Ω
Clipping level	V_{cl}	LSELO, RSELO: THD = 1.0%		2.65		Vrms
Output load resistance	R_L	LSELO, RSELO	3			k Ω
[Volume control block]						
Input resistance	R_{in}	LVRIN, RVRIN	60	100	140	k Ω
[Equalizer control block]						
Control range	G_{eq}	Max, boost/cut	± 8	± 10	± 12	dB
Step resolution	E_{step}		1	2	3	dB
Internal feedback resistance	R_{feed}		17	28	39	k Ω
[Overall characteristics]						
Total harmonic distortion	THD (1)	$V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, with all controls flat overall		0.0033		%
	THD (2)	$V_{IN} = 1\text{ Vrms}$, $f = 20\text{ kHz}$, with all controls flat overall		0.012		%
Crosstalk	CT	$V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, with all controls flat overall, $R_g = 1\text{ k}\Omega$		86		dB
Output at maximum attenuation	$V_O\text{ min}$	$V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, main volume $-\infty$		-90		dB
Output noise voltage	V_N (1)	With all controls flat overall (IHF-A), $R_g = 1\text{ k}\Omega$		3.9		μV
	V_N (2)	With all controls flat overall (DIN-AUDIO), $R_g = 1\text{ k}\Omega$		5.4		μV
Current drain	I_{DD}	$V_{DD} - V_{SS} = 11\text{ V}$		25	33	mA
Input high level current	I_{IH}	CL, DI, CE, $V_{IN} = 11\text{ V}$			10	μA
Input low level current	I_{IL}	CL, DI, CE, $V_{IN} = 0\text{ V}$	-10			μA

Input Amplifier Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} - V_{SS} = 10\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input offset voltage	V_{IO}		-10		+10	mV
Input offset current	I_{IO}	$V_{SS} \leq V_{IN} \leq V_{DD}$		± 10		nA
Open-loop voltage gain	A_O			80		dB
Width of 0 dB band	f_T			2.5		MHz
Allowable load resistance	R_L		3			k Ω

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Equivalent Block Diagram and Sample Application Circuit



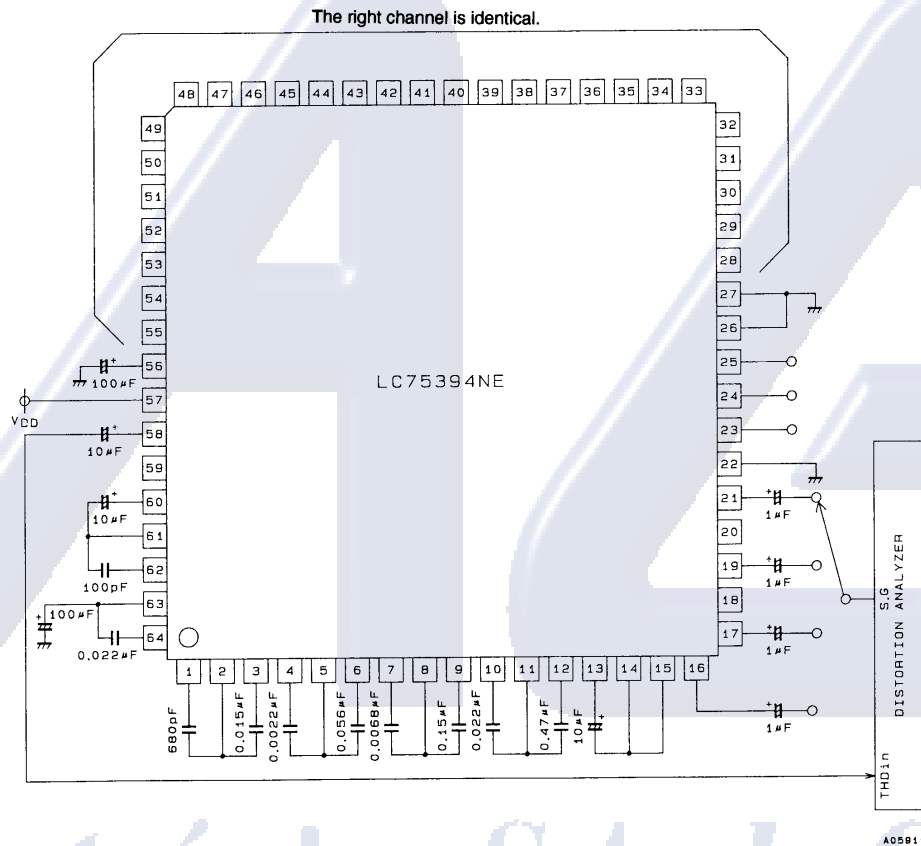
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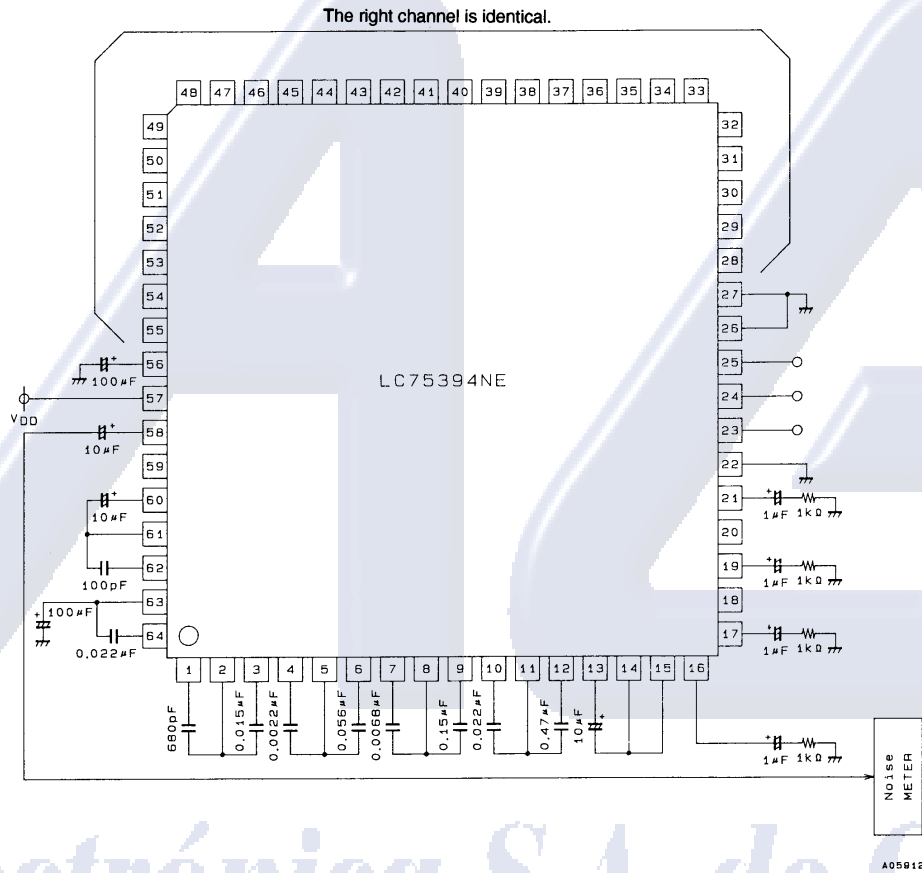
Test Circuits

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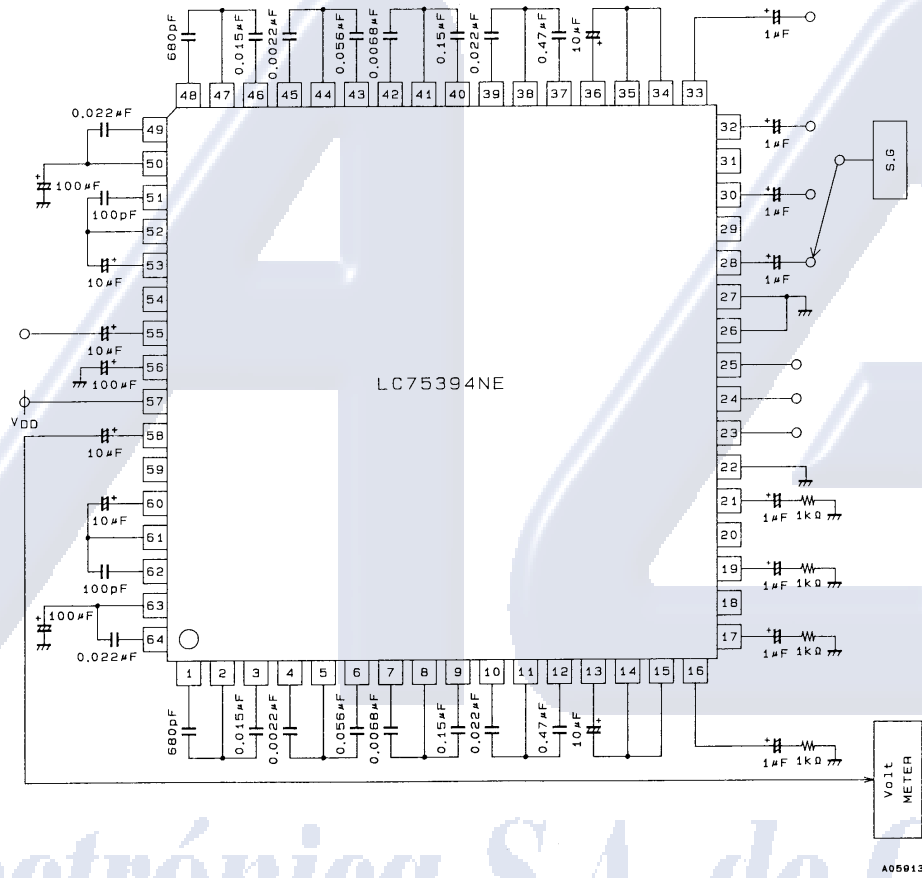
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2. Output Noise Voltage



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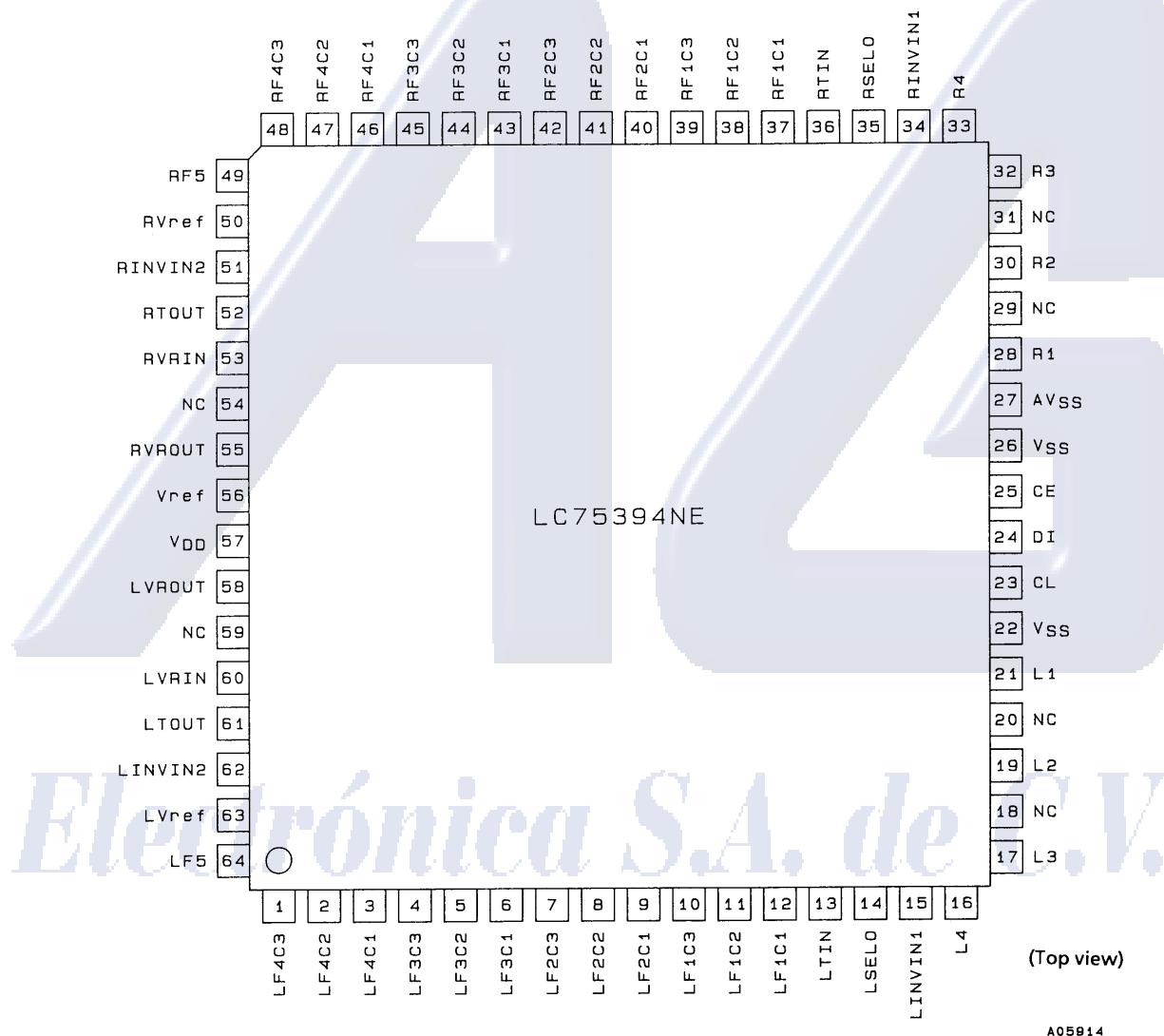
3. Crosstalk



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Pin Assignment

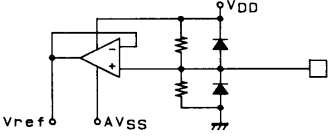
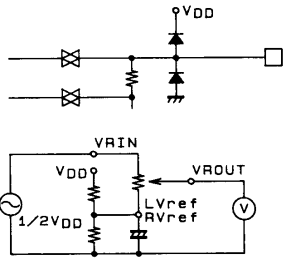
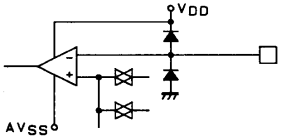
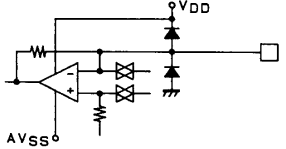
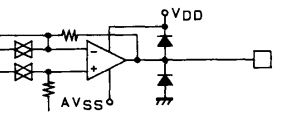
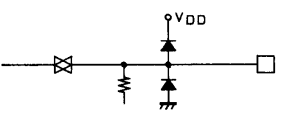
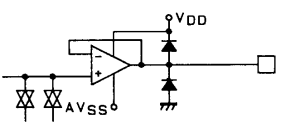
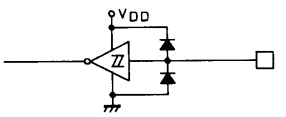


Pin Functions

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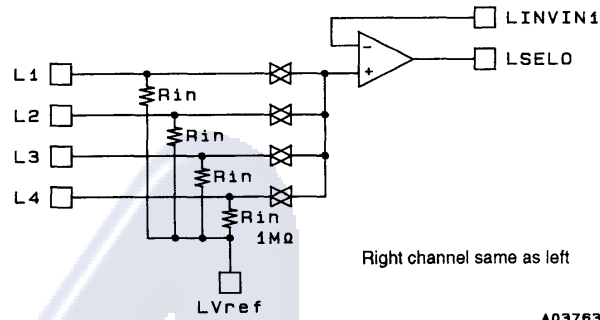
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Pin No.	Symbol	Function	Note
56	Vref	$V_{DD}/2$ voltage generator block. Connect capacitors between Vref and V_{SS} to minimize the effects of power supply ripple.	 A03755
63 50	LVref RVref	Pins common to volume control, tone control, and input selection blocks. Select the capacitors between these pins and V_{SS} carefully as they contribute residual resistance when the volume is turned down. The voltage must never exceed V_{DD} .	 A03756
15 34	LINVIN1 RINVIN1	Operational amplifier inverted input for specifying input gain.	 A03757
62 51	LINVIN2 RINVIN2	Operational amplifier inverted input for specifying graphic equalization. Connecting a capacitor across INVIN2 and TOUT permits the removal of unwanted bands and reduces the risk of oscillation.	 A03758
61 52	LTOUT RTOUT	Tone control output	 A03759
60 53	LVRIN RVRIN	Volume control input. Must be driven with low-impedance circuits.	 A03760
58 55	LVROUT RVROUT	Volume control output	 A03761
25	CE	Chip enable pin. The chip uses falling edge timing to write data to the internal latch and shift analog switches. The high level enables data transfer.	 A03762
24 23	DI CL	Serial data and clock input used for control	
18 20 29 31 54 59	NC NC NC NC NC NC	Leave unconnected	

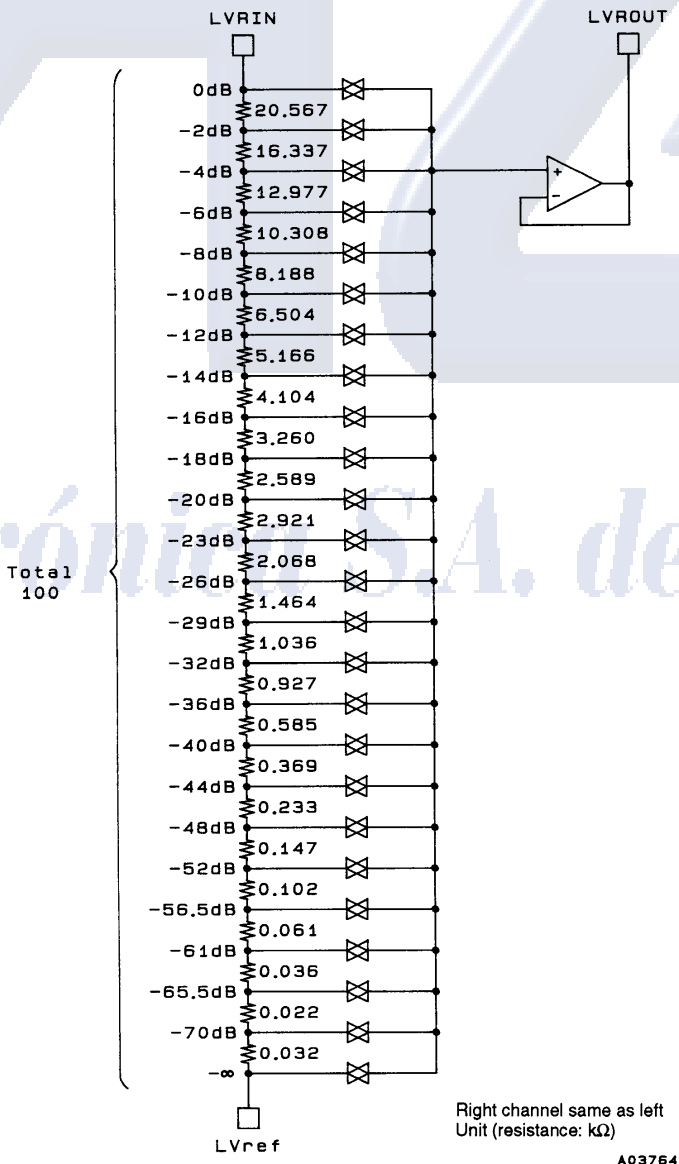
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Input Block Internal Equivalent Circuit Diagram

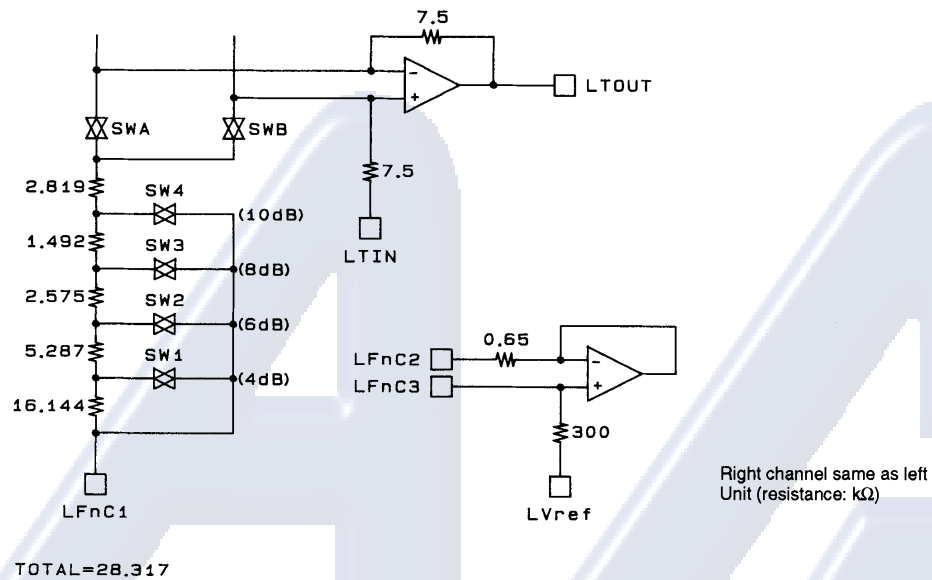


Volume Control Block Internal Equivalent Diagram



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Equalizer Control Block Internal Equivalent Circuit (Bands F1 to F4)



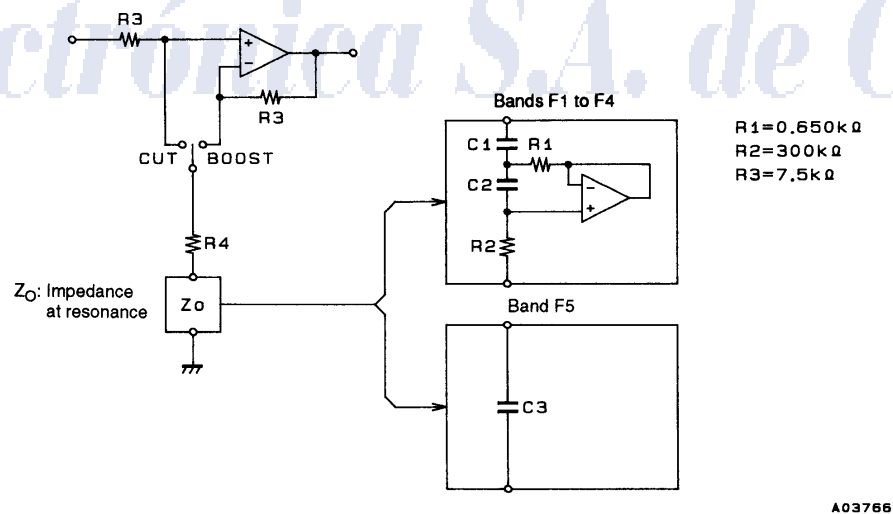
Calculating the Size of External Capacitors

The LC75394NE supports four bands with peaking characteristics and one band with shelving characteristics

1. Peaking Characteristics (bands F1 to F4)

The external capacitor functions as the structural element of a simulated inductor. The equivalent circuit and the calculations required to achieve the desired center frequency are shown below.

- Equivalent circuit for the simulated inductor



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- Calculation example

Specifications: Central frequency, $F_O = 107 \text{ Hz}$

Q factor at maximum boost, $Q_{+10 \text{ dB}} = 0.8$

— Calculate Q_O , the sharpness of the simulated inductance itself.

$$Q_O = (R1 + R4)/R1 \times Q_{+10\text{dB}} \\ \neq 4.270$$

Note: R4 is from the separately issued internal block diagram.

— Calculate C1

$$C1 = 1/2\pi F_O R1 Q_O \neq 0.536 \text{ (}\mu\text{F)}$$

— Calculate C2

$$C2 = Q_O/2\pi F_O R2 \neq 0.021 \text{ (}\mu\text{F)}$$

- Sample results

Central frequency F_O (Hz)	C1 (F)	C2 (F)
107	0.536 μ	0.021 μ
340	0.169 μ	6663 p
1070	0.054 μ	2117 p
3400	0.017 μ	666 p

- Shelving characteristics (Band F5)

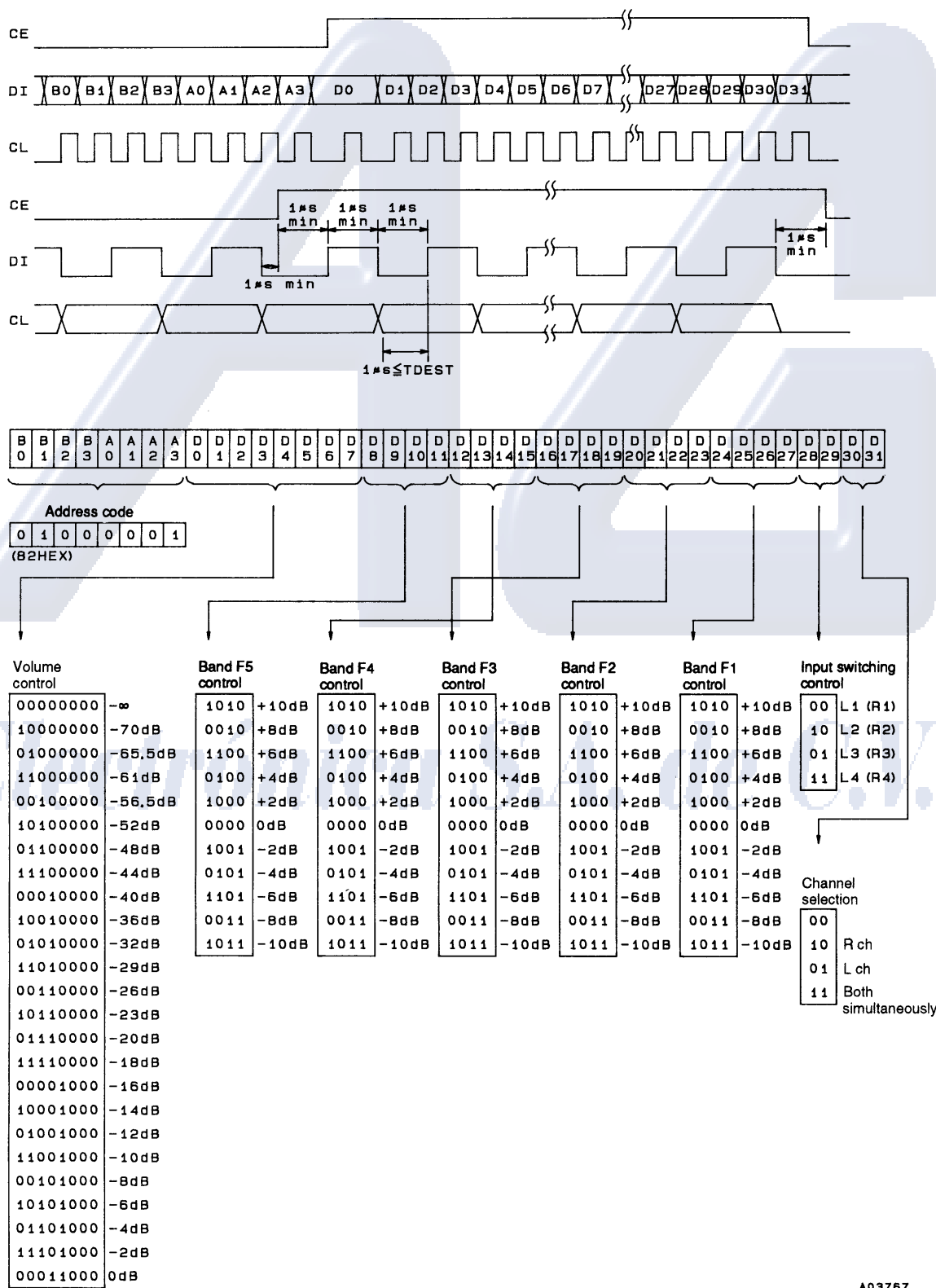
Achieving the desired control of 2-dB steps over the range between +10 dB to -10 dB requires choosing a capacitor, C3, with an impedance of 650 Ω .

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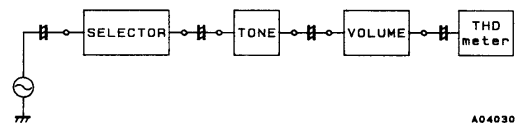
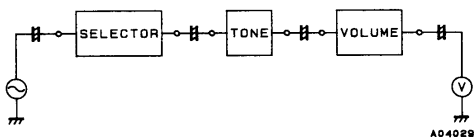
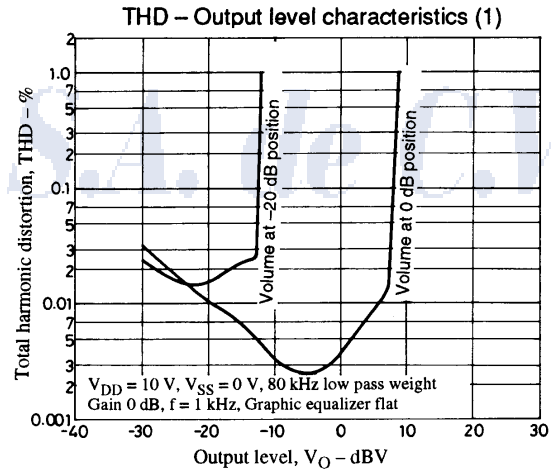
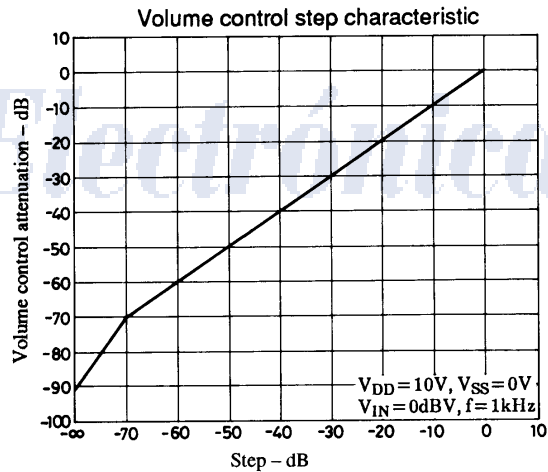
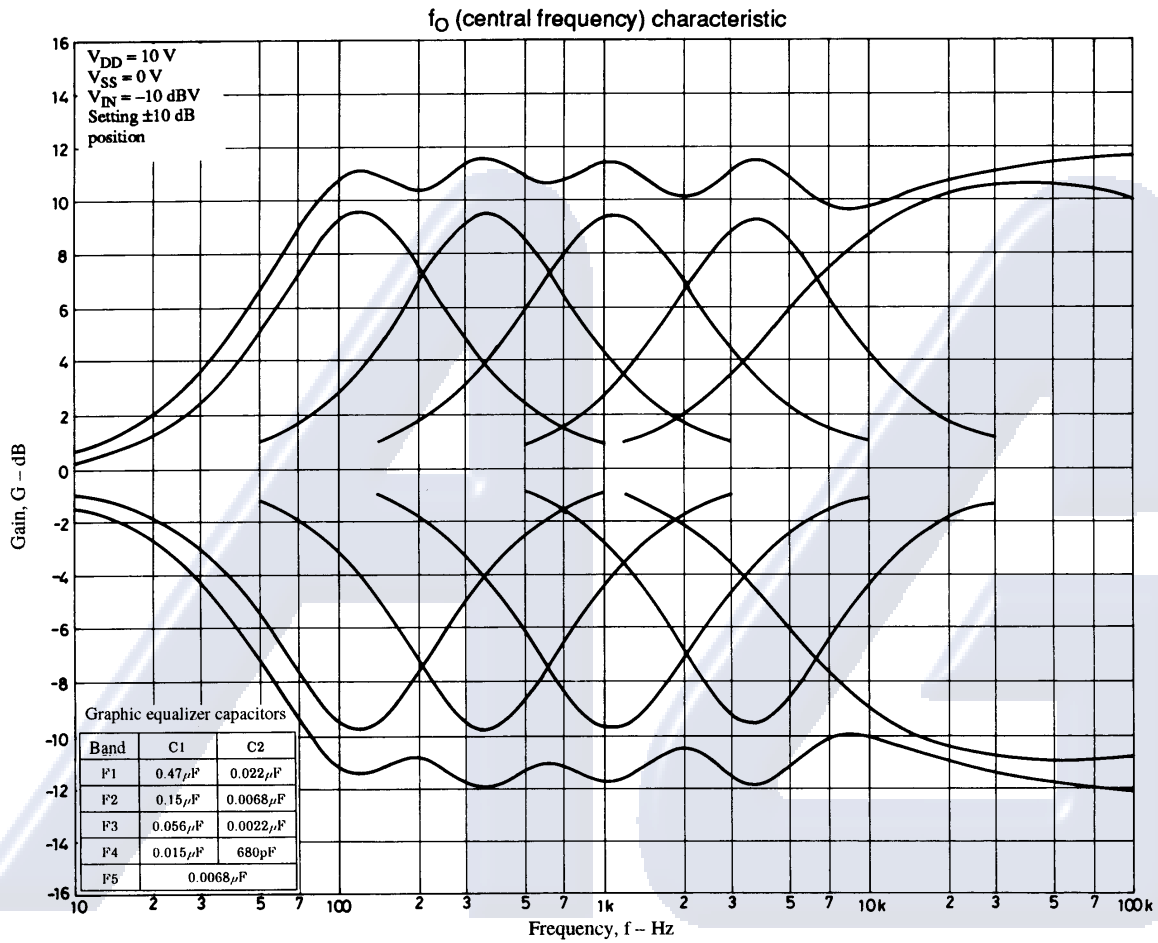
Control System Timing and Data Formats

The LC75394NE receives its control sequences via a serial interface comprised of pins CE, CL, and DI. Each sequence consists of 40 bits: an 8-bit address followed by 32 bits of data.



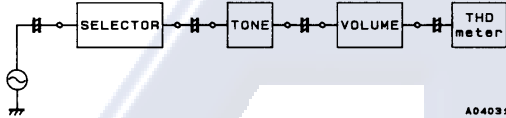
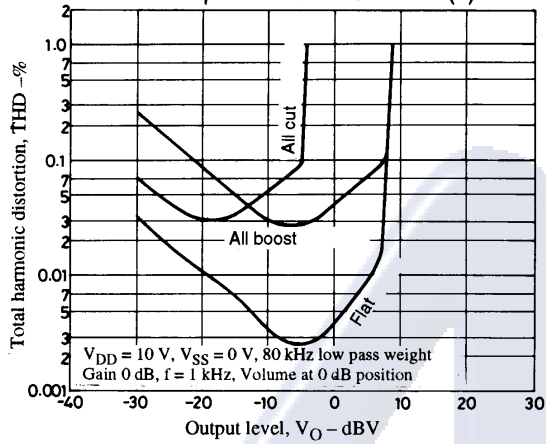
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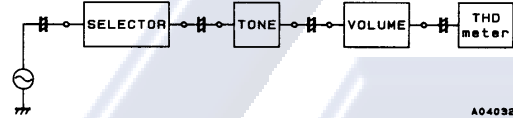
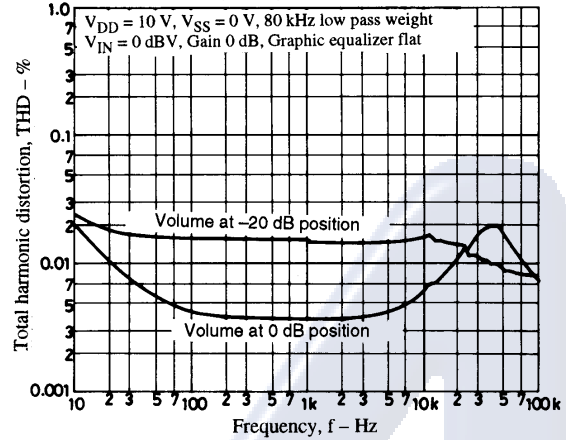
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THD – Output level characteristics (2)



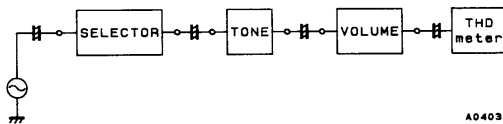
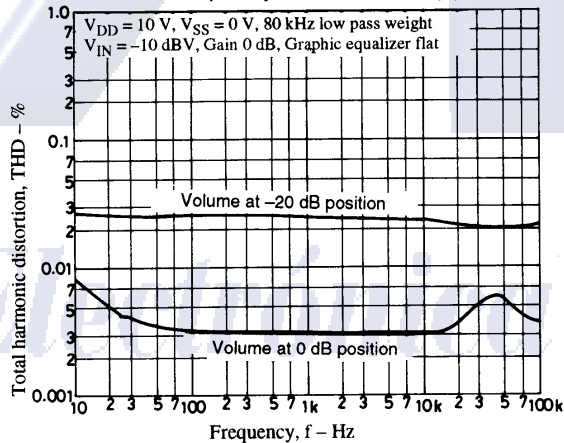
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THD – Frequency characteristics (1)



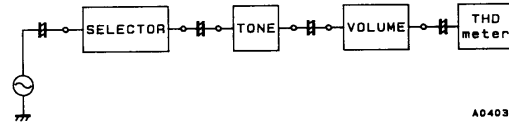
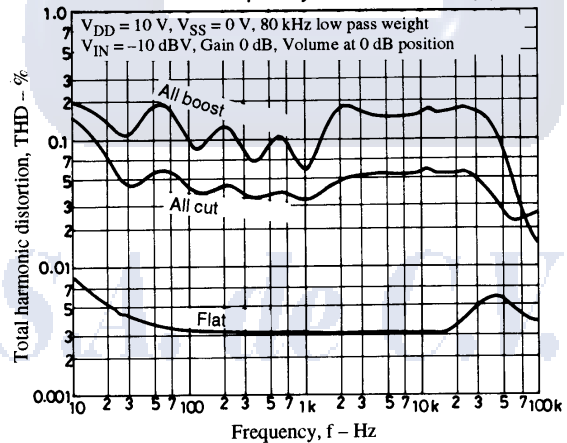
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THD – Frequency characteristics (2)



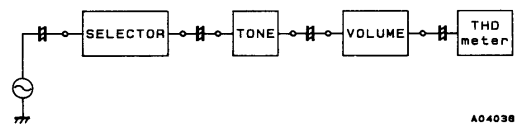
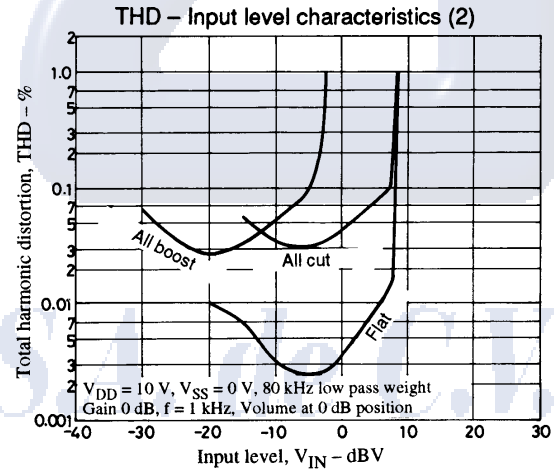
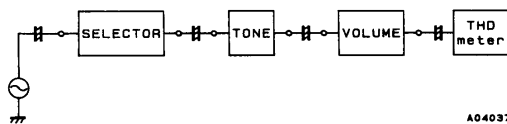
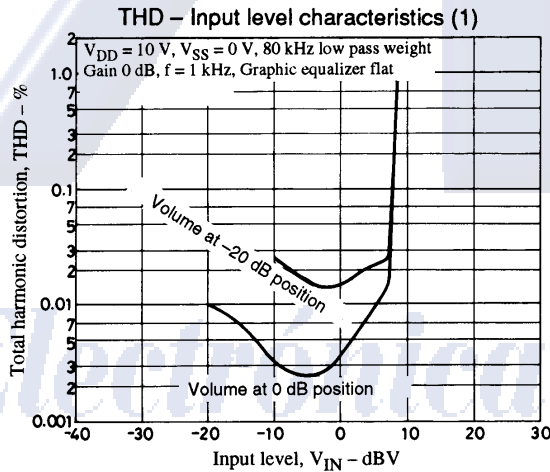
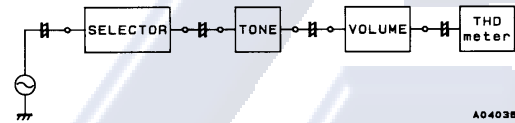
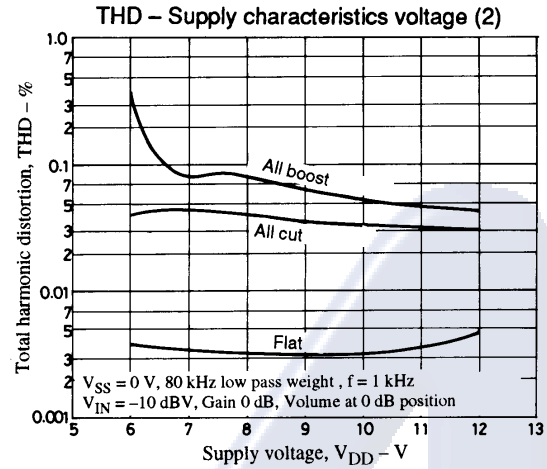
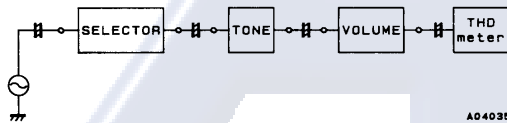
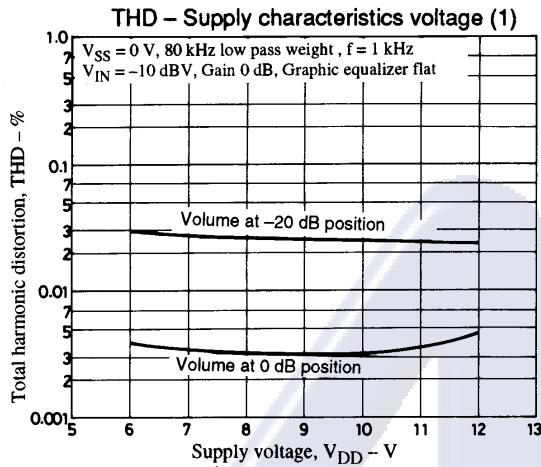
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THD – Frequency characteristics (3)



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Usage Notes

1. When the power is first applied, the internal analog switches are in indeterminate states. The chip therefore requires muting or other external measures until it has received the proper data.
2. Provide grounding patterns or shielding for the lines to the CL, DI, and CE pins so as to prevent their high-frequency data signals from interfering with the operation of nearby analog circuits.

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