ANALOG DEVICES

1nV/√Hz 420MHz GBW, 180V/μs, Low Distortion Rail-to-Rail Output Op Amps

FEATURES

- **Ultra Low Voltage Noise: 1nV/√Hz**
- **Low Distortion: HD2/HD3<–90dB$_C$ at 4V$_{P-P}$,1MHz into 1kΩ**
- **High Slew Rate: 180V/μs**
- **GBW = 420MHz**
- **–3dB Frequency (A$_V$ = +1): 330MHz**
- Input Common Mode Range Includes Negative Rail
- Output Swings Rail-to-Rail
- Supply Current: 5.5mA/Channel Typ
- Operating Supply Range: 2.8V to 11.75V
- Input Offset Voltage: 95μV Max
- Offset Drift :0.4μV/°C
- Low Power Shutdown
- Very High Open Loop Gain: 9V/μV (139dB), R_L = 1kΩ
- Operating Temp Range: –40°C to 125°C
- Single in 8-Lead SOIC, TSOT-23, 2mm × 2mm DFN. Duals in 3mm × 3mm DFN, MS8E

APPLICATIONS

- Optical Electronics: Fast AC-Coupled Transimpedance Amplifiers
- Driving High Dynamic Range A/D Converters
- Active Filters
- Video Amplifiers
- Low Voltage Low Distortion Amplification

DESCRIPTION

The LTC®6226/LTC6227 are very fast, low noise rail-to-rail output, unity gain stable single/dual op amps, with a gain-bandwidth product of 420MHz and a slew rate of 180V/μs. The low input referred voltage noise of only 1nV/√Hz and low distortion of less than –90dB$_C$ for 4V$_{P-P}$ signals at 1MHz makes them ideal for applications that require high dynamic range and deal with very fast signals, such as driving A/D converters.

The combination of low offset, low offset drift, high gain (139dB) and high CMRR (114dB) make these excellent devices for high dynamic range applications.

The LTC6226 family maintains excellent performance for supply voltages of 2.8V to 11.75V and the devices are fully specified at supplies of 3V, 5V and 10V (±5V).

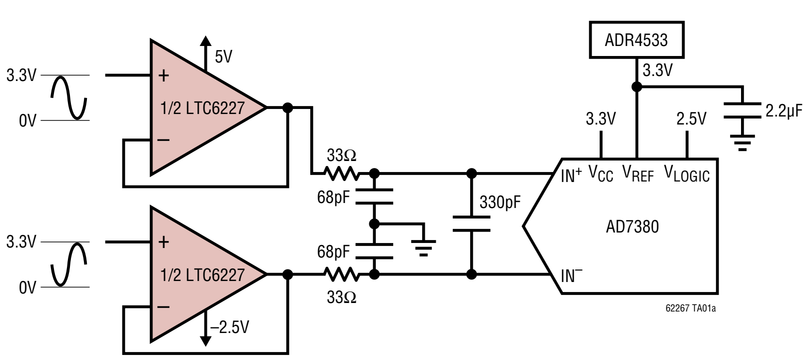
With an input range extending to the negative rail and rail-to-rail output stage, the operational amplifier can accommodate wide swinging signals, and true single supply operation.

For space constrained applications, the amplifiers come in 2mm × 2mm DFN (single) and 3mm × 3mm DFN (dual) packages. The devices are also available in 8-lead SOIC,TSOT-23 and MS8E.

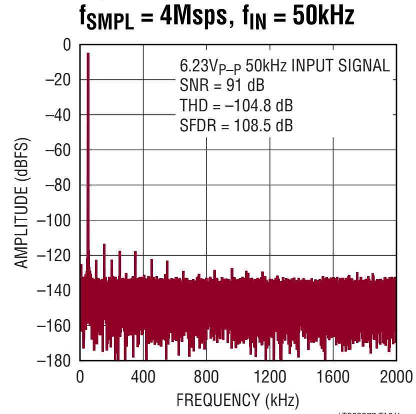
These amplifiers can be used as replacements for many high speed op amps to improve speed, noise and dynamic range.

TYPICAL APPLICATION

High Performance Transparent LTC6227 Based Driver for the 16-Bit AD7380



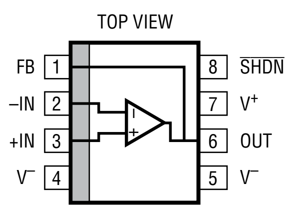
16-Bit ADC Driver Performance
Input Signal = –0.5dBFS
f$_{SMPL}$ = 4Msps, f$_{IN}$ = 50kHz



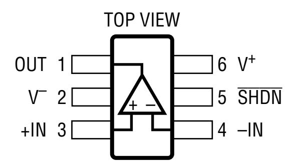
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^- to V^+) 12V
Input Voltage (–IN, +IN, $\overline{\text{SHDN}}$).... V^- – 0.3V to V^+ + 0.3V
Input Current (–IN, +IN, $\overline{\text{SHDN}}$) (Note 2).............. ±10mA
Operating Temperature Range
  LTC6226I/LTC6227I (Note 4)............... –40°C to 85°C
  LTC6226H/LTC6227H (Note 4).......... –40°C to 125°C
Specified Temperature Range
  LTC6226I/LTC6227I (Note 4)............... –40°C to 85°C
  LTC6226H/LTC6227H (Note 4).......... –40°C to 125°C
Output Current (Note 3) .... ±100mA
Output Short-Circuit Duration ....Thermally Limited
Storage Temperature Range .... –65°C to 125°C
Maximum Junction Temperature .... 150°C
MSOP Lead Temperature (Soldering 10s) .... 300°C

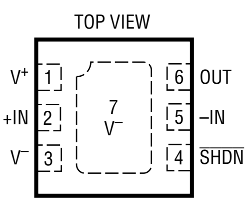
PIN CONFIGURATION



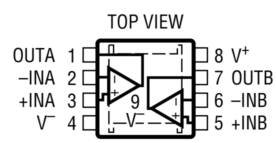
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 120°C/W (NOTE 8)



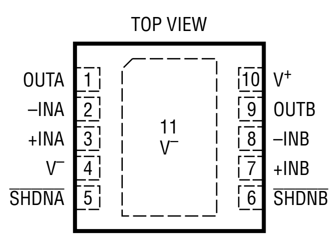
S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 192°C/W (NOTE 8)



DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (NOTE 8)
EXPOSED PAD (PIN 7) IS V^-, MUST BE SOLDERED TO PCB



MSE PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 35°C/W (NOTE 8)
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W (NOTE 8)
EXPOSED PAD (PIN 11) IS V^-, MUST BE SOLDERED TO PCB

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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6226IS6#TRMPBF	LTC6226IS6#TRPBF	LTHGY	6-Lead TSOT-23	–40°C to 85°C
LTC6226HS6#TRMPBF	LTC6226HS6#TRPBF	LTHGY	6-Lead TSOT-23	–40°C to 125°C
LTC6226IDC#TRMPBF	LTC6226IDC#TRPBF	LHGZ	6-Lead 2mm × 2mm DFN	–40°C to 85°C
LTC6226HDC#TRMPBF	LTC6226HDC#TRPBF	LHGZ	6-Lead 2mm × 2mm DFN	–40°C to 125°C
LTC6226IS8#PBF	LTC6226IS8#TRPBF	6226	8-Lead SOIC-8	–40°C to 85°C
LTC6226HS8#PBF	LTC6226HS8#TRPBF	6226	8-Lead SOIC-8	–40°C to 125°C
LTC6227IMS8E#PBF	LTC6227IMS8E#TRPBF	LTHHB	8-Lead MSOP, Exposed Pad	–40°C to 85°C
LTC6227HMS8E#PBF	LTC6227HMS8E#TRPBF	LTHHB	8-Lead MSOP, Exposed Pad	–40°C to 125°C
LTC6227IDD#PBF	LTC6227IDD#TRPBF	LHHC	10-Lead 3mm × 3mm DFN	–40°C to 85°C
LTC6227HDD#PBF	LTC6227HDD#TRPBF	LHHC	10-Lead 3mm × 3mm DFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS (V_S = ±5V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		 ●	–95 –225	20	95 225	µV µV
ΔV_{OS}	Input Offset Voltage Match (Channel to Channel, LTC6227, Note 5)		 ●	–140 –400	18	140 400	µV µV
T_{CVOS}	Input Offset Voltage Drift		●		0.4		µV/°C
I_B	Input Bias Current (Note 6)		 ●	–20 –25	–8.4		µA µA
ΔI_B	Input Bias Current Match (Channel to Channel,LTC6227, Note 5)		 ●	–2 –3	0.3	2 3	µA µA
I_{OS}	Input Offset Current		 ●	–0.35 –0.5	0.2	0.35 0.5	µA µA
ΔI_{OS}	Input OffsetCurrent Match (Channel to Channel, LTC6227, Note 5)		 ●	–0.7 –1	0.15	0.7 1	µA µA
e_n	Input Noise Voltage Spectral Density	f = 1MHz			1		nV/√Hz
	Integrated 1/f Noise	0.1Hz to 10Hz			0.77		$µV_{P-P}$
i_n	Input Noise Current Spectral Density	f = 1MHz			2.4		pA/√Hz
C_{IN}	Input Capacitance	Differential Mode Common Mode			3 1		pF pF
R_{IN}	Input Resistance	Differential Mode Common Mode			4.7 6		kΩ MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1kΩ to Half Supply V_{OUT} = ±4V	 ●	114 110	139		dB dB
		R_L = 100Ω to Half Supply V_{OUT} = ±2.5V	 ●	93 88	110		dB dB
CMRR	Common Mode Rejection Ratio	V_{CM} = $V^–$ – 0.1V to V^+ – 1.2V	 ●	100 95	114		dB dB
V_{CMR}	Input Common Mode Range (Note 10)		●	$V^–$ – 0.1		V^+ – 1.2	V
$PSRR^+$	Positive Power Supply Rejection Ratio	$V^–$ = –1V, V^+ = 1.8V to 10.75V	 ●	100 95	115		dB dB

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ELECTRICAL CHARACTERISTICS (V_S = ±5V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$PSRR^-$	Negative Power Supply Rejection Ratio	V^+ = 1.5V, V^- = –1.3V to –10.25V	 ●	103 108	127		dB dB
	Supply Voltage Range (V^+ – V^-) (Note 7)		●	2.8		11.75	V
V_{OL}	Output Swing Low (V_{OUT} – V_{EE})	No Load	 ●		19	21 26	mV mV
		I_{SINK} = 5mA	 ●		100	45 120	mV mV
		I_{SINK} = 25mA	 ●		330	427 670	mV mV
V_{OH}	Output Swing High (V_{CC} – V_{OUT})	No Load	 ●		14	20 26	mV mV
		I_{SINK} = 5mA	 ●		140	180 200	mV mV
		I_{SOURCE} = 25mA	 ●		600	1000 1370	mV mV
I_{SC}	Output Short-Circuit Current	Sourcing	 ●		–64	–42 –35	mA mA
		Sinking	 ●	45 32	60		mA mA
I_S	Supply Current per Channel		 ●		5.5	5.8 7.4	mA mA
I_{SD}	Disable Supply Current Per Channel, Amplifier Off	$V_{\overline{SHDN}}$ = V^+ – 2.75V	 ●		350	450 520	μA μA
V_{L_SHDN}	$\overline{SHDN}$ Pin Input Voltage Low, Disable Amplifier		●			V^+ – 2.75	V
V_{H_SHDN}	$\overline{SHDN}$ Pin Input Voltage High, Enable Amplifier		●	V^+ – 1.6			V
I_{L_SHDN}	$\overline{SHDN}$ Pin Input Current, Disable Amplifier	$V_{\overline{SHDN}}$ = V^+ – 2.75V	●	–10	–2.5	10	μA
I_{H_SHDN}	$\overline{SHDN}$ Pin Input Current, Enable Amplifier	$V_{\overline{SHDN}}$ = V^+ – 1.6V	●	–10	–0.3	10	μA
I_{OSD}	Output Leakage Current in Shutdown				100		nA
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1kΩ to Half Supply			330		MHz
GBW	Gain-Bandwidth Product	f = 5MHz, R_L = 1kΩ to Half Supply	 ●	350 300	420		MHz MHz
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = V^+ – 2.75V to V^+ – 1.6V			2100		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = V^+ – 1.6V to V^+ – 2.75V			800		ns
$t_{S\_0.1}$	Settling Time to 0.1%	A_V = 1, 2V Output Step, R_L = 1kΩ			58		ns
		A_V = 1, 4V Output Step, R_L = 1kΩ			61		ns
$t_{S\_0.01}$	Settling Time to 0.01%	A_V = 1, 6V Output Step, R_L = 1kΩ			150		ns

ELECTRICAL CHARACTERISTICS (V_S = ±5V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, V_{CM} = 0V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	A_V = +4, 8V Output Step (Note 9)	 ●	115 90	180		V/µS V/µS
FPBW	Full Power Bandwidth	V_{OUT} = $8V_{P-P}$, A_V = +2, THD < –40dBc			5.5		MHz
HD2/HD3	Harmonic Distortion, R_L = 1kΩ to Half Supply, A_V = +1	f_C = 100kHz, V_O = $4V_{P-P}$ f_C = 1MHz, V_O = $4V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2MHz, V_O = $4V_{P-P}$ f_C = 2MHz, V_O = $2V_{P-P}$			–128/–136 –99/–91 –104/–95 –89/–79 –91/–80		dBc dBc dBc dBc dBc
	Harmonic Distortion, R_L = 100Ω to Half Supply, A_V = +1	f_C = 100kHz, V_O = $4V_{P-P}$ f_C = 1MHz, V_O = $4V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2MHz, V_O = $4V_{P-P}$ f_C = 2MHz, V_O = $2V_{P-P}$			–111/–123 –93/–77 –96/–80 –89/–70 –90/–70		dBc dBc dBc dBc dBc
ΔG	Differential Gain	A_V = 2, R_L = 150Ω A_V = +1, R_L = 1kΩ			0.4 0.08		% %
Δθ	Differential Phase	A_V = 2, R_L = 150Ω A_V = +1, R_L = 1kΩ			0.025 0.13		Deg Deg

ELECTRICAL CHARACTERISTICS (V_S = 5V, 0V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = V_{OUT} = 2.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		 ●	–100 –235	20	100 235	µV µV
ΔV_{OS}	Input Offset Voltage Match (Channel to Channel, LTC6227, Note 5)		 ●	–140 –400	18	140 400	µV µV
T_{CVOS}	Input Offset Voltage Drift		●		0.4		µV/°C
I_B	Input Bias Current (Note 5)		 ●	–20 –25	–8.4		µA µA
ΔI_B	Input Bias Current Match (Channel to Channel, LTC6227, Note 5)		 ●	–2 –3	0.3	2 3	µA µA
I_{OS}	Input Offset Current			–0.35 –0.5	0.2	0.35 0.5	µA µA
ΔI_{OS}	Input Offset Current Match (Channel to Channel, LTC6227, Note 5)		 ●	–0.7 –1	0.15	0.7 1	µA µA
e_n	Input Noise Voltage Spectral Density	f = 1MHz			1		$nV/\sqrt{Hz}$
	Integrated 1/f Noise	0.1Hz to 10Hz			0.77		$µV_{P-P}$
i_n	Input Noise Current Spectral Density	f = 1MHz			2.4		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	Differential Mode Common Mode			3 1		pF pF
R_{IN}	Input Resistance	Differential Mode Common Mode			4.7 6		kΩ MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1kΩ to Half Supply V_{OUT} = 0.5V to 4.5V	 ●	114 110	135		dB dB
		R_L = 100Ω to Half Supply V_{OUT} = 0.9V to 4.1V	 ●	105 93	120		dB dB
CMRR	Common Mode Rejection Ratio	V_{CM} = $V^–$ – 0.1V to V^+ – 1.2V		99 95	114		dB dB

ELECTRICAL CHARACTERISTICS (V_S = 5V, 0V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = V_{OUT} = 2.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CMR}	Input Common Mode Range (Note 10)		●	V^- – 0.1		V^+ – 1.2	V
$PSRR^+$	Positive Power Supply Rejection Ratio	V^- = –1V, V^+ = 1.8V to 10.75V	 ●	100 95	115		dB dB
$PSRR^-$	Negative Power Supply Rejection Ratio	V^+ = 1.5V, V^- = –1.3V to –10.25V	 ●	103 100	127		dB dB
	Supply Voltage Range (V^+ – V^-) (Note 7)		●	2.8		11.75	V
V_{OL}	Output Swing Low (V_{OUT} – V_{EE})	No Load	 ●		16	21 23	mV mV
		I_{SINK} = 5mA	 ●		90	110 155	mV mV
		I_{SINK} = 15mA	 ●		220	270 370	mV mV
V_{OH}	Output Swing High (V_{CC} – V_{OUT})	No Load	 ●		11	15 20	mV mV
		I_{SINK} = 5mA	 ●		150	180 200	mV mV
		I_{SOURCE} = 15mA	 ●		331	500 650	mV mV
I_{SC}	Output Short-Circuit Current	Sourcing	 ●		–52	–34 –30	mA mA
		Sinking	 ●	42 30	57		mA mA
I_S	Supply Current per Channel		 ●		5.8	6.3 7.6	mA mA
I_{SD}	Disable Supply Current Per Amplifier, Amplifier Off	$V_{\overline{SHDN}}$ = V^+ – 2.65V	 ●		245	310 330	µA µA
$V_{L\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Voltage Low, Disable Amplifier		●			V^+ – 2.65	V
$V_{H\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Voltage High, Enable Amplifier		●	V^+ – 1.6			V
$I_{L\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Current, Disable Amplifier	$V_{\overline{SHDN}}$ = V^+ – 2.65V	●	–10	–2.9	10	µA
$I_{H\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Current, Enable Amplifier	$V_{\overline{SHDN}}$ = V^+ – 1.6V	●	–10	–0.3	10	µA
I_{OSD}	Output Leakage Current in Shutdown				100		nA
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1kΩ to Half Supply			490		MHz
GBW	Gain-Bandwidth Product	f = 5MHz, R_L = 1kΩ to Half Supply	 ●	350 290	430		MHz MHz
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = V^+ – 2.65V to V^+ – 1.6V			2100		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = V^+ – 1.6V to V^+ – 2.65V			800		ns
$t_{S\_0.1}$	Settling Time to 0.1%	A_V = 1, 2V Output Step, R_L = 1kΩ			59		ns

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ELECTRICAL CHARACTERISTICS (V_S = 5V, 0V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V, V_{CM} = V_{OUT} = 2.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	A_V = +4, 4V Output Step (Note 9)			140		V/µS
FPBW	Full Power Bandwidth	V_{OUT} = $4V_{P-P}$, A_V = +2, THD < –40dBc			6		MHz
HD2/HD3	Harmonic Distortion, R_L = 1kΩ to Half Supply	f_C = 100kHz, V_O = $2V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2MHz, V_O = $2V_{P-P}$			–125/–135 –104/–106 –90/–90		dBc dBc dBc
	Harmonic Distortion, R_L = 100Ω to Half Supply	f_C = 100kHz, V_O = $2V_{P-P}$ f_C = 1MHz, V_O = $2V_{P-P}$ f_C = 2MHz, V_O = $2V_{P-P}$			–112/–128 –96/–88 –88/–74		dBc dBc dBc
ΔG	Differential Gain	A_V = 2, R_L = 150Ω A_V = +1, R_L = 1kΩ			0.17 0.09		% %
Δθ	Differential Phase	A_V = 2, R_L = 150Ω A_V = +1, R_L = 1kΩ			0.3 0.04		Deg Deg

ELECTRICAL CHARACTERISTICS (V_S = 3V, 0V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		 ●	–110 –250	24	110 250	µV µV
ΔV_{OS}	Input Offset Voltage Match (Channel to Channel, LTC6227, Note 5)		 ●	–140 –400	18	140 400	µV µV
T_{CVOS}	Input Offset Voltage Drift		●		0.4		µV/°C
I_B	Input Bias Current (Note 6)	Bias Cancellation Disabled	 ●	–20 –26	–8.4		µA µA
ΔI_B	Input Bias Current Match (Channel to Channel, LTC6227, Note 5)		 ●	–2 –3	0.3	2 3	µA µA
I_{OS}	Input Offset Current		 ●	–0.35 –0.5	0.2	0.35 0.5	µA µA
ΔI_{OS}	Input Offset Current Match (Channel to Channel,LTC6227, Note 5)		 ●	–0.7 –1	0.15	0.7 1	µA µA
e_n	Input Noise Voltage Spectral Density	f = 1MHz			1		$nV/\sqrt{Hz}$
	Integrated 1/f Noise	0.1Hz to 10Hz			0.77		μV_{P-P}
i_n	Input Current Noise Spectral Density	f = 1MHz			2.4		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	Differential Mode Common Mode			3 1		pF pF
R_{IN}	Input Resistance	Differential Mode Common Mode			4.7 6		kΩ MΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1kΩ to Half Supply, (V_{OUT} = V_{CM} ±1V)	 ●	114 100	135		dB dB
		R_L = 100Ω to Half Supply, (V_{OUT} = V_{CM} ±1V)			114		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- – 0.1V to V^+ – 1.2V	 ●	98 90	114		dB dB
V_{CMR}	Input Common Mode Range (Note 10)		●	V^- – 0.1		V^+ – 1.2	V
$PSRR^+$	Positive Power Supply Rejection Ratio	V^- = –1V, V^+ = 1.8V to 10.75V	 ●	100 95	115		dB dB

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ELECTRICAL CHARACTERISTICS (V_S = 3V, 0V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$PSRR^-$	Negative Power Supply Rejection Ratio	V^+ = 1.5V, V^- = –1.3V to –10.25V	 ●	103 100	127		dB dB
	Supply Voltage Range ($V^+ – V^-$) (Note 7)		●	2.8		11.75	V
V_{OL}	Output Swing Low ($V_{OUT} – V_{EE}$)	No Load	 ●		12	14 18	mV mV
		I_{SINK} = 5mA	 ●		91	121 160	mV mV
		I_{SINK} = 10mA	 ●		161	205 275	mV mV
V_{OH}	Output Swing High ($V_{CC} – V_{OUT}$)	No Load	 ●		10	14 18	mV mV
		I_{SINK} = 5mA	 ●		150	180 230	mV mV
		I_{SOURCE} = 10mA	 ●		250	330 430	mV mV
I_{SC}	Output Short Circuit Current	Sourcing			47		mA
		Sinking			57		mA
I_S	Supply Current/Channel		 ●		5.5	6 7.25	mA mA
I_{SD}	Disable Supply Current, Amplifier Off	$V_{\overline{SHDN}}$ = V^+ – 2.65V	●		195	247 278	μA μA
$V_{L\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Voltage Low, Disable Amplifier		●			V^+ – 2.65	V
$V_{H\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Voltage High, Enable Amplifier		●	V^+ – 1.6			V
$I_{L\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Current, Disable Amplifier	$V_{\overline{SHDN}}$ = V^+ – 2.65V	●	–10	–2.9	10	μA
$I_{H\_\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Current, Enable Amplifier	$V_{\overline{SHDN}}$ = V^+ – 1.6V	●	–10	0.3	10	μA
I_{OSD}	Output Leakage Current in Shutdown				100		nA
BW	–3dB Closed Loop Bandwidth	A_V = 1, R_L = 1kΩ to Half Supply			450		MHz
GBW	Gain-Bandwidth Product	f = 5MHz, R_L = 1kΩ to Half Supply	 ●	340 280	415		MHz MHz
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = V^+ – 2.65V to V^+ – 1.6V			2100		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = V^+ – 1.6V to V^+ – 2.65V			800		ns
$t_{S\_0.1}$	Settling Time to 0.1%	A_V = 1, V_{CM} = 1V, 1V Output Step, R_L = 1kΩ to V_{CM}			84		ns
SR	Slew Rate (Note 9)	A_V = +4, 2V Output Step			100		V/μS
FPBW	Full Power Bandwidth	V_{OUT} = $2V_{P-P}$, A_V = –1, THD < –40dBc			8		MHz

ELECTRICAL CHARACTERISTICS (V_S = 3V, 0V)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3V, 0V, V_{CM} = 1.5V, $V_{\overline{SHDN}}$ = floating unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
HD2/HD3	Harmonic Distortion, R_L = 1kΩ to V_{CM}, V_{OUT} = $1V_{P-P}$, V_{CM} = 1V	f_C = 100kHz f_C = 1MHz f_C = 2MHz			–122/–137 –108/–111 –95/–95		dBc dBc dBc
	Harmonic Distortion, R_L = 100Ω to V_{CM}, V_{OUT} = $1V_{P-P}$, V_{CM} = 1V	f_C = 100kHz f_C = 1MHz f_C = 2MHz			–113/–130 –100/–94 –90/–79		dBc dBc dBc

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If any of the input or shutdown pins goes 300mV beyond either supply or the differential input voltage exceeds 0.7V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output current is high.

Note 4: The LTC6226I/LTC6227I are guaranteed functional and specified over the temperature range of –40°C to 85°C. The LTC6226H/LTC6227H are guaranteed and specified functional over the temperature range of –40°C to 125°C.

Note 5: Matching parameters are the difference between amplifiers A and B on the LTC6227.

Note 6: The input bias current is the average of the average of the currents through the positive and negative input pins.

Note 7: Supply Voltage Range is guaranteed by Power Supply Rejection Ratio test.

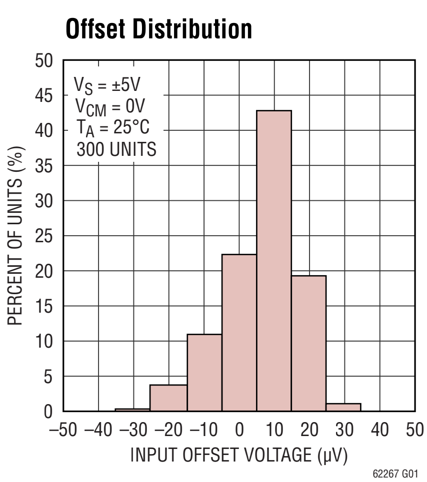
Note 8: Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are with short traces connected to the leads.

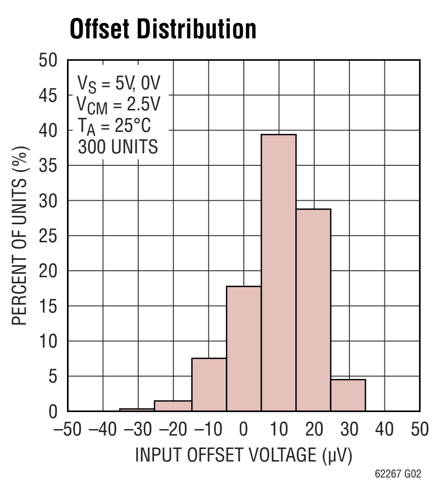
Note 9: Middle 2/3 of the output waveform is observed for Slew Rate. R_L = 1k to half supply.

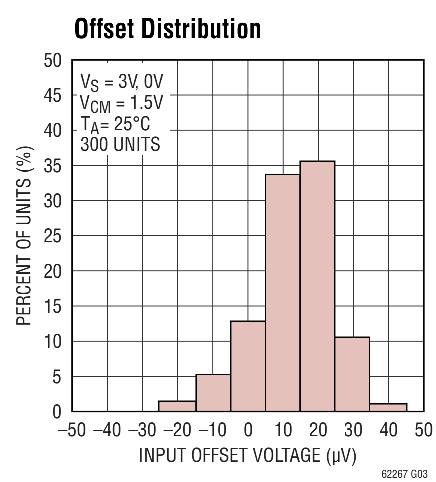
Note 10: Input Common Mode Range is guaranteed by Common Mode Rejection Ratio Test.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5V, V_{CM} = 0V, R_L = 1kΩ to Half Supply, T_A = 25°C, unless otherwise noted.

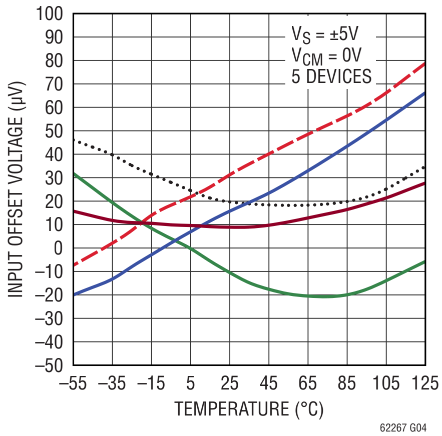




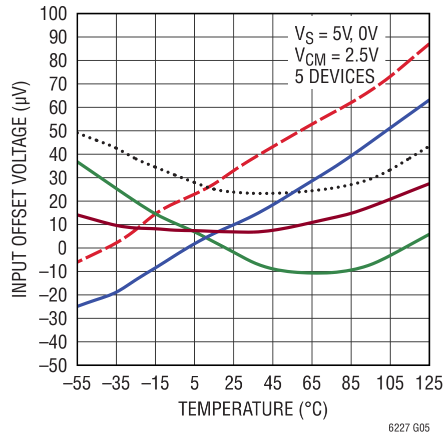


TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm 5V$, $V_{CM} = 0V$, $R_L = 1k\Omega$ to Half Supply, $T_A = 25°C$, unless otherwise noted.

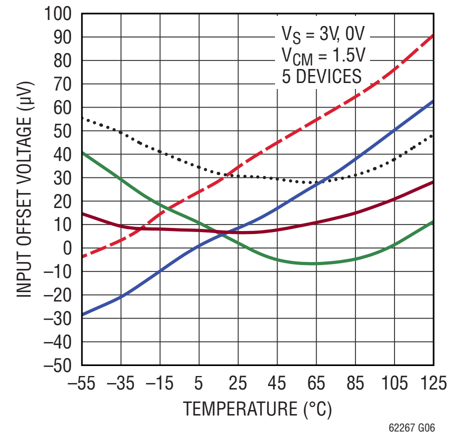
V_{OS} vs Temperature, 10V Supply



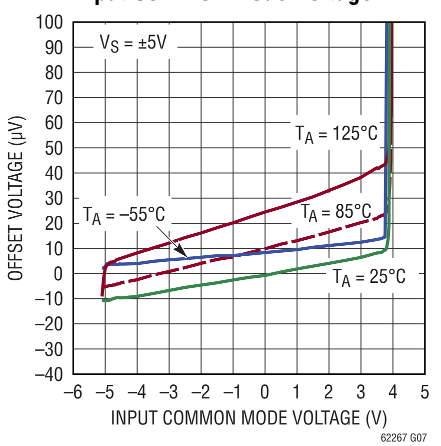
V_{OS} vs Temperature, 5V Supply



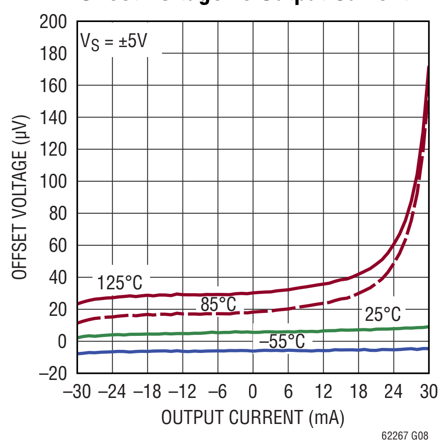
V_{OS} vs Temperature, 3V Supply



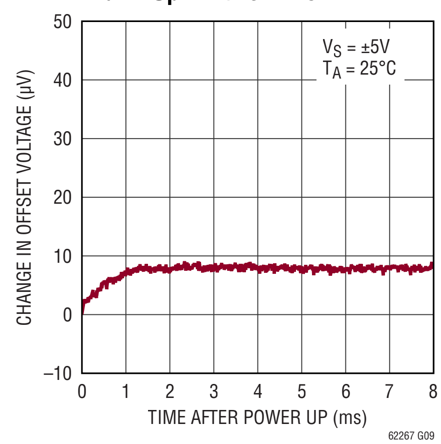
Offset Voltage vs Input Common Mode Voltage



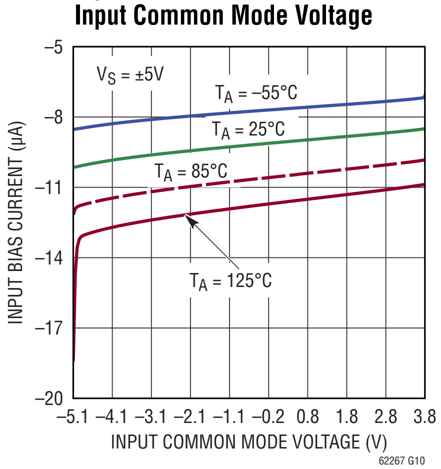
Offset Voltage vs Output Current



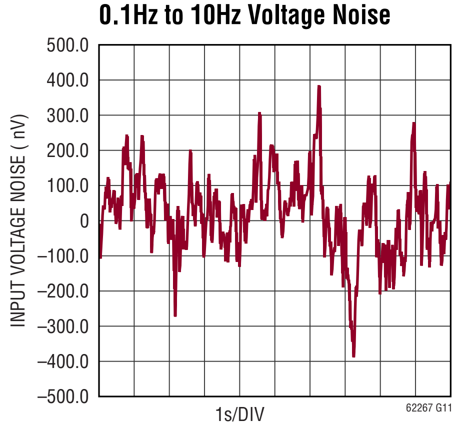
Warm Up Drift vs Time



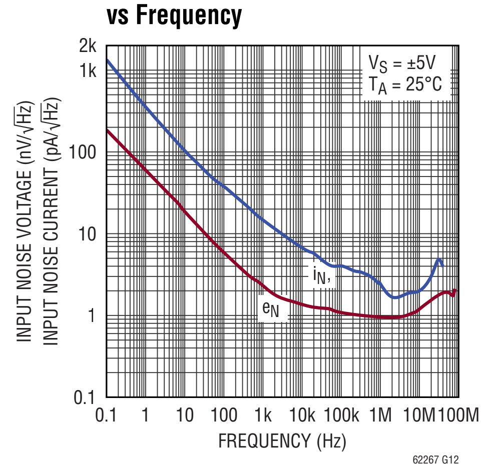
Input Bias Current vs Input Common Mode Voltage



0.1Hz to 10Hz Voltage Noise



Input Noise Voltage and Noise Current Spectral Densities vs Frequency

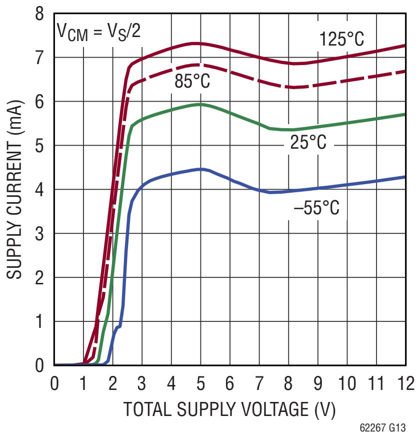


Rev 0

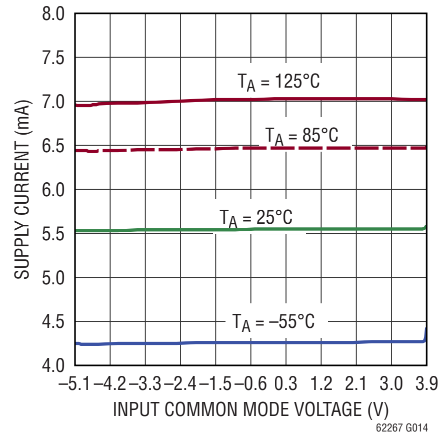
TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5V, V_{CM} = 0V, R_L = 1kΩ to Half Supply, T_A = 25°C, unless otherwise noted.

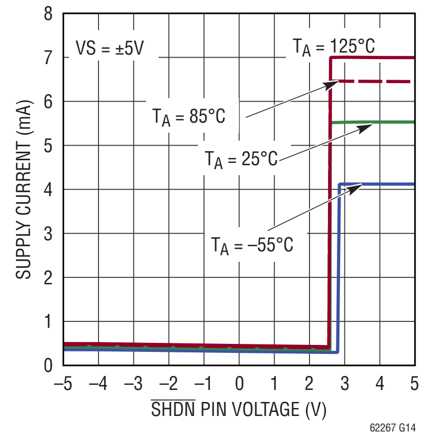
Supply Current vs Supply Voltage



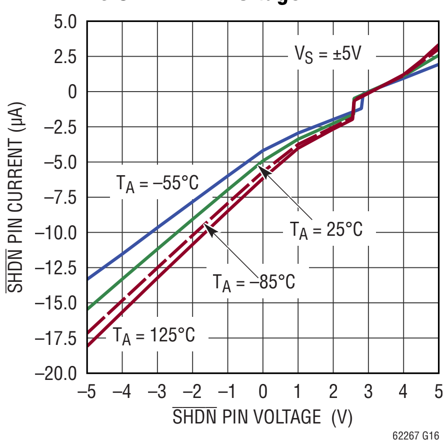
Supply Current vs Input Common Mode Voltage



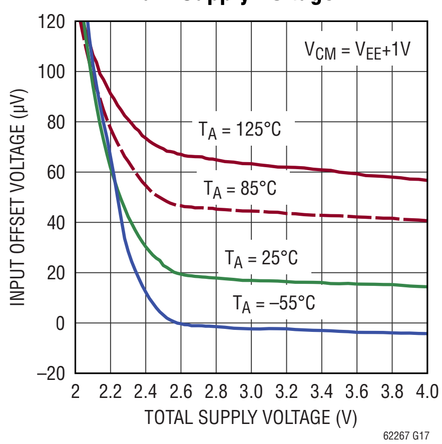
Supply Current vs SHDN Pin Voltage



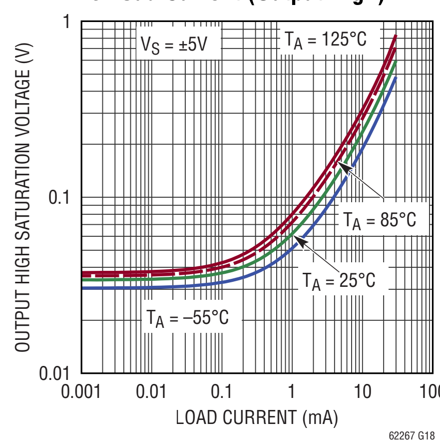
SHDN Pin Current vs SHDN Pin Voltage



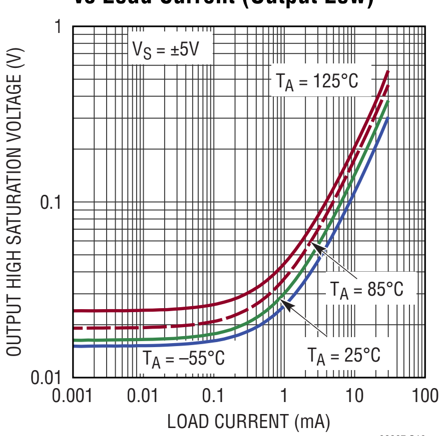
Minimum Supply Voltage



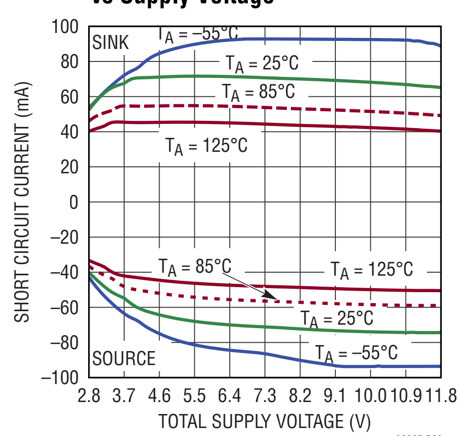
Output Saturation Voltage vs Load Current (Output High)



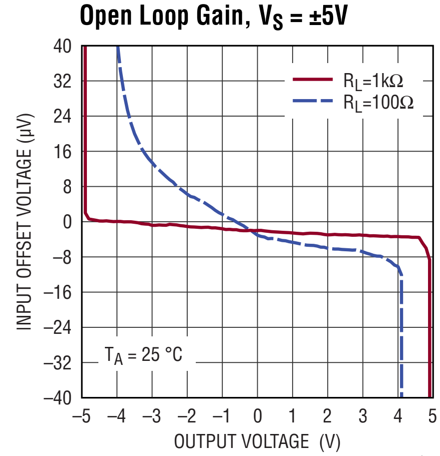
Output Saturation Voltage vs Load Current (Output Low)



Output Short Circuit Current vs Supply Voltage

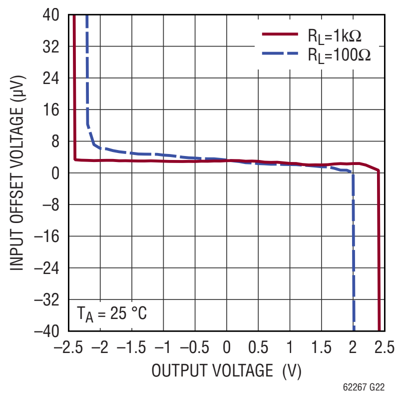


Open Loop Gain, V_S = ±5V

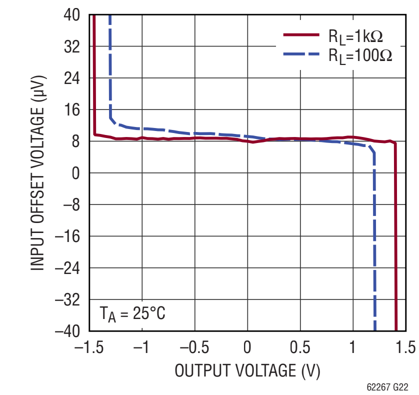


TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm5V$, $V_{CM} = 0V$, $R_L = 1k\Omega$ to Half Supply, $T_A = 25°C$, unless otherwise noted.

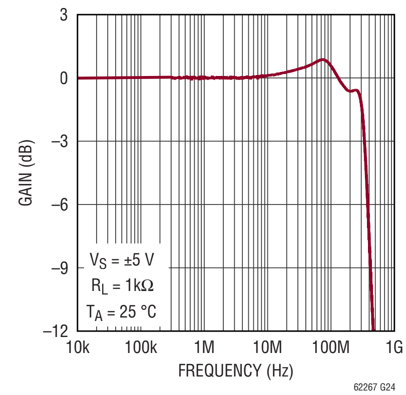
Open Loop Gain, $V_S = \pm2.5V$



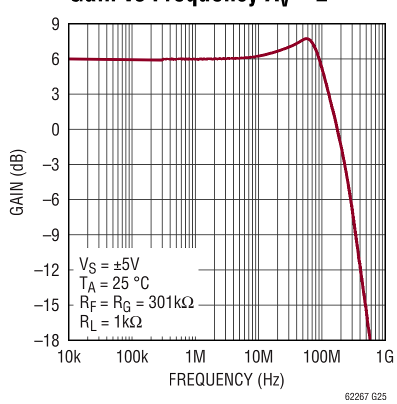
Open Loop Gain, $V_S = \pm1.5V$



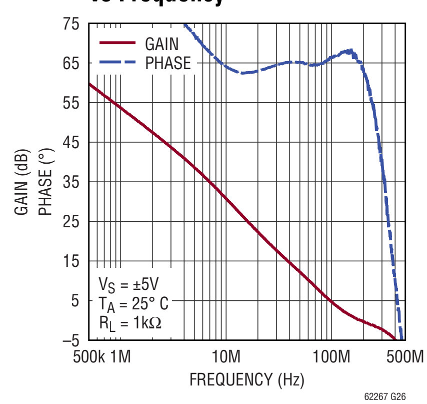
Gain vs Frequency $A_V = 1$



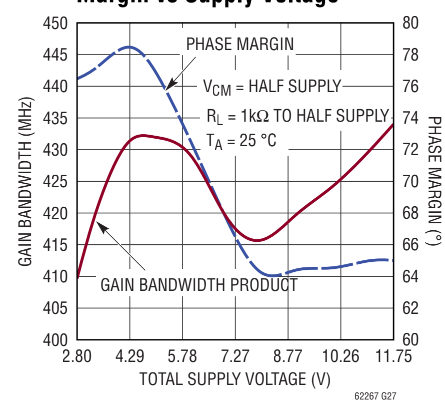
Gain vs Frequency $A_V = 2$



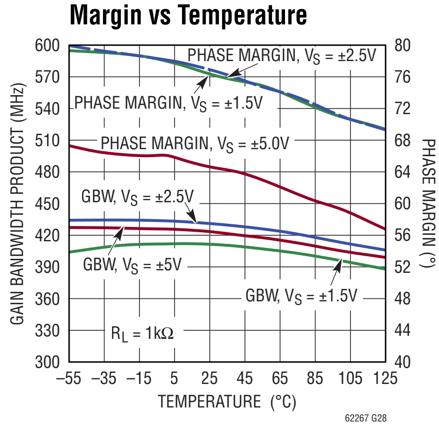
Open Loop Gain and Phase vs Frequency



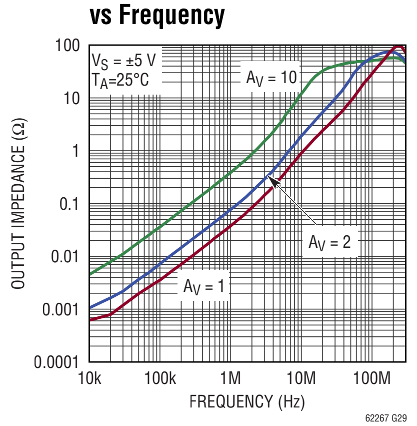
Gain Bandwidth and Phase Margin vs Supply Voltage



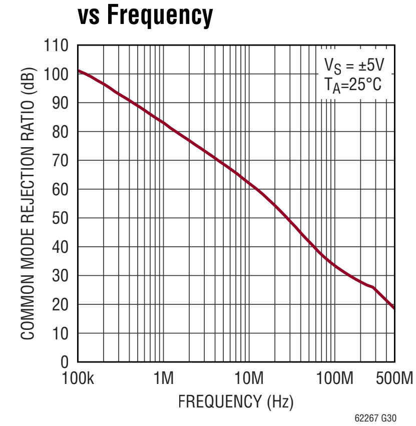
Gain Bandwidth and Phase Margin vs Temperature



Output Impedance vs Frequency



Common Mode Rejection Ratio vs Frequency



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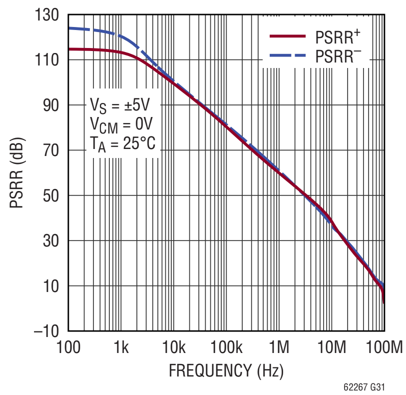
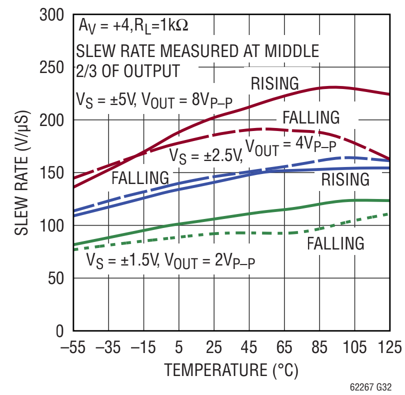
TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm5V$, $V_{CM} = 0V$, $R_L = 1k\Omega$ to Half Supply, $T_A = 25°C$, unless otherwise noted.

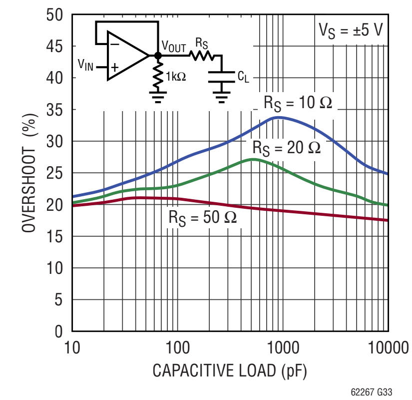
Power Supply Rejection Ratio vs Frequency



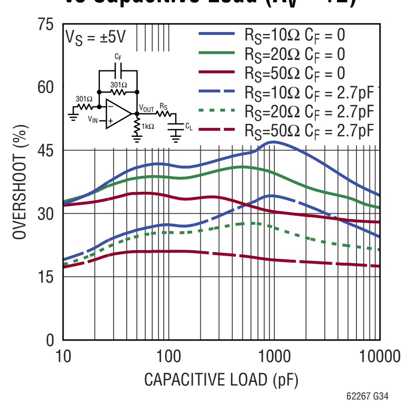
Slew Rate vs Temperature



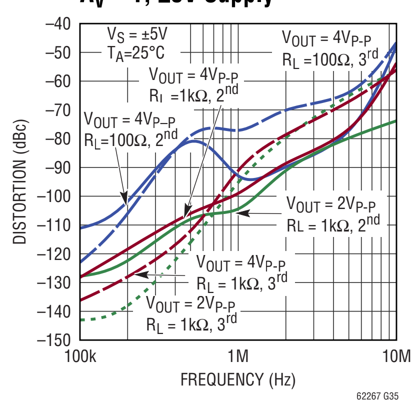
Overshoot vs Capacitive Load ($A_V = +1$)



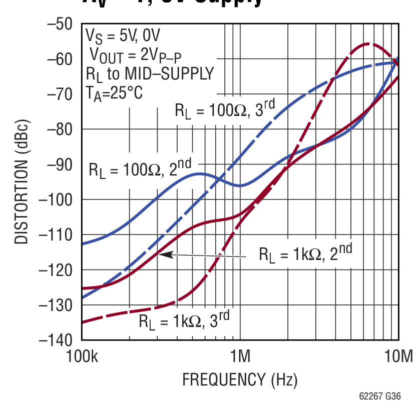
Overshoot vs Capacitive Load ($A_V = +2$)



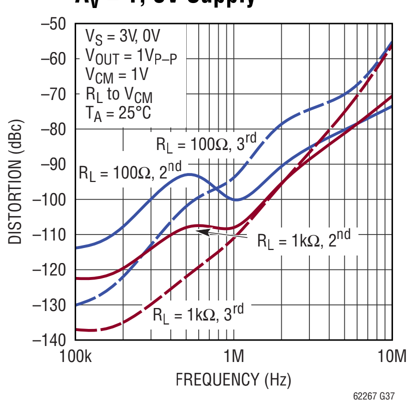
Distortion vs Frequency, $A_V = 1$, ±5V Supply



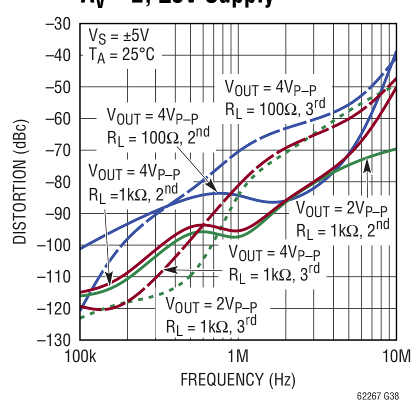
Distortion vs Frequency, $A_V = 1$, 5V Supply



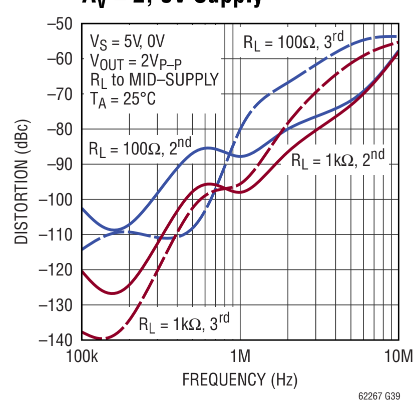
Distortion vs Frequency, $A_V = 1$, 3V Supply



Distortion vs Frequency, $A_V = 2$, ±5V Supply



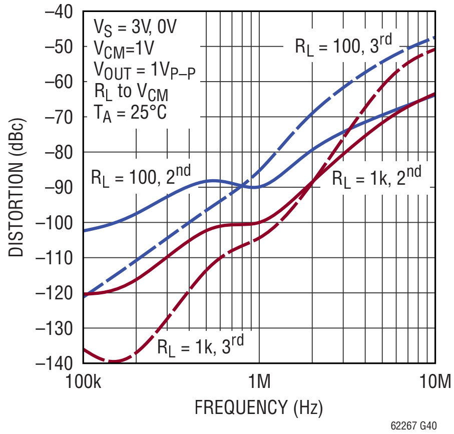
Distortion vs Frequency, $A_V = 2$, 5V Supply



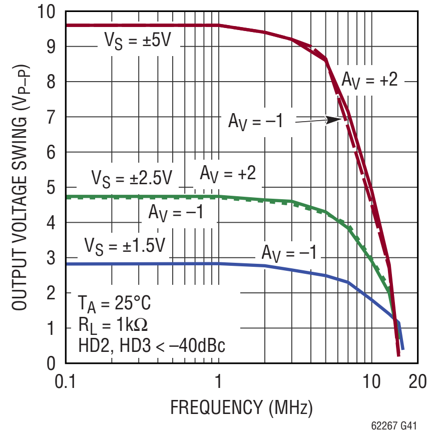
TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm5V$, $V_{CM} = 0V$, $R_L = 1k\Omega$ to Half Supply, $T_A = 25°C$, unless otherwise noted.

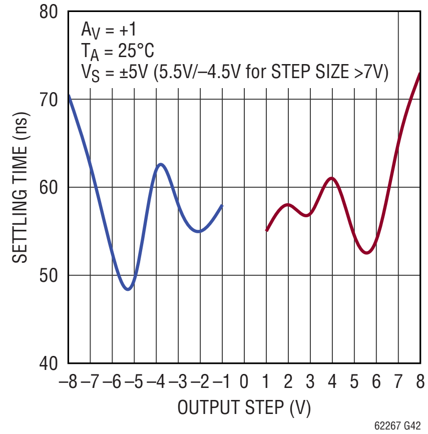
Distortion vs Frequency, $A_V = 2$, 3V Supply



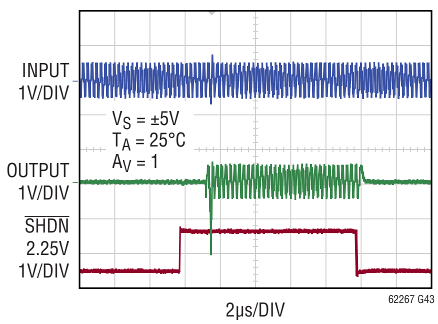
Maxium Undistorted Output Signal vs Frequency



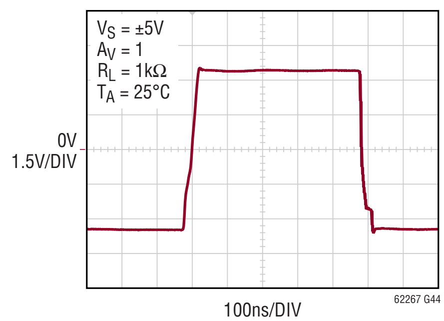
0.1% Settling Time vs Output Step



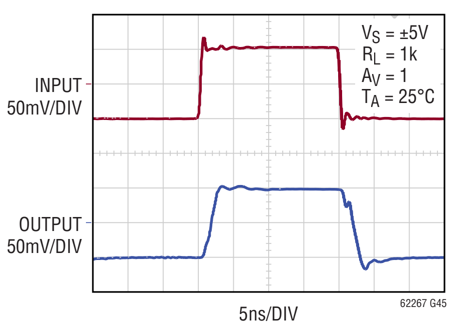
$\overline{\text{SHDN}}$ Pin Response Time



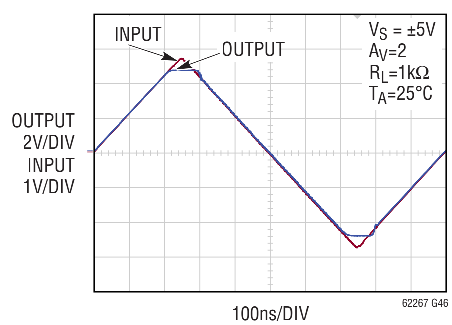
Large Signal Response



Small Signal Response



Output Overdriven Recovery



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PIN FUNCTIONS

FB (SOIC-8 Only): Feedback Pin. Internally connected to OUT.

+IN: Non-Inverting Input of Amplifier. Valid input range is from V^- to V^+ – 1.2V

–IN: Inverting Input of Amplifier. Valid input range is from V^- to V^+ – 1.2V

OUT: Output of the Amplifier. Swings rail to rail and can typically source/sink 60mA of current.

$\overline{\text{SHDN}}$: Shutdown Pin (Active Low). Referenced to V^+. When taken 2.75V below V^+, the amplifier shuts down and enters low power mode, with the outputs in a high impedance state. When left floating, the amplifier is on.

V^+: Positive Supply to Amplifier. Valid range is from 2.8V to 11.75V when V^- is 0V.

V^-: Negative Supply to Amplifier. Typically 0V. This can be made a negative voltage as long as $2.8V \le (V^+ – V^-) \le 11.75V$

APPLICATIONS INFORMATION

Circuit Description

The LTC6226/LTC6227 have an input signal range that extends from the negative power supply to 1.2V below the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage consists of PNP transistors Q1 and Q2. Bootstrap transistor Q13 improves DC accuracy by reducing the offset contribution of the base currents of Q11 and Q12 since it has twice their collector current thus Q11/Q12 current matching becomes independent of transistor β. The bootstrap arrangement also enhances gain by improving output impedance. A pair of complementary common emitter stages, Q15 and Q14, enables the output to swing to either rail. The $\overline{\text{SHDN}}$ Interface block translates the $\overline{\text{SHDN}}$ signal into pwr_dn for powering down the device (by deactivating current sources I1 - I4) and putting the output in a high impedance state (by shorting the bases of Q15/Q14 to the supplies via M2 and M1).

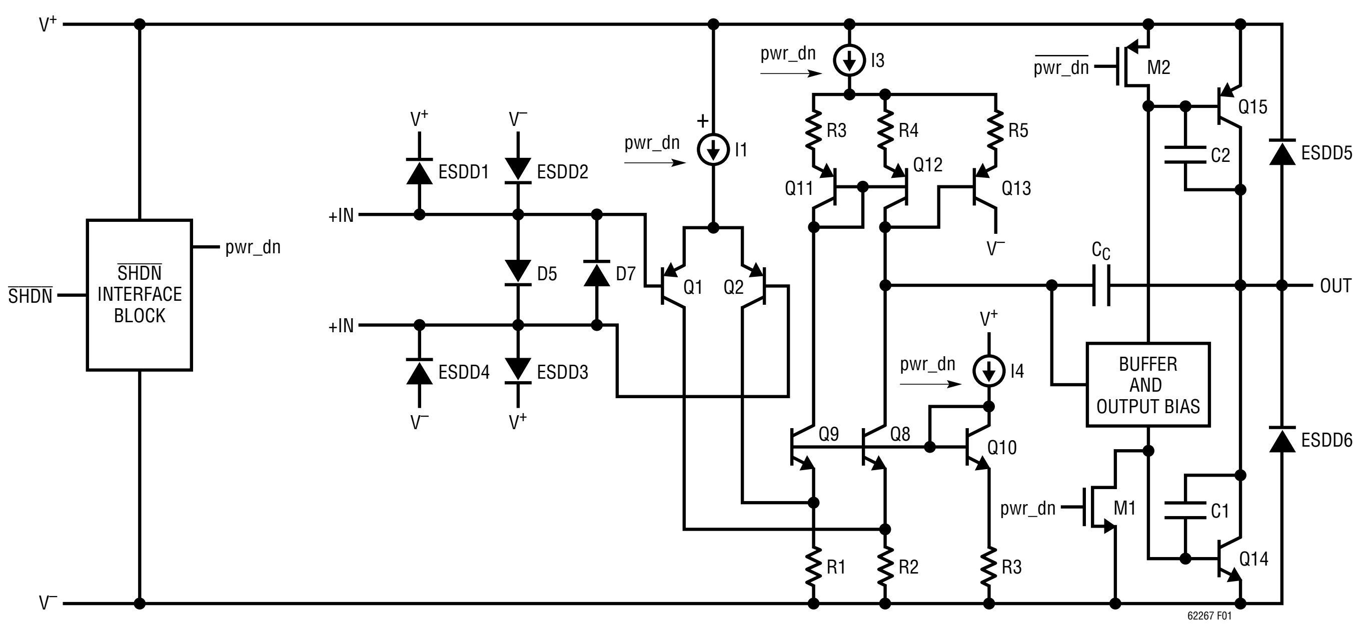


Figure 1. LTC6226/LTC6227 Simplified Schematic Diagram

APPLICATIONS INFORMATION

Output

The LTC6226 family has excellent output drive capability. The amplifiers can typically deliver more than 50mA of output drive current at a total supply of 10V, and can typically swing to within 600mV of the rail for load currents as high as 25mA. As the supply voltage to the amplifier decreases, the output current capability also decreases. Attention must be paid to keep the junction temperature of the IC below 150°C (refer to power dissipation section) when the output is in continuous short-circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, extremely high currents will flow through those diodes which can result in damage to the device. Forcing the output to even 1V beyond either supply could result in several hundred milliamps of current through either diode. Thus forcing the output beyond the supplies should be avoided.

Input Protection

The LTC6226/LTC6227 has a pair of back to back diodes (D5 and D7) to prevent the emitter base breakdown of the input transistors and limit the differential input to ±700mV. Unlike many other high performance amplifiers, the bases of the input pair transistors Q1 and Q2 are not connected to the pins using internal resistors to limit input current, since that would cause the noise to increase. For instance, a 100Ω resistor in series with each input would generate 1.8nV/$\sqrt{Hz}$ of noise, and the total amplifier noise voltage would rise from 1nV/$\sqrt{Hz}$ to 2.06nV/$\sqrt{Hz}$. Once the input differential voltage exceeds ±0.7V, current conducted though the protection diodes should be limited to ±10mA. This implies 25Ω of protection resistance per quarter volt (250mV) of overdrive beyond ±0.7V. In addition, the input and shutdown pins have reverse biased diodes connected to the supplies. The current in these diodes must be limited to less than 10mA. The amplifiers should not be used as comparators or in other open loop applications.

ESD

The LTC6226 family has reverse biased ESD protection diodes on all inputs as shown in Figure 1. There is an additional clamp between the positive and negative supplies that further protects the device during ESD strikes.

Hot plugging of the device into a powered socket must be avoided since this can trigger the clamp resulting in larger currents flowing between the supply pins.

Capacitive Loads

The LTC6226/LTC6227 are optimized for high bandwidth applications, and have not been designed to directly drive capacitive loads. Hence any trace capacitance at the output should be made as small as possible. Increased capacitance at the output creates an additional pole in the open loop frequency response, worsening the phase margin. When driving capacitive loads, a resistor of 10Ω to 100Ω should be connected between the amplifier output and the capacitive load to avoid ringing or oscillation. The feedback should be taken directly from the amplifier output. Higher voltage gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin. The graphs titled Overshoot vs Capacitive Load demonstrate the transient response of the amplifier when driving capacitive loads with various series resistors.

APPLICATIONS INFORMATION

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example if the amplifier is set up in a gain of +2 configuration with gain and feedback resistors of 1k, a parasitic capacitance of 7pF (device + PC board) at the amplifier's inverting input will cause the part to oscillate, due to a pole formed at 45MHz. An additional capacitor of 7pF across the feedback resistor as shown in Figure 2 will eliminate any ringing or oscillation. In general, if the resistive feedback network results in a pole whose frequency lies within the closed loop bandwidth of the amplifier, a capacitor can be added in parallel with the feedback resistor to introduce a zero whose frequency is close to the frequency of the pole, improving stability. For high speed designs, minimizing parasitic inductance is important. The use of capacitors where the electrodes are terminated on the long side instead of the short side (for example the use of 0306 instead of 0603 components) can help in this regard.

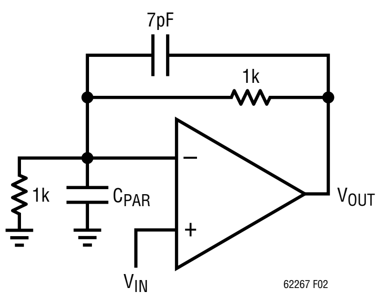


Figure 2. 7pF Feedback Cancels Parasitic Pole

Shutdown

The LTC6226 and LTC6227DD have $\overline{\text{SHDN}}$ pins that can shut down the amplifier to 350µA typical supply current. The $\overline{\text{SHDN}}$ pin needs to be taken 2.75V below the positive supply to shut down. When left floating, the $\overline{\text{SHDN}}$ pin is internally pulled up to 1.2V below the positive supply and the amplifier remains on. During shutdown, the output transistors Q15 and Q14 in Figure 1 are in a high impedance state.

Power Dissipation

Care must be taken to ensure that the junction temperature of the die does not exceed 150°C.

The junction temperature, T_J, is calculated from the ambient temperature, T_A, power dissipation, P_D, and thermal resistance, θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA}).$$

The power dissipation in the IC is a function of the supply voltage, output voltage and load resistance. For symmetric supply voltages with output load connected to ground, the worst-case power dissipation $P_{D(MAX)}$ occurs when the supply current is maximum and the output voltage at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is approximately (since I_S actually changes with output load current) given by:

$$P_{D(MAX)} = (2 \bullet V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_L$$

Example: For an LTC6227 in a 8-lead MS package operating on ±5V supplies and driving a 250Ω load to ground, the worst-case power dissipation is approximately given by $P_{D(MAX)}/\text{Amp} = (10 \bullet 7.4\text{mA}) + (5/2)^2/250 = 99\text{mW}$. If both channels are loaded identically, the total power dissipation is 198mW.

At the Absolute Maximum ambient operating temperature, the junction temperature under these conditions will be:

$$T_J = T_A + (P_D \bullet \theta_{JA}) = 125 + 0.198 \bullet 35 = 132°\text{C}$$

which is less than the absolute maximum junction temperature for the LTC6227.

Refer to the Pin Configuration section for thermal resistances of various packages

Board Layout and Bypass Capacitors

High speed and RF board layout techniques should be applied due to the very high speeds of the signals involved. For the LTC6226 SOIC-8 package option, the feedback should be taken from the FB pin rather than from the output pin, to reduce signal trace length.

Stray capacitances at the –IN and +IN pins should be made as low as possible to reduce stability degradation.

APPLICATIONS INFORMATION

For single supply applications, it is recommended that high quality 0.1µF||1000pF ceramic bypass capacitors be placed directly between each V^+ pin and its closest V^- pin with short connections. The V^- pins (including the Exposed Pad) should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that additional high quality 0.1µF||1000pF ceramic capacitors be used to bypass V^+ pins to ground and V^- pins to ground, again with minimal routing.

Noise Considerations

The ultralow input referred voltage noise of of $1nV/\sqrt{Hz}$ is equivalent to that of an 60Ω resistor. As with all BJT input amplifiers, lowering input referred noise is achieved by increasing the collector current of the input differential pair, which increases the input referred current noise.

Figure 3 shows the LTC6226 in a typical gain configuration.

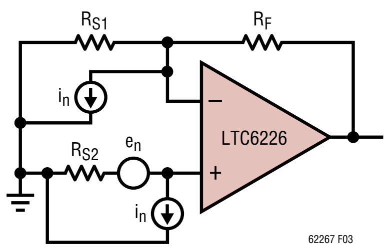


Figure 3.

As can be seen, the input referred noise spectral density of the gain stage (e_T) can be calculated by the following equations:

$$e_T^2 = e_n^2 + i_n^2 R_{EQ}^2 + 4kTR_{EQ}$$

Where

$R_{EQ} = R_{S2} + R_{S1}||R_F$, k is the Boltzmann constant and T is the temperature (in Kelvin).

Op amp input referred noise dominates the input referred noise of the gain stage when

$$R_{EQ} << e_n^2/4kT$$

Resistor noise dominated the input referred noise of the gain stage when

$$R_{EQ} >> e_n^2/4kT \text{ and } R_{EQ} << 4kT/i_n^2$$

Op amp input referred current noise dominates the input referred noise when

$$R_{EQ} >> 4kT/i_n^2$$

With an input referred voltage noise spectral density of 1nV/Hz and an input referred current noise of 2.4pA/Hz, it is easy to see that the gain stage's input referred noise is dominated by op amp voltage noise when $R_{EQ} << 60\Omega$ and by resistor noise when

$$60\Omega << R_{EQ} << 2.9k\Omega.$$

Above an R_{EQ} of 2.9kΩ, input referred current noise dominates.

Distortion/Noise Trade-Off

As evident from the previous section, gain stage noise can be reduced by reducing R_{EQ}. However, reducing R_{EQ} has its disadvantages. In addition to increasing power dissipation in the presence of large output signals, the use of smaller resistors for a given gain results in increased distortion, because the internal nonlinearities of the op amp worsen with increasing load current. In addition, smaller resistors decrease op amp gain and hence can affect bandwidth. Hence when designing a system using the LTC6226/LTC6227, it is recommended that the resistor values be limited only by the system noise requirements with the caveat that the effect of the impedances' parasitic capacitances shouldn't affect the gain below the intended bandwidth. For example, for a feedback resistor of 5kΩ, a parasitic capacitor of 400fF will impact gain at frequencies above 79MHz.

TYPICAL APPLICATIONS

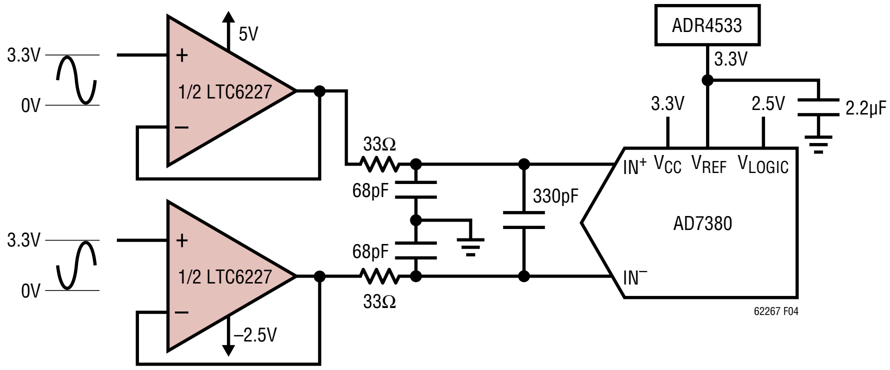


Figure 4. Transparent Driver for 16-Bit ADC

16-Bit High Performance Transparent ADC Driver

The ultralow noise and distortion performance of the LTC6226/LTC6227 makes it an excellent candidate for driving high sample rate high resolution ADCs. Figure 4 shows the LTC6227 driven by a differential input, driving an AD7380, a 4Msps, 16-bit ADC. Figure 5 shows the FFT obtained with a –0.5 dBFS, 50kHz input signal. Spurious free dynamic range is an excellent 108.5dB with an SNR of 91dB. Increasing the input frequency to 100kHz results in excellent performance as well, with a THD of –100dBc, SNR of 89dB and SFDR of 104.9dB.

16-Bit ADC Driver Performance
Input Signal = –0.5dBFS
f_{SMPL} = 4Msps, f_{IN} = 50kHz

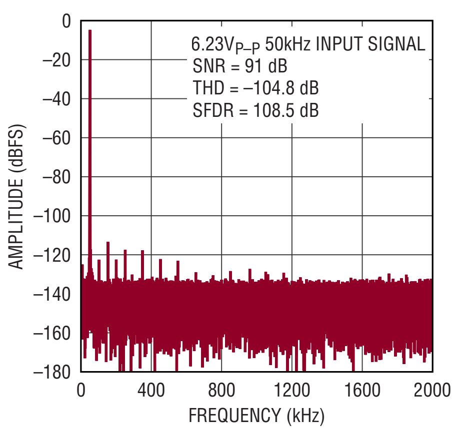


Figure 5. Measured Performance of LTC6227 Based Driver Driving the AD7380

High Performance Single Ended to Differential 16-Bit ADC Driver

In many applications, the signal to be digitized is single ended, whereas the A/D Converter needs differential inputs to maximize performance. The LTC6227 can be used to implement a Single-Ended to differential ADC driver as shown in Figure 6. One channel is configured in unity gain and drives another channel configured in an inverting gain stage of 1, both outputs drive the LTC2323-16 through an RC filter. Figure 7 shows the FFT obtained with a –1dBFS 156.25kHz input signal, with a demanding 5Msps sample rate. The obtained SNR of 81 dB is equivalent to that of the ADC by itself, thus there is no degradation due to the driver. The SFDR obtained is 84dB.

TYPICAL APPLICATIONS

High Speed Low Voltage Low Noise Instrumentation Amplifier with High CMRR

Figure 8 shows a three op amp instrumentation amplifier with a gain of 10V/V which can operate on a wide range of supply voltages. The resistors are implemented using instances of the LT5401, a matched resistor array chip. The resistor matching of U3 is crucial in achieving high common mode rejection. The front end gain stage resistors were also implemented using instances of the LT5401, but can be implemented using other means as well, since they are not crucial for common mode rejection. Implementing them using the LT5401 minimizes gain variation across temperature. The amplifiers were implemented using instances of the LTC6227MS8, and supply voltages of ±1.5V were used. Figure 9 shows the measured frequency response, and Figure 10 shows the measured CMRR of the instrumentation amplifier, with the single ended output observed. Figure 11 shows the transient response for a 150mV$_{P-P}$ input square wave.The low offset and 1/f noise allow for wide band operation down to DC. The broadband input referred noise of 4.6nV/$\sqrt{Hz}$ is dominated by the resistors.

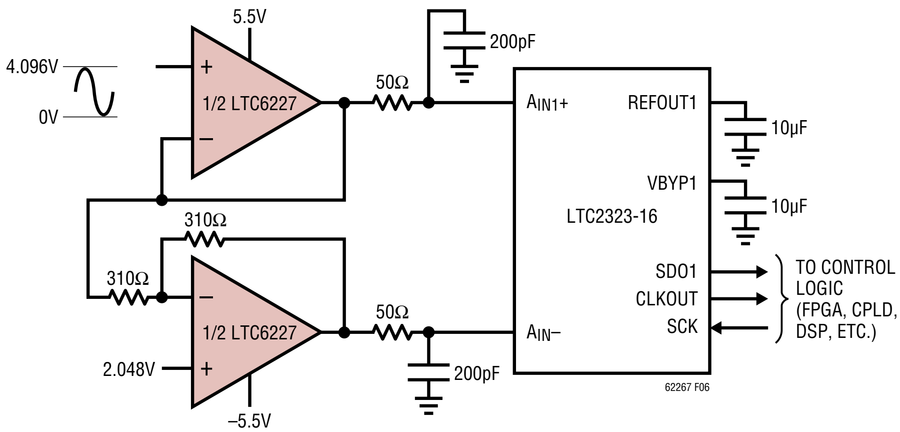


Figure 6. Single-Ended to Differential Driver for 16-Bit ADC

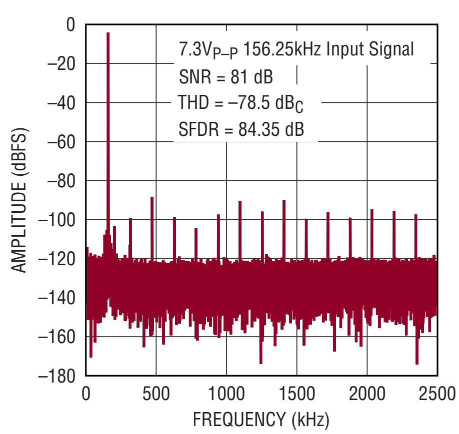


Figure 7. Measured Performance of the LTC6227 Based Single-Ended to Differential Converter Driving the LTC2323-16 ADC

TYPICAL APPLICATIONS

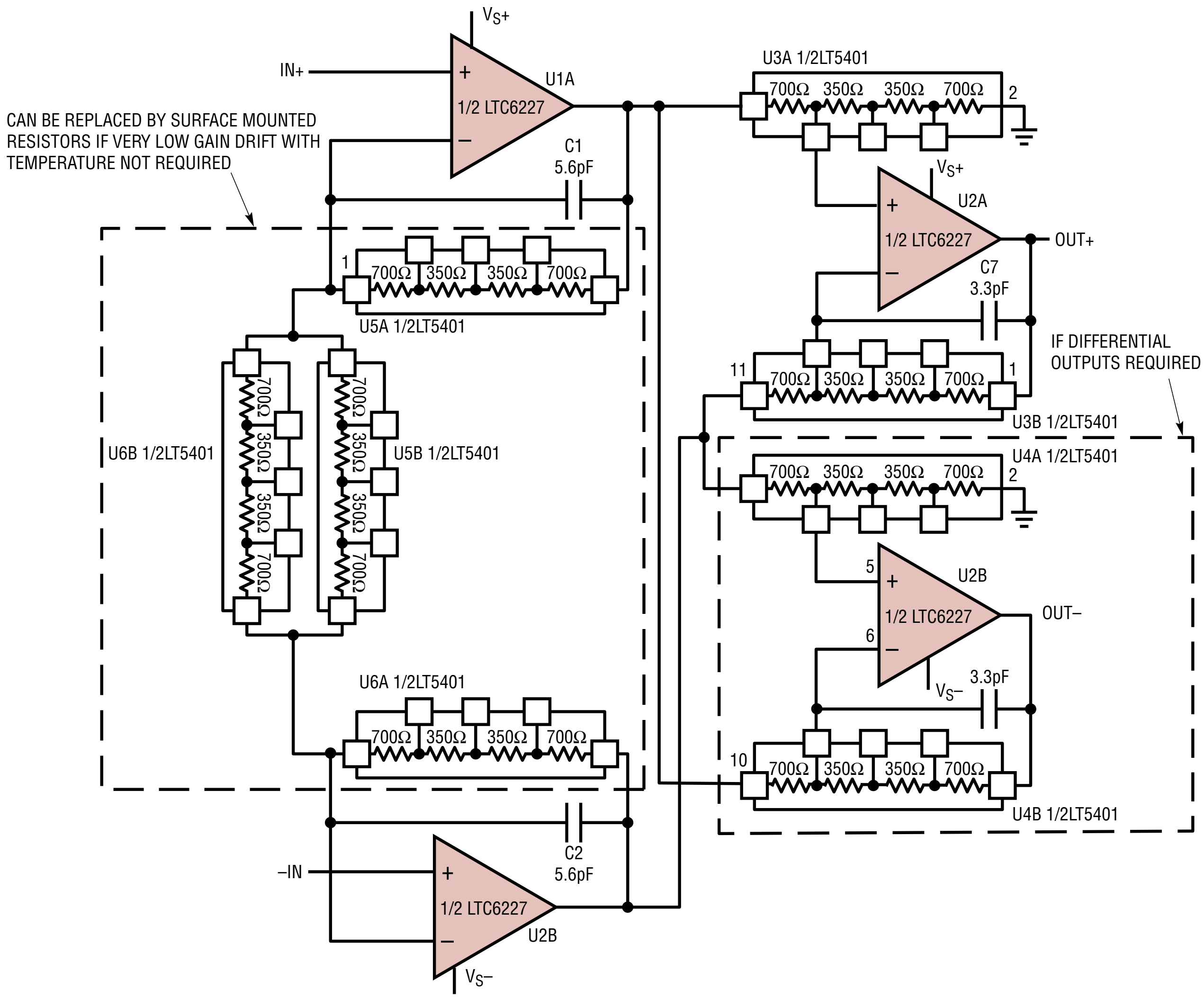


Figure 8. High Speed High CMRR Instrumentation Amplifier

TYPICAL APPLICATIONS

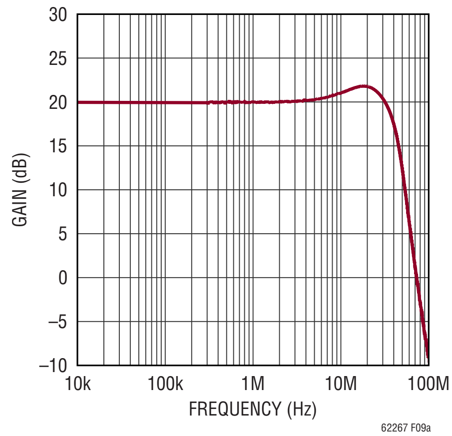


Figure 9. LTC6227-LT5401 Based Instrumentation Amplifier Frequency Response

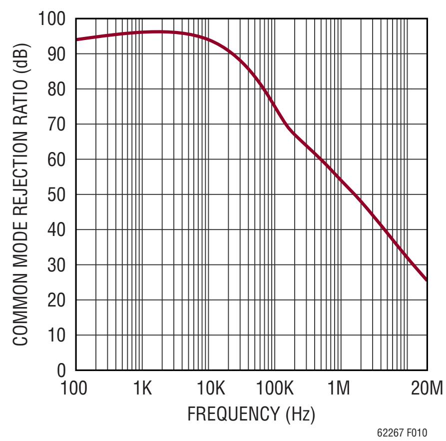


Figure 10. LTC6227-LT5401 Based Instrumentation Amplifier CMRR

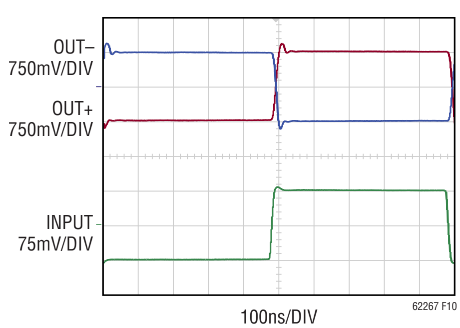
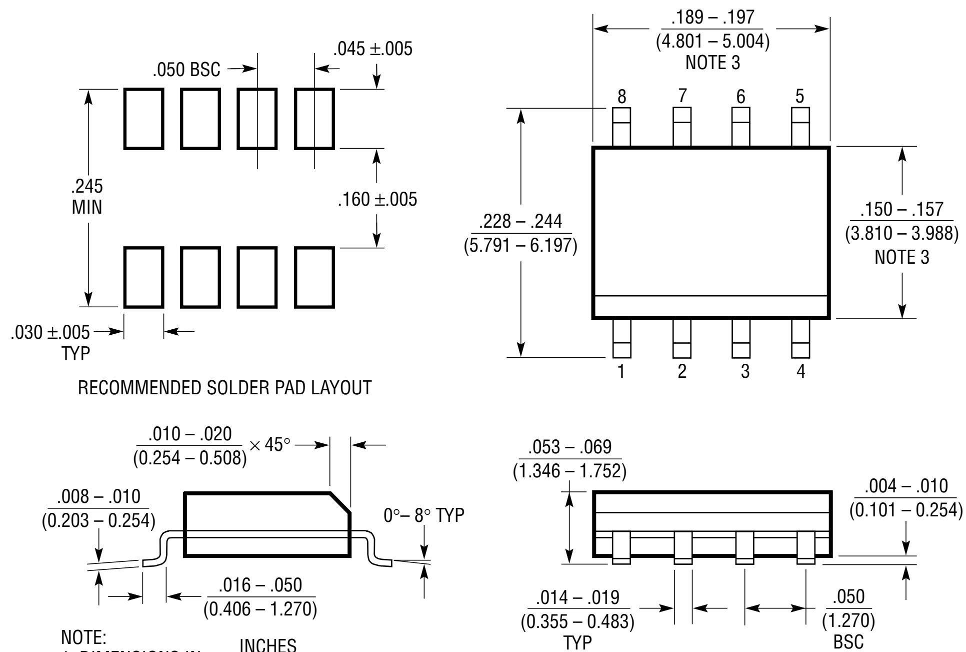


Figure 11. LTC6227-LT5401 Based Instrumentation Amplifier Transient Response

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)

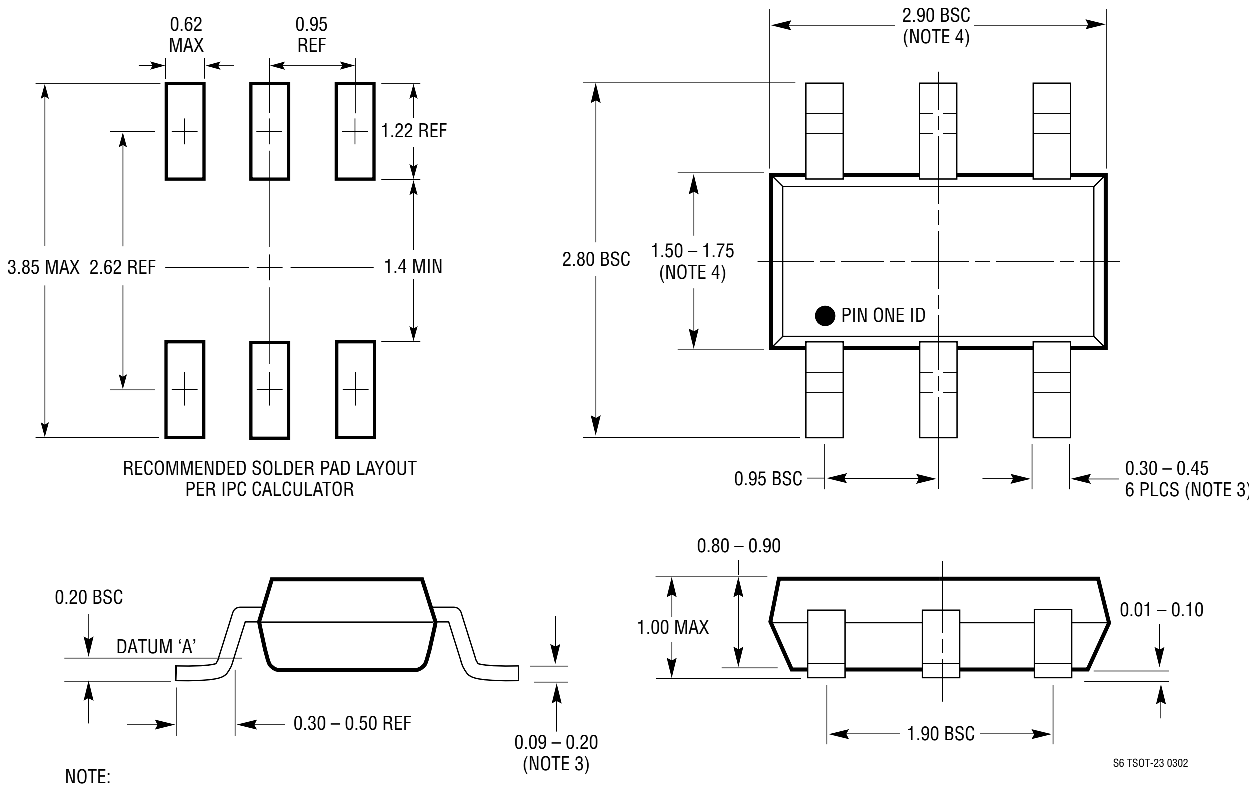


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

PACKAGE DESCRIPTION

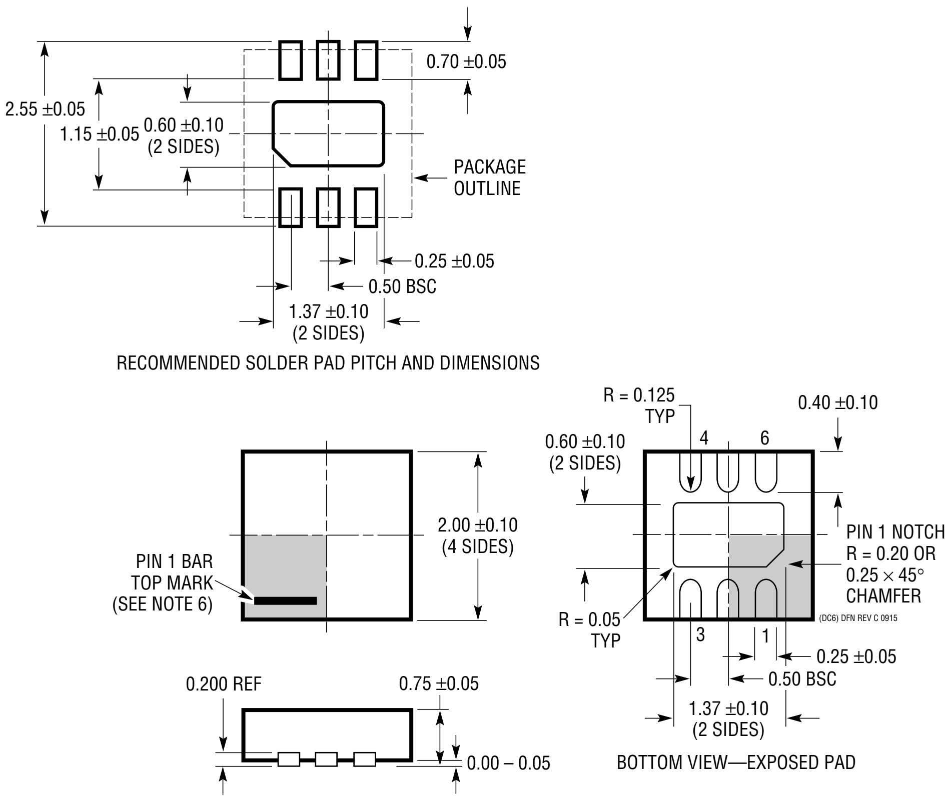
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

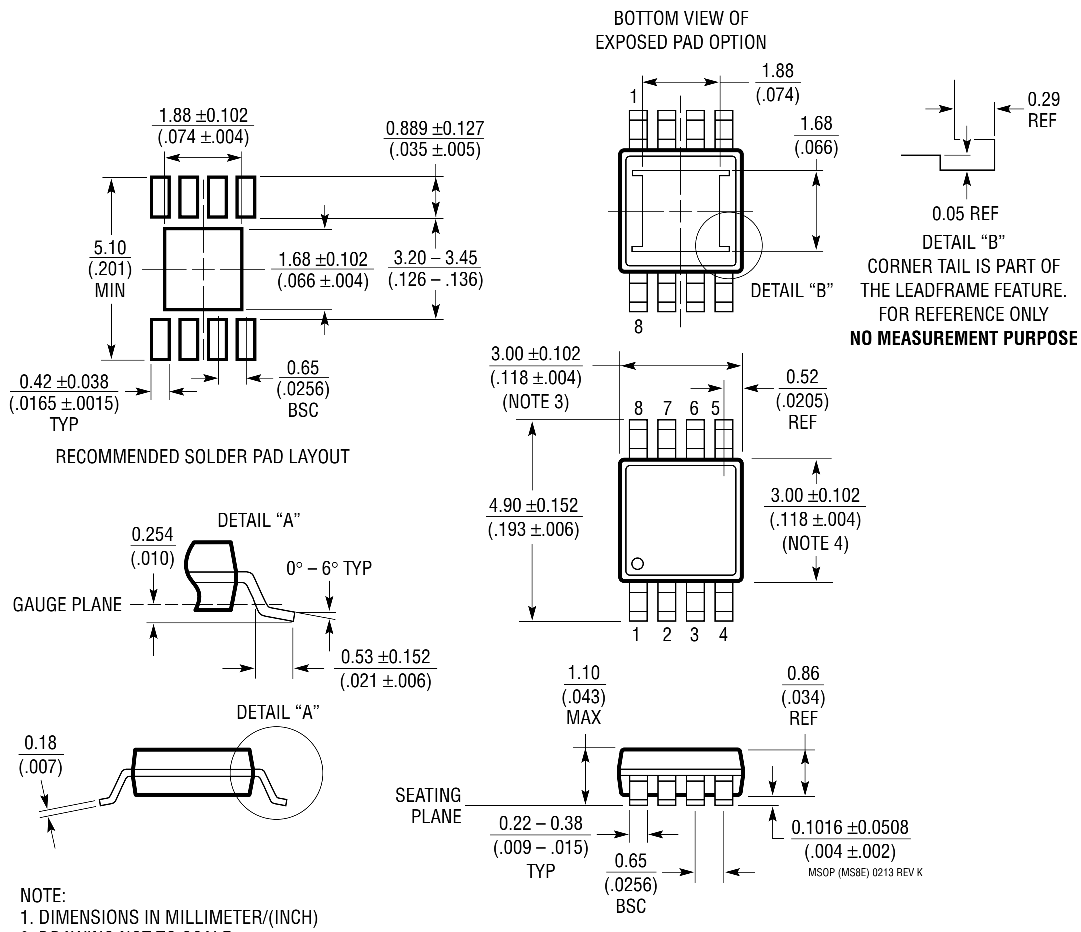
DC6 Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

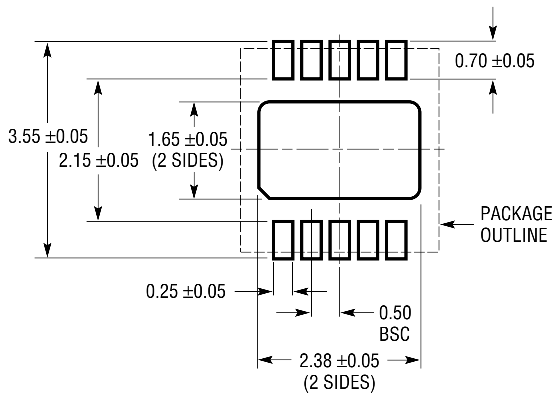
MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



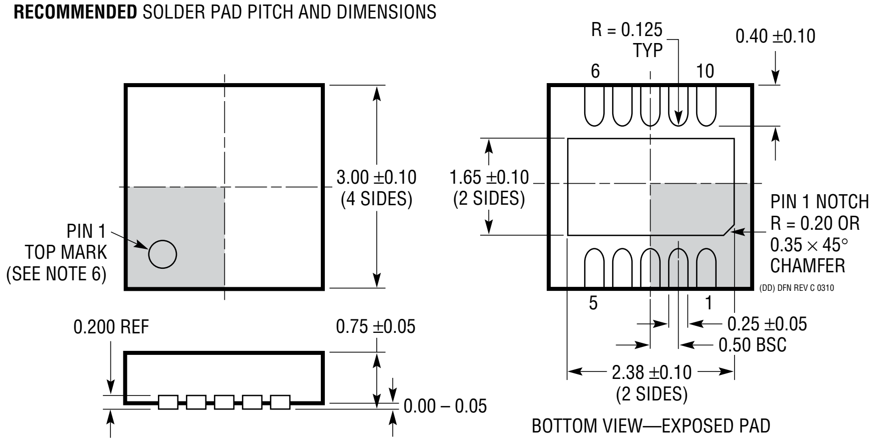
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

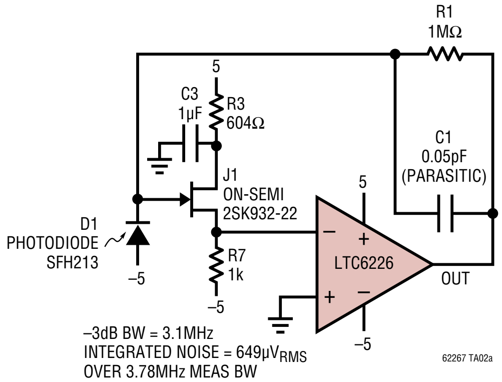


BOTTOM VIEW—EXPOSED PAD

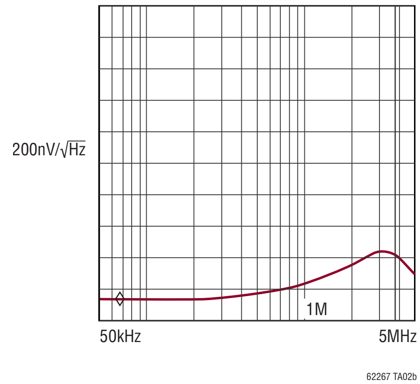
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

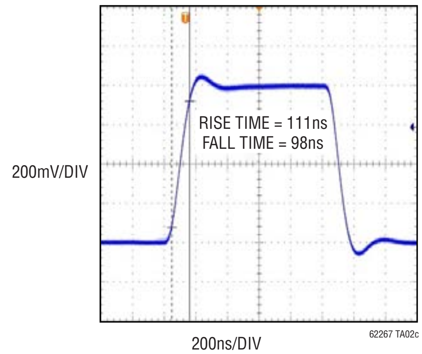
High Speed High Dynamic Range Photodiode Amplifier



Photodiode Amplifier Noise Spectrum



Photodiode Amplifier Transient Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Operational Amplifiers		
LTC6228/LTC6229	Single/Dual High Speed Ultra Low Noise Low Distortion Rail-to-Rail Output Op Amps	0.88 nV/√Hz, 730MHz, 500V/µs Unity Gain Stable
LTC6252/LTC6253/ LTC6254	Single/Dual/Quad High Speed Rail-to-Rail Input and Output Op Amps	720MHz, 3.5mA, 2.75nV/√Hz, 280V/µs, 0.35mV, Unity Gain Stable
ADA4899-1	High Speed Ultra Low Noise Ultra Low Distortion	1 nV/√Hz, 600MHz, 310V/µs Unity Gain Stable
LTC6268/LTC6269	Single/Dual High Speed FET Input Op Amp	400MHz, 4nV/√Hz, ±3f_A Input Bias Current
LT1818/LT1819	Single/Dual Wide Bandwidth, High Slew Rate Low Noise and Distortion Op Amps	400MHz, 9mA, 6nV/√Hz, 2500V/µs, 1.5mV –85dBc at 5MHz
ADA4896-1/ ADA4896-2	Low Noise Low Power Rail-to-Rail Output	3mA 1 nV/√Hz 230 MHz 120 V/µs Unity Gain Stable
LT6230/LT6231/ LT6232	Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps	215MHz, 3.5mA, 1.1nV/√Hz, 70V/µs, 350µV
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad High Speed Rail-to-Rail Input and Output Op Amps	180MHz, 1mA, 4.2nV/√Hz, 90V/µs, 0.5mV
LT6200/LT6201	Single/Dual Ultralow Noise Rail-to-Rail Input/Output Op Amps	165MHz, 20mA, 0.95nV/√Hz, 44V/µs, 1mV
LT6202/LT6203/ LT6204	Single/Dual/Quad Ultralow Noise Rail-to-Rail Op Amp	100MHz, 3mA, 1.9nV/√Hz, 25V/µs, 0.5mV
LT1801/LT1802	Dual/Quad Low Power High Speed Rail-to-Rail Input and Output Op Amps	80MHz, 2mA, 8.5nV√Hz, 25V/µs, 350µV
LT1028	Ultralow Noise, Precision High Speed Op Amps	75MHz, 9.5mA, 0.85nV/√Hz, 11V/µs, 40µV
LTC6350	Low Noise Single-Ended to Differential Converter/ADC Driver	33MHz (–3dB), 4.8mA, 1.9nV/√Hz, 240ns Settling to 0.01% 8V_{P-P}
ADCs		
LTC2387-18	18-Bit, 15Msps SAR-ADC	95.7dB SNR
AD7380	4Msps 16-Bit SAR-ADC	92dB DNR SNR, 6.6 V_{P-P} Input Range
LTC2323-16	5Msps 16-Bit SAR-ADC	81dB SNR,8V_{P-P} Input Range
AD4020	1.8 Msps 20-Bit SAR-ADC	99 dB SNR