

M5M5256BP, BFP, BKP-70, -85, -10, -12, -15, -70L, -85L, -10L, -12L, -15L, -70LL, -85LL, -10LL, -12LL, -15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256BP, BFP, BKP is a 262,144-bit CMOS static RAM organized as 32,768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

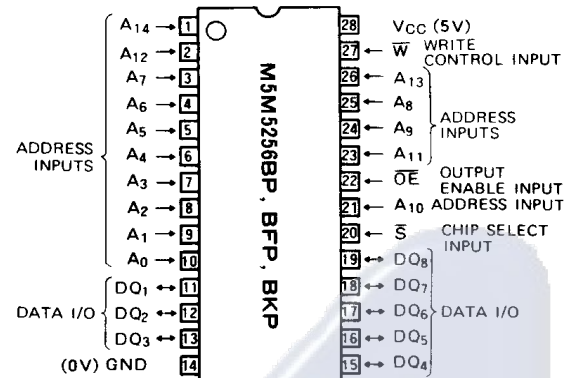
The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256BP, BFP, BKP-70	70 ns	70 mA	2 mA
M5M5256BP, BFP, BKP-85	85 ns		
M5M5256BP, BFP, BKP-10	100 ns		
M5M5256BP, BFP, BKP-12	120 ns		
M5M5256BP, BFP, BKP-15	150 ns		
M5M5256BP, BFP, BKP-70L	70 ns	70 mA	100 μ A ($V_{CC} = 5.5V$) 50 μ A ($V_{CC} = 3.0V$)
M5M5256BP, BFP, BKP-85L	85 ns		
M5M5256BP, BFP, BKP-10L	100 ns		
M5M5256BP, BFP, BKP-12L	120 ns		
M5M5256BP, BFP, BKP-15L	150 ns		
M5M5256BP, BFP, BKP-70LL	70 ns	70 mA	20 μ A ($V_{CC} = 5.5V$) 10 μ A ($V_{CC} = 3.0V$)
M5M5256BP, BFP, BKP-85LL	85 ns		
M5M5256BP, BFP, BKP-10LL	100 ns		
M5M5256BP, BFP, BKP-12LL	120 ns		
M5M5256BP, BFP, BKP-15LL	150 ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability

PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (BP)
28P2W-C (BFP)
28P4Y (BKP)

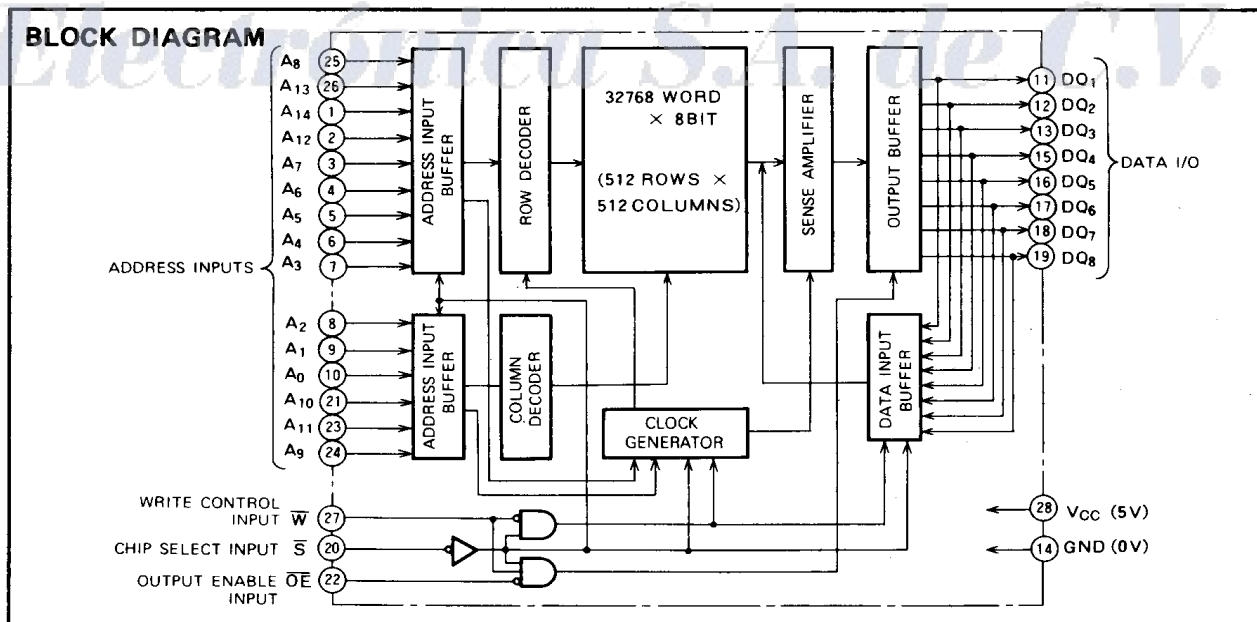
- Simple Memory Expansion by $\bar{S}$
- $\bar{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O
- Package

M5M5256BP 28 Pin 600 mil DIP
M5M5256BKP 28 Pin 300 mil DIP
M5M5256BFP . 28 Pin Small Outline Package (SOP)

APPLICATION

Small Capacity Memory Units.

BLOCK DIAGRAM



M5M5256BP, BFP, BKP-70, -85, -10, -12, -15, -70L, -85L, -10L, -12L, -15L, -70LL, -85LL, -10LL, -12LL, -15LL

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FUNCTION

The operation mode of the M5M5256BP, BFP, BKP is determined by a combination of the device control inputs $\bar{S}$, $\bar{W}$ and $\bar{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\bar{W}$ overlaps with the low level $\bar{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\bar{W}$, $\bar{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\bar{OE}$ directly controls the output stage. Setting the $\bar{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\bar{W}$ at a high level and $\bar{OE}$ at a low level while $\bar{S}$ are in an active state.

When setting $\bar{S}$ at a high level, the chip is in a non-

selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\bar{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\bar{S}$	$\bar{W}$	$\bar{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	$-0.3 \sim 7$	V
V_I	Input voltage		$-0.3 \sim V_{CC} + 0.3$	V
V_O	Output voltage		$0 \sim V_{CC}$	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		$0 \sim 70$	$^\circ\text{C}$
T_{stg}	Storage temperature		$-65 \sim 150$	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} \pm 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		$V_{CC} + 0.3$	V
V_{IL}	Low input voltage		-0.3		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input leakage current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_O	Output leakage current	$\bar{S} = V_{IH}$ or $\bar{OE} = V_{IH}$, $V_{I/O} = 0 \sim V_{CC}$			± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\bar{S} < 0.2$, $\bar{W} > V_{CC} - 0.2$, Output open Other input < 0.2 or $> V_{CC} - 0.3$ Min. cycle		30	65	mA
I_{CC2}	Active supply current (AC, TTL level)	$\bar{S} = V_{IL}$, $\bar{W} = V_{IH}$, Output open Other input $= V_{IL}$ or V_{IH} Min. cycle		35	70	mA
I_{CC3}	Stand by supply current	$\bar{S} \geq V_{CC} - 0.2\text{V}$			2	mA
		Other inputs $= 0 \sim V_{CC}$			100	μA
					20	μA
I_{CC4}	Stand by supply current	$\bar{S} = V_{IH}$, Other inputs $= 0 \sim V_{CC}$			3	mA
C_i	Input capacitance ($T_a = 25^\circ\text{C}$)	$V_I = \text{GND}$, $V_I = 25\text{mVrms}$, $f = 1\text{MHz}$			6	pF
C_O	Output capacitance ($T_a = 25^\circ\text{C}$)	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)

2 Typical value is $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$



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262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

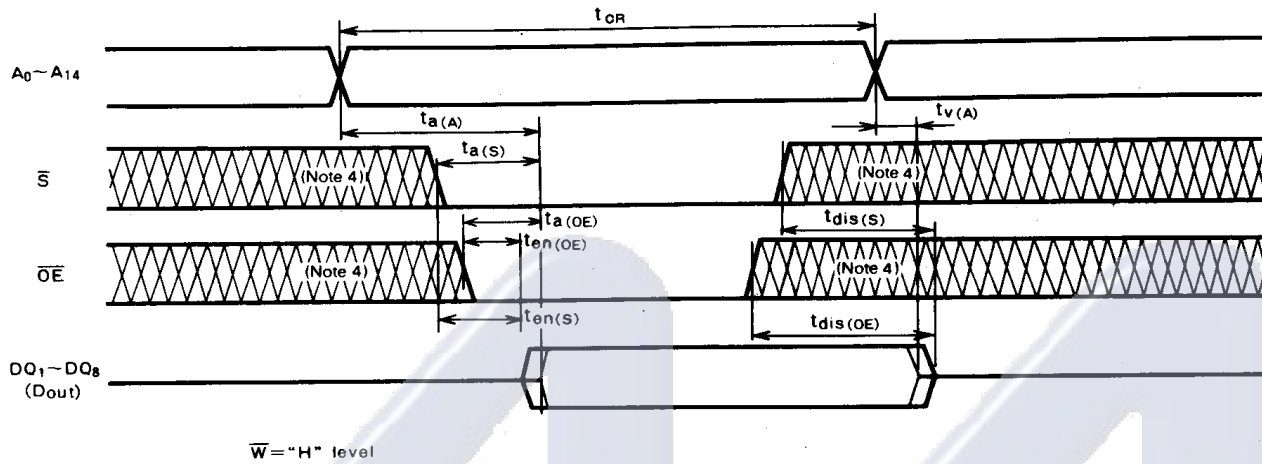
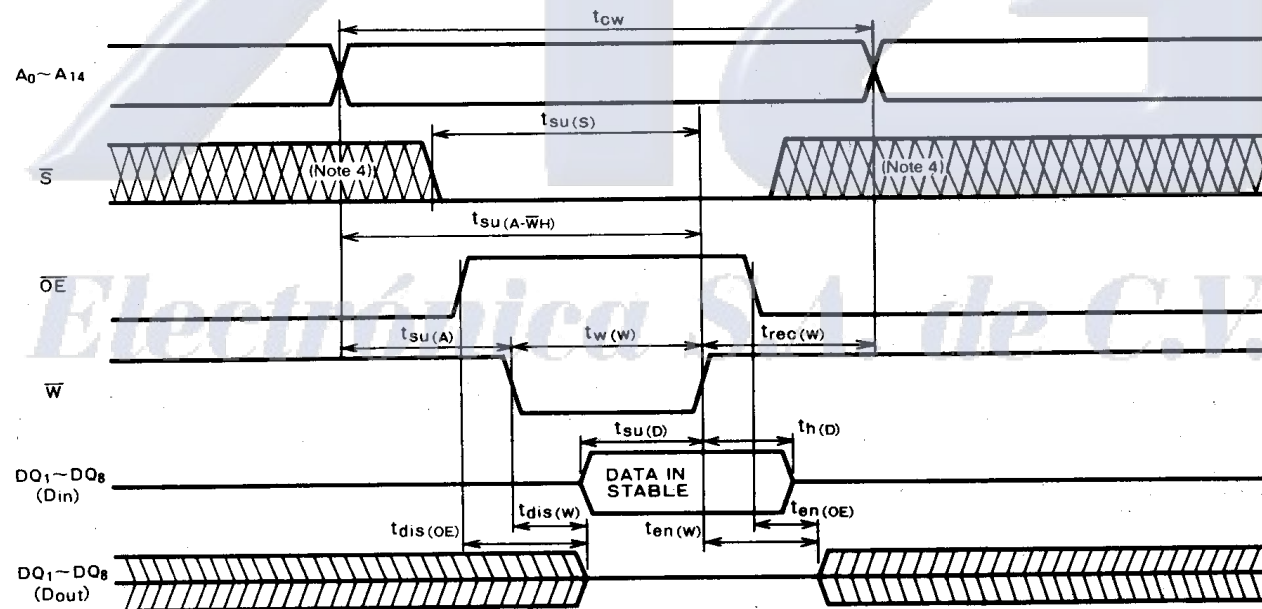
Read cycle

Symbol	Parameter	Limits										Unit
		M5M5256-70		M5M5256-85		M5M5256-10		M5M5256-12		M5M5256-15		
		M5M5256-70L		M5M5256-85L		M5M5256-10L		M5M5256-12L		M5M5256-15L		
		M5M5256-70LL		M5M5256-85LL		M5M5256-10LL		M5M5256-12LL		M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	70		85		100		120		150		ns
t _a (A)	Address access time		70		85		100		120		150	ns
t _a (S)	Chip select access time		70		85		100		120		150	ns
t _a (OE)	Output enable access time		35		45		50		60		75	ns
t _{dis} (S)	Output disable time after $\overline{S}$ high		30		30		35		40		45	ns
t _{dis} (OE)	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
t _{en} (S)	Output enable time after $\overline{S}$ low	5		5		10		10		10		ns
t _{en} (OE)	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns
t _v (A)	Data valid time after address change	20		20		20		20		20		ns

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Write cycle

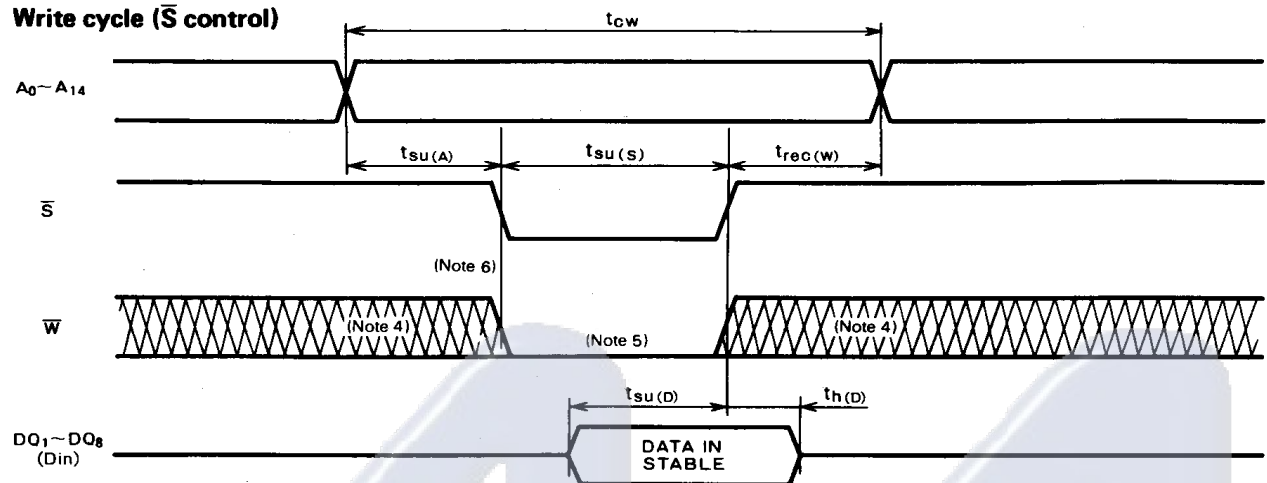
Symbol	Parameter	Limits										Unit
		M5M5256-70		M5M5256-85		M5M5256-10		M5M5256-12		M5M5256-15		
		M5M5256-70L		M5M5256-85L		M5M5256-10L		M5M5256-12L		M5M5256-15L		
		M5M5256-70LL		M5M5256-85LL		M5M5256-10LL		M5M5256-12LL		M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{CW}	Write cycle time	70		85		100		120		150		ns
t _{w(W)}	Write pulse width	55		60		60		70		80		ns
t _{su(A)}	Address set up time	0		0		0		0		0		ns
t _{su(A-$\overline{W}$H)}	Address set up time with respect to $\overline{W}$ high	65		75		80		85		90		ns
t _{su(S)}	Chip select set up time	65		75		80		85		90		ns
t _{su(D)}	Data set up time	30		35		35		40		50		ns
t _{h(D)}	Data hold time	0		0		0		0		0		ns
t _{rec(W)}	Write recovery time	0		0		0		0		0		ns
t _{dis(W)}	Output disable time after $\overline{W}$ low		25		30		35		40		45	ns
t _{dis(OE)}	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
t _{en(W)}	Output enable time after $\overline{W}$ high	5		5		10		10		10		ns
t _{en(OE)}	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns

**M5M5256BP, BFP, BKP-70, -85, -10, -12, -15, -70L, -85L,
-10L, -12L, -15L, -70LL, -85LL, -10LL, -12LL, -15LL****262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM****TIMING DIAGRAM****Read cycle****Write cycle ($\overline{W}$ control)**

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Write cycle ($\bar{S}$ control)



Note 3: Test condition

Input pulse level $V_{IH} = 2.4V$, $V_{IL} = 0.6V$

Input rise and fall time 10ns

Reference level $V_{OH} = V_{OL} = 1.5V$

Output loads Fig. 1, $C_L = 100pF$ (BP, BFP, BKP-85, -10, -12, -15, -85L, -10L, -12L, -15L, -85LL, -10LL, -12LL, -15LL)

$C_L = 30pF$ (BP, BFP, BKP-70, -70L, -70LL)

$C_L = 5pF$ (for t_{en} , t_{dis})

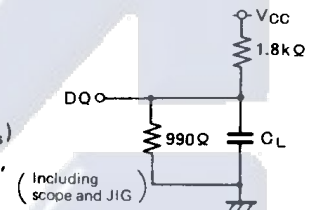


Fig. 1 Output load

Note 4: Hatching indicates the state is don't care.

5: Writing is executed in overlap of $\bar{S}$ and $\bar{W}$ low.

6: If $\bar{W}$ goes low simultaneously with or prior to $\bar{S}$, the output remains in the high-impedance state.

7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\bar{S})$	Chip select input $\bar{S}$	$2.2V \leq V_{CC(PD)}$	2.2			V
		$2V \leq V_{CC(PD)} \leq 2.2V$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3V$, Other inputs = 3V			2	mA
					50	μA
					10*	μA

* $T_a = 25^\circ C$, $I_{CC(PD)} = 1\mu A$

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

