MAX232x Dual EIA-232 Drivers/Receivers

1 Features

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0-µF Charge-Pump Capacitors
- Operates up to 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current: 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1-µF Charge-Pump Capacitors is Available With the MAX202 Device

2 Applications

- TIA/EIA-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

3 Description

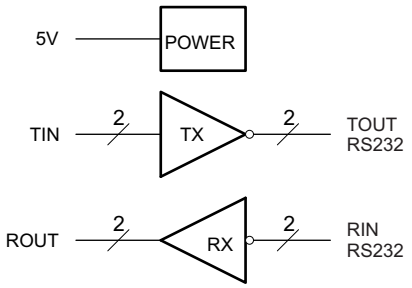
The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels.

Device Information(1)

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
MAX232x	SOIC (16)	9.90 mm × 3.91 mm
	SOIC (16)	10.30 mm × 7.50 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOP (16)	10.3 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

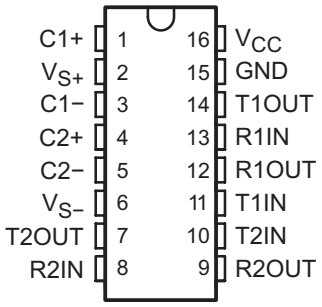
Changes from Revision L (March 2004) to Revision M **Page**

- Removed Ordering Information table. ... 1
- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Moved T_{stg} to Handling Ratings table. ... 4

6 Pin Configuration and Functions

Top View

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
VS+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
VS-	6	O	Negative charge pump output for storage capacitor only
T2OUT, T1OUT	7, 14	O	RS232 line data output (to remote RS232 system)
R2IN, R1IN	8, 13	I	RS232 line data input (from remote RS232 system)
R2OUT, R1OUT	9, 12	O	Logic data output (to UART)
T2IN, T1IN	10, 11	I	Logic data input (from UART)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 5V power supply

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Input Supply voltage range(2)		–0.3	6	V
V_{S+}	Positive output supply voltage range		V_{CC} – 0.3	15	V
$V_{S–}$	Negative output supply voltage range		–0.3	–15	V
V_I	Input voltage range	T1IN, T2IN	–0.3	V_{CC} + 0.3	V
		R1IN, R2IN		±30	
V_O	Output voltage range	T1OUT, T2OUT	$V_{S–}$ – 0.3	V_{S+} + 0.3	V
		R1OUT, R2OUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	T1OUT, T2OUT	Unlimited		
T_J	Operating virtual junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	–40		85	

7.4 Thermal Information

THERMAL METRIC(1)		MAX232xD	MAX232xDW	MAX232xN	MAX232xNS	UNIT
		SOIC	SOIC wide	PDIP	SOP	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	57	67	64	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics –– Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V, all outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V
(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

7.6 Electrical Characteristics –– Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
V_{OL}	Low-level output voltage(3)	T1OUT, T2OUT	R_L = 3 kΩ to GND		–7	–5	V
r_O	Output resistance	T1OUT, T2OUT	$V_{S+} = V_{S-} = 0$, V_O = ±2 V	300			Ω
I_{OS}(4)	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0 V		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	µA

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

7.7 Electrical Characteristics –– Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = –1 mA	3.5			V
V_{OL}	Low-level output voltage(3)	R1OUT, R2OUT	I_{OL} = 3.2 mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	V
r_I	Receiver input resistance	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

7.8 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(1)	MAX	UNIT
SR	Driver slew rate	RL = 3 kΩ to 7 kΩ, see Figure 4			30	V/µs
SR(t)	Driver transition region slew rate	see Figure 5		3		V/µs
	Data rate	One TOUT switching		120		kbit/s
$t_{PLH®)}$	Receiver propagation delay time, low- to high-level output	TTL load, see Figure 3		500		ns
$t_{PHL®)}$	Receiver propagation delay time, high- to low-level output	TTL load, see Figure 3		500		ns

(1) Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

7.9 Typical Characteristics

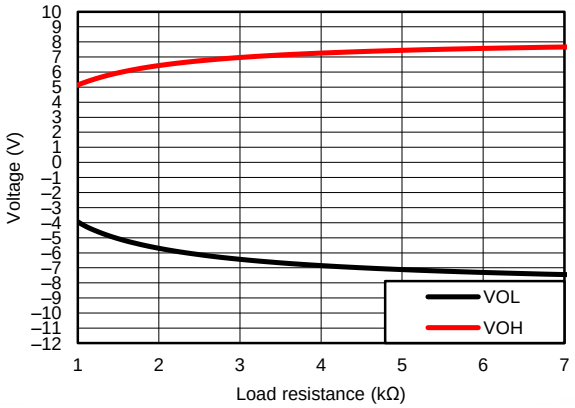


Figure 1. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

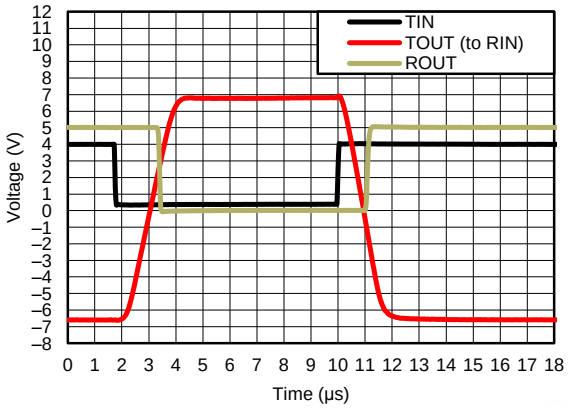
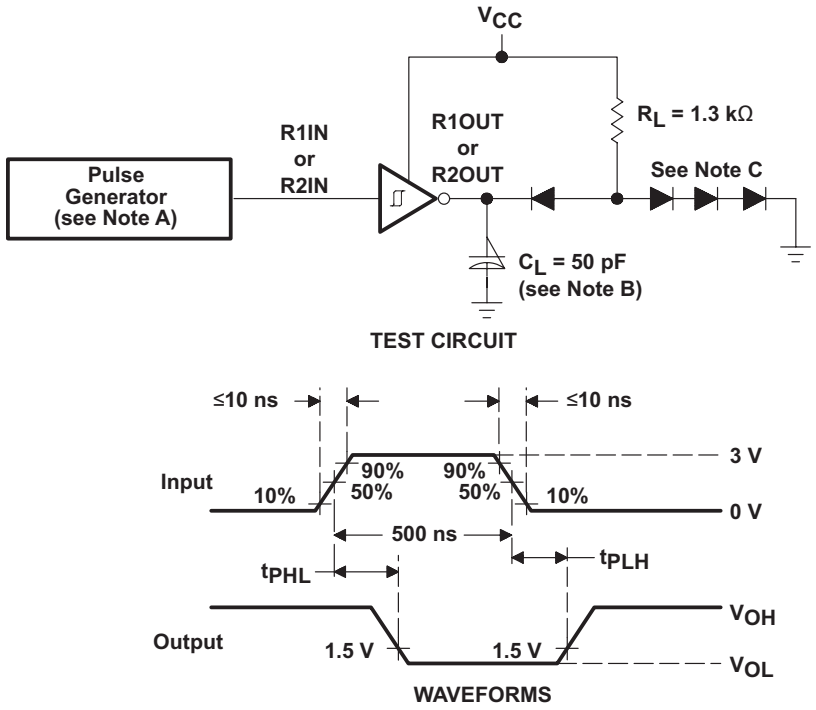


Figure 2. Driver to Receiver Loopback Timing Waveform

8 Parameter Measurement Information



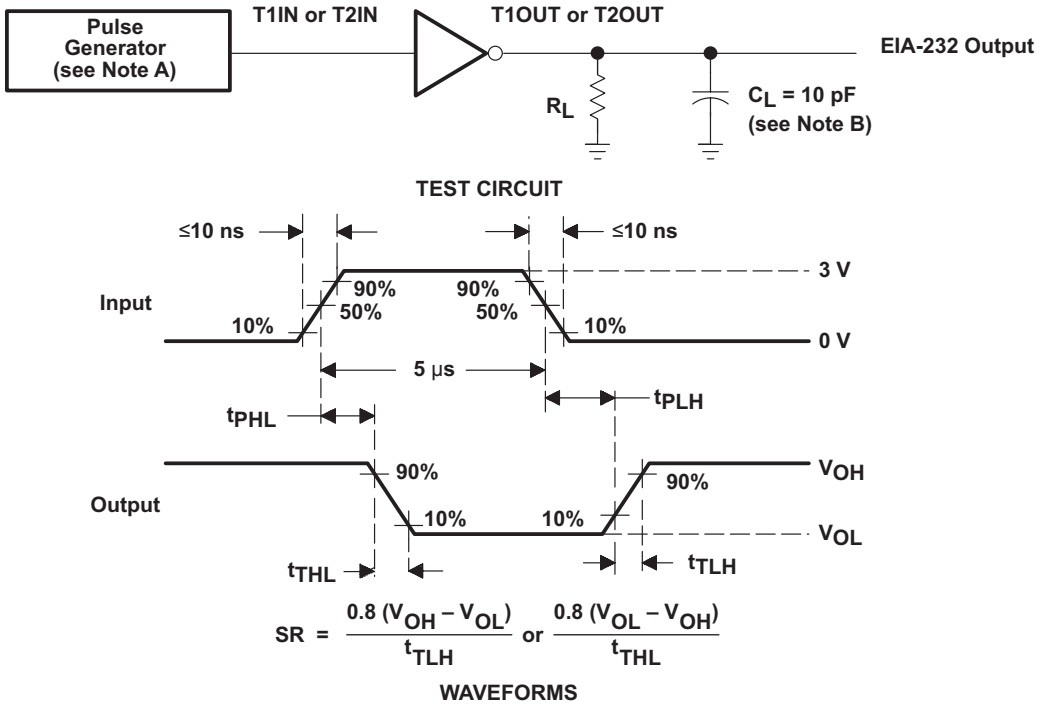
A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

Figure 3. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

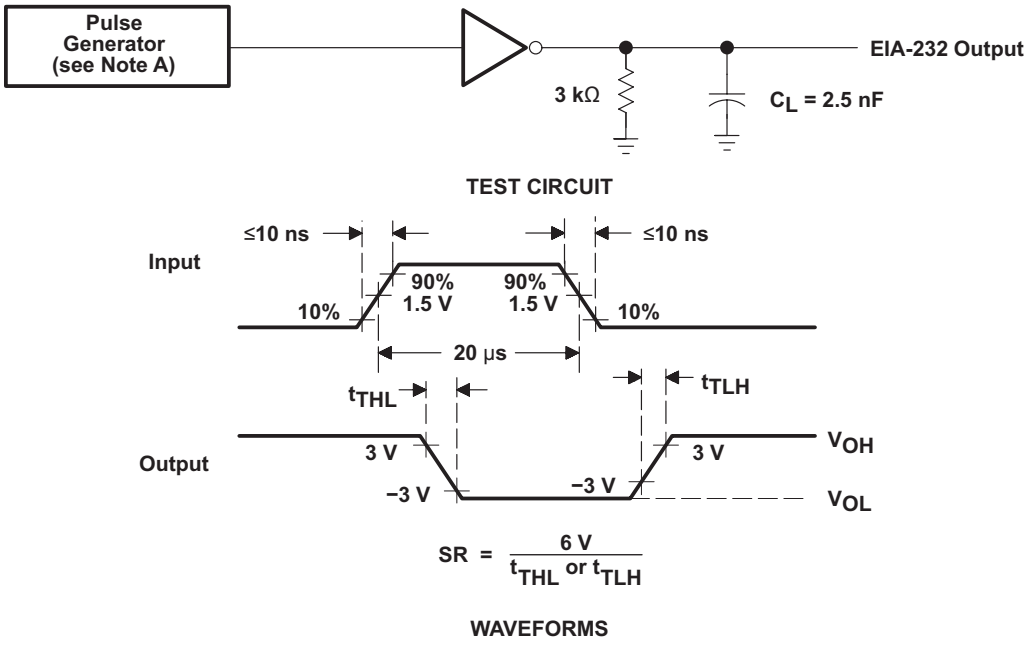
Parameter Measurement Information (continued)



A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)



A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

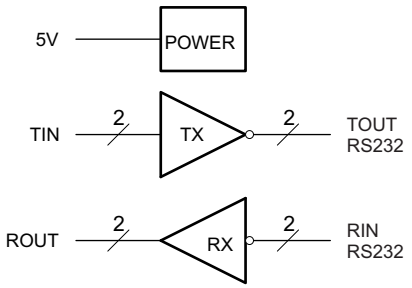
Figure 5. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

9 Detailed Description

9.1 Overview

The MAX232 device is a dual driver/receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library. Outputs are protected against shorts to ground.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power

The power block increases and inverts the 5V supply for the RS232 driver using a charge pump that requires four 1-µF external capacitors.

9.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Internal pull up resistors on TIN inputs ensures a high input when the line is high impedance.

9.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT.

9.4 Device Functional Modes

9.4.1 V_{CC} powered by 5V

The device will be in normal operation.

9.4.2 V_{CC} unpowered

When MAX232 is unpowered, it can be safely connected to an active remote RS232 device.

Table 1. Function Table Each Driver(1)

INPUT TIN	OUTPUT TOUT
L	H
H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 2. Function Table Each Receiver(1)

INPUTS RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

10 Application and Implementation

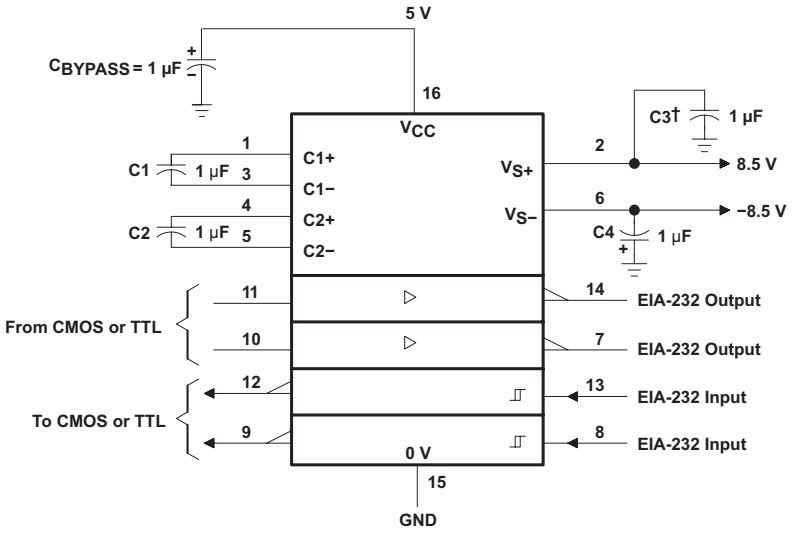
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

For proper operation add capacitors as shown in Figure 6. Pins 9 through 12 connect to UART or general purpose logic lines. EIA-232 lines will connect to a connector or cable.

10.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX202 can operate with 0.1-µF capacitors.

Figure 6. Typical Operating Circuit

10.2.1 Design Requirements

- V_{CC} minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 120 kbps.

10.2.2 Detailed Design Procedure

Use 1 uF tantalum or ceramic capacitors.

Typical Application (continued)

10.2.3 Application Curves

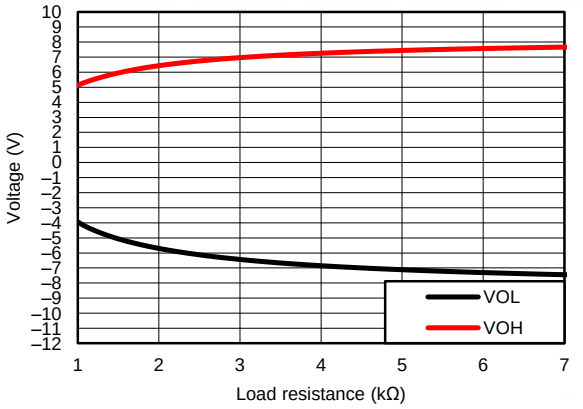


Figure 7. TOUT VOH & VOL vs Load Resistance, Both Drivers Loaded

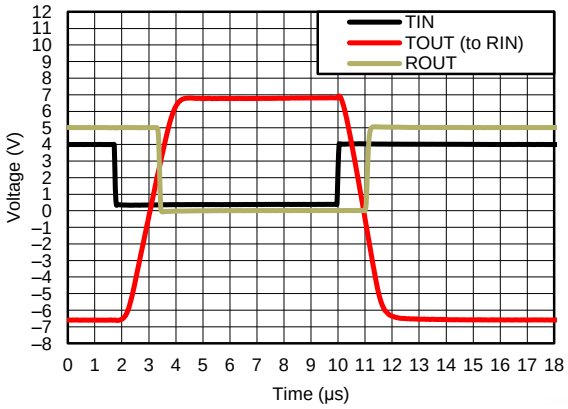


Figure 8. Driver to Receiver Loopback Timing Waveform

11 Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to TIN pins. V_{CC} should be between 4.5V and 5.5V.

12 Layout

12.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

12.2 Layout Example

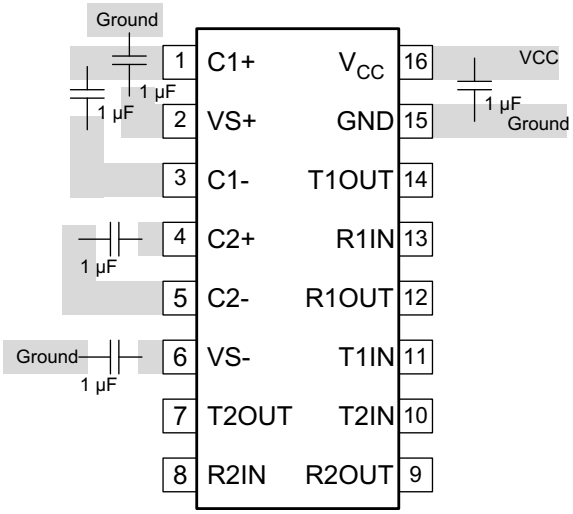
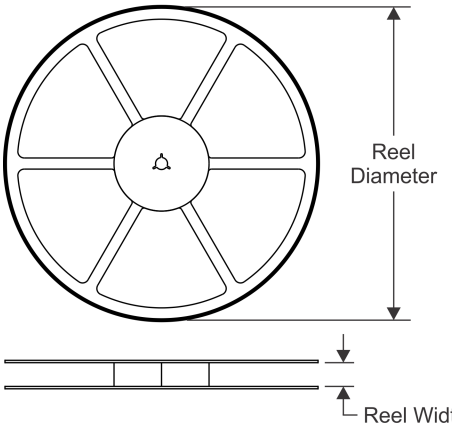


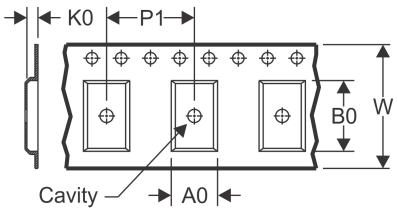
Figure 9. Layout Schematic

TAPE AND REEL INFORMATION

REEL DIMENSIONS

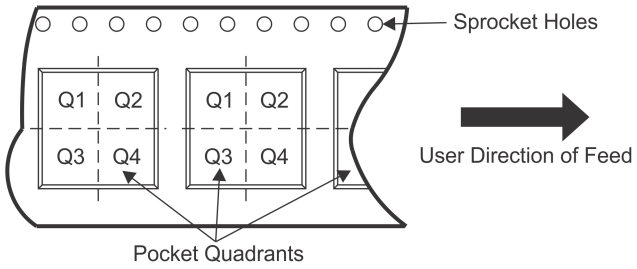


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

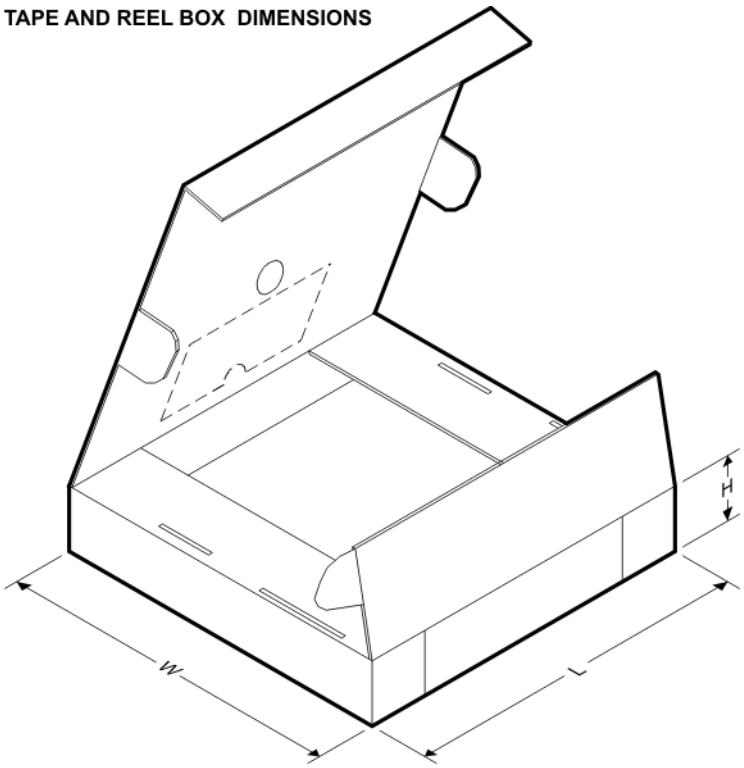
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232DWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232IDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



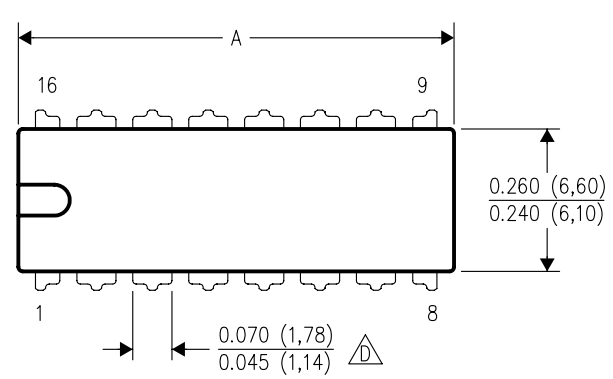
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232DR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232DR	SOIC	D	16	2500	367.0	367.0	38.0
MAX232DRG4	SOIC	D	16	2500	333.2	345.9	28.6
MAX232DRG4	SOIC	D	16	2500	367.0	367.0	38.0
MAX232DWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232DWRG4	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232IDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232IDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232IDWRG4	SOIC	DW	16	2000	367.0	367.0	38.0

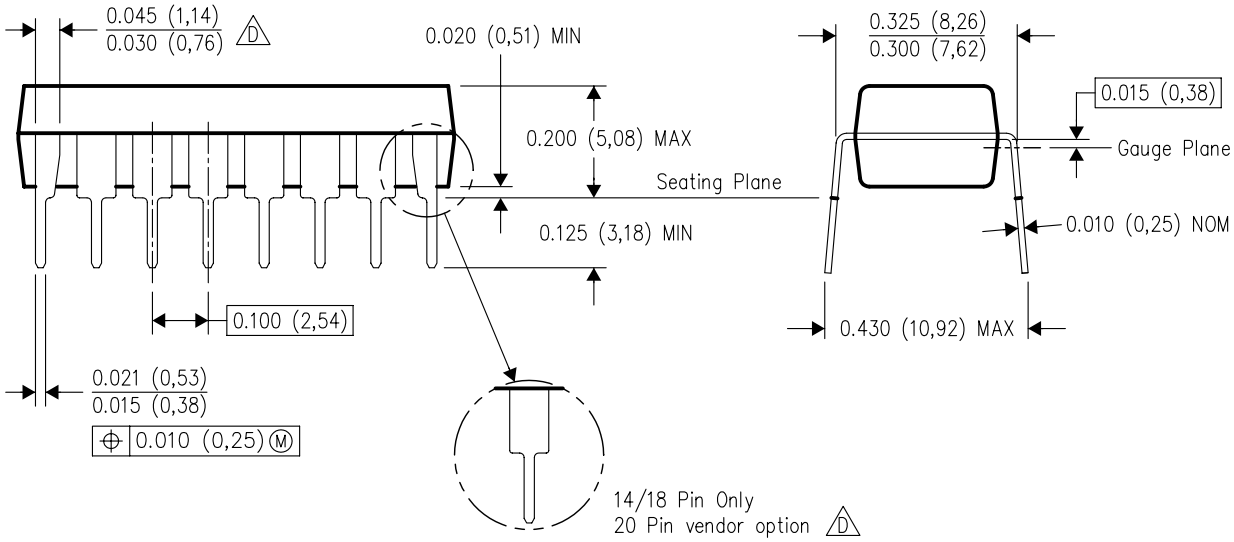
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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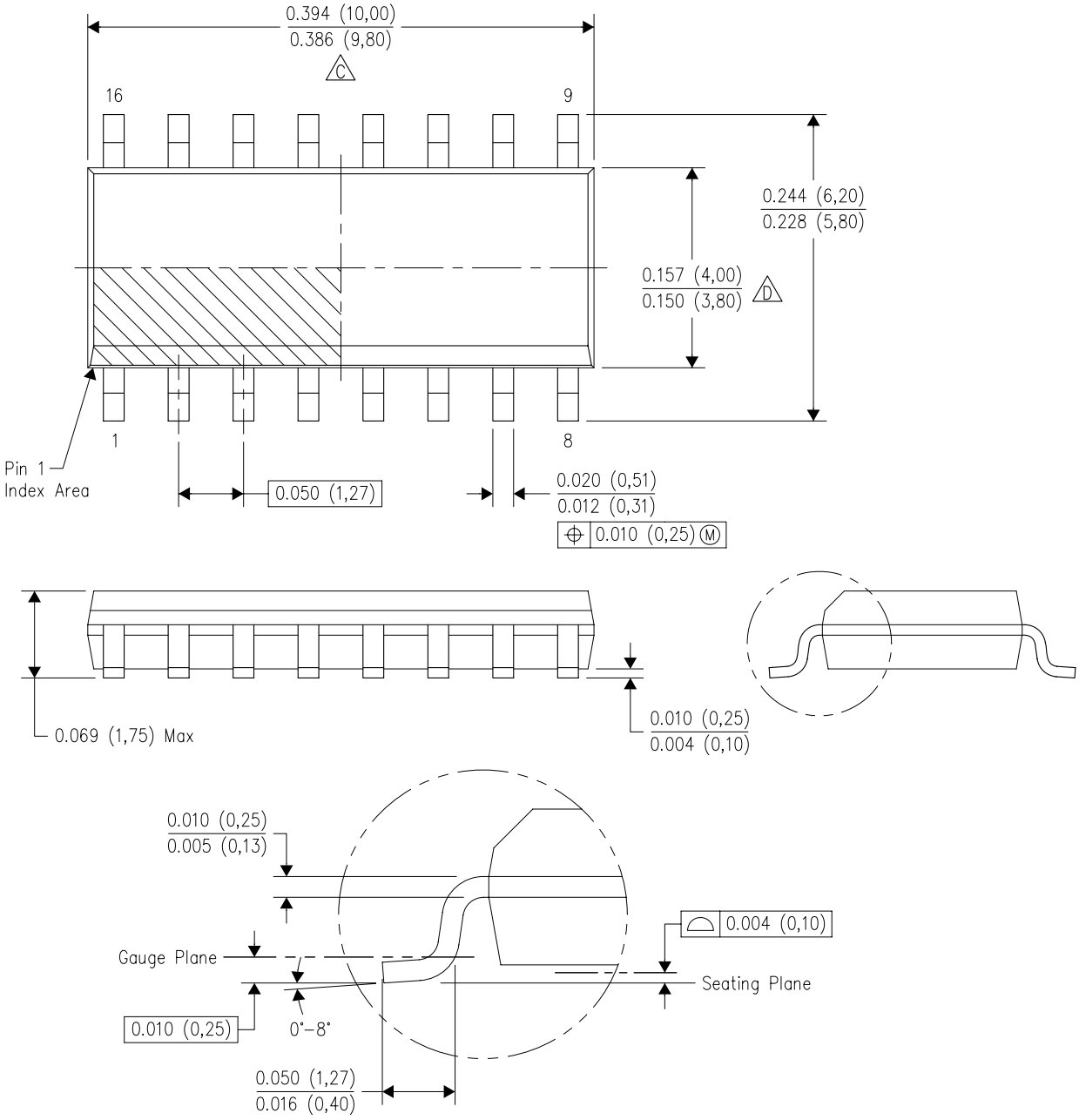
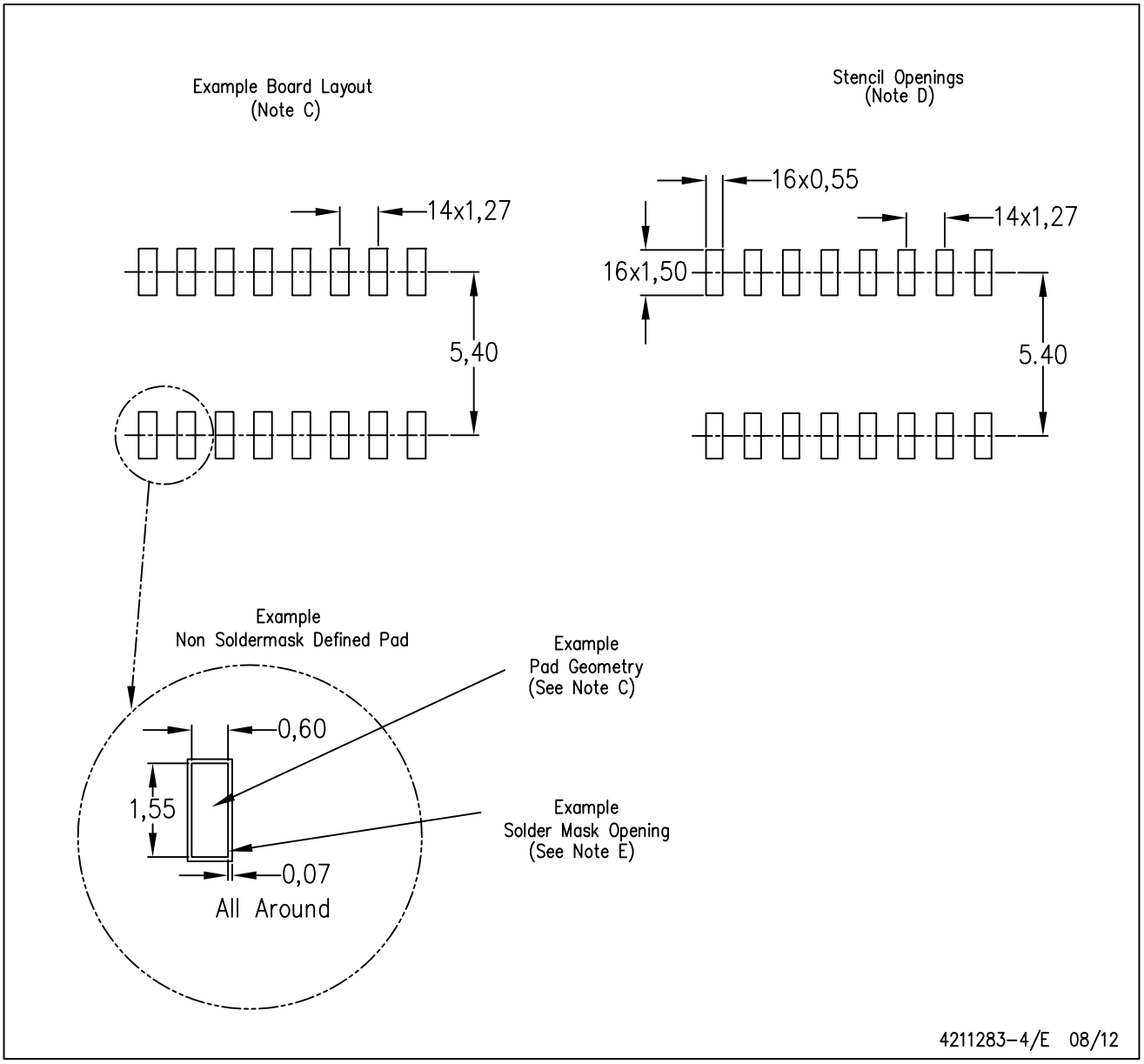
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



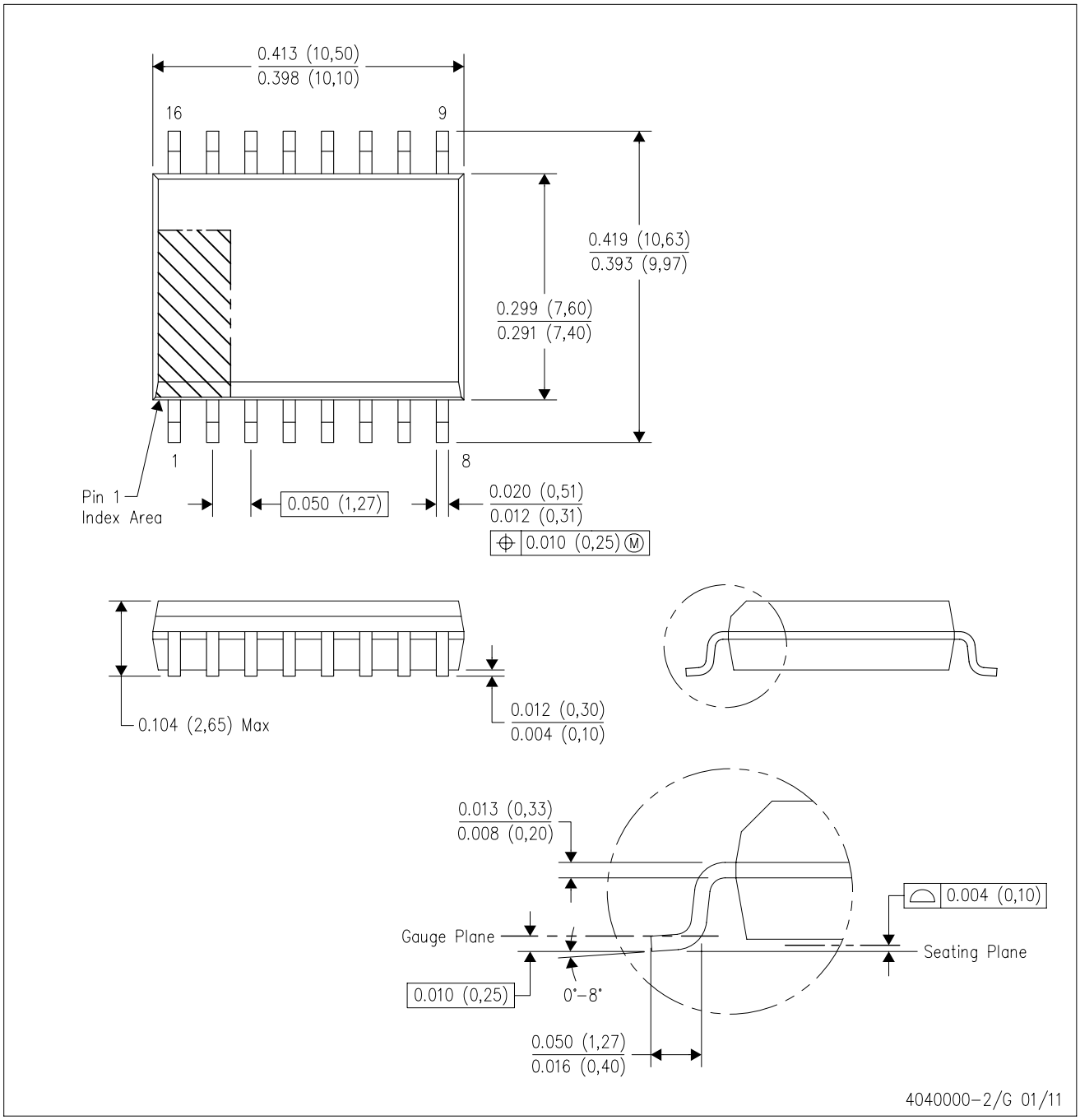
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE

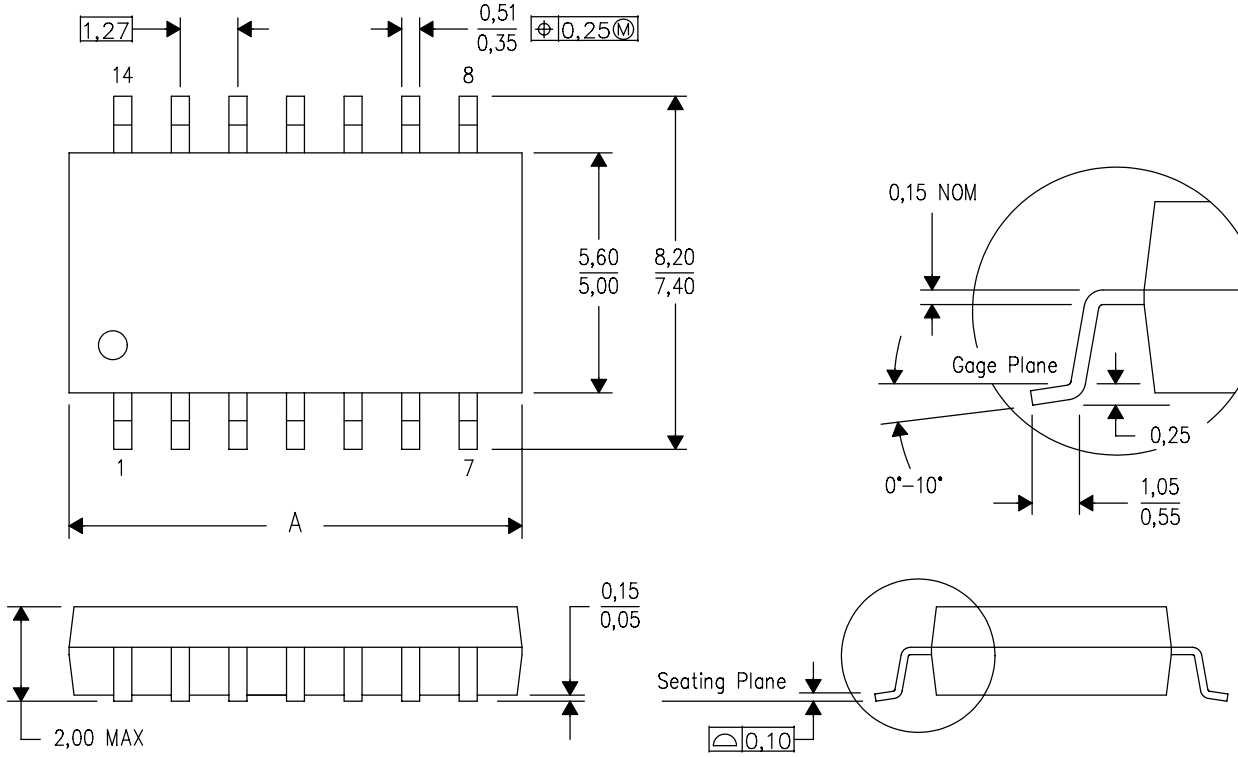


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.