

February 1995

MM5450/MM5451 LED Display Drivers

General Description

The MM5450 and MM5451 are monolithic MOS integrated circuits utilizing N-channel metal-gate low threshold, enhancement mode, and ion-implanted depletion mode devices. They are available in 40-pin molded or cavity dual-in-line packages. The MM5450/MM5451 is designed to drive common anode-separate cathode LED displays. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} .

Applications

- COPSTM or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA sink capability
- Alphanumeric capability
- θ_{JA} DIP

Board = 49°C/W
Socket = 54°C/W

Block Diagram

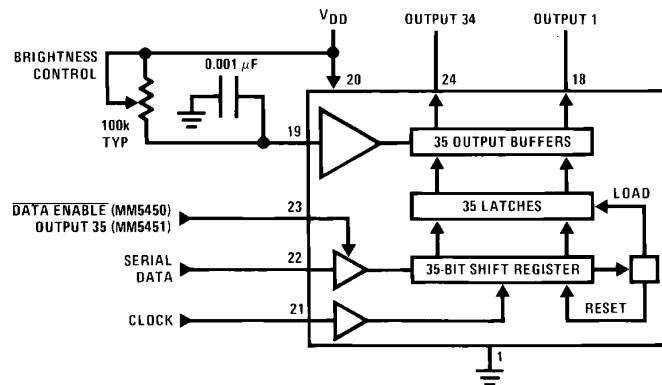


FIGURE 1

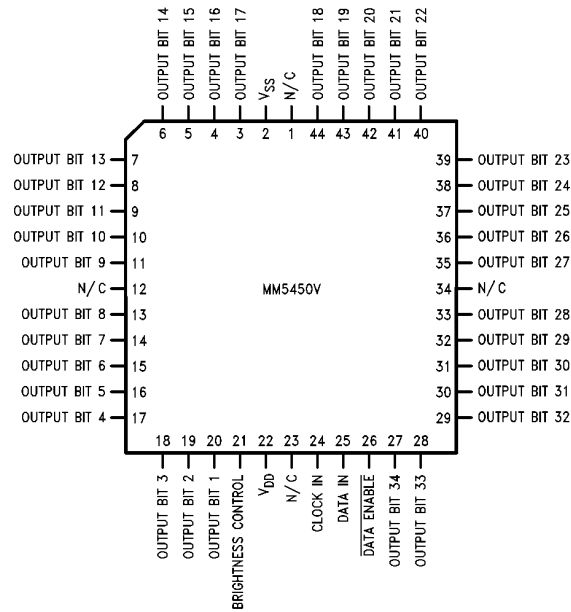
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COPSTM is a trademark of National Semiconductor Corporation.

See NS Package Number N40A or V44A

Connection Diagrams (Continued)

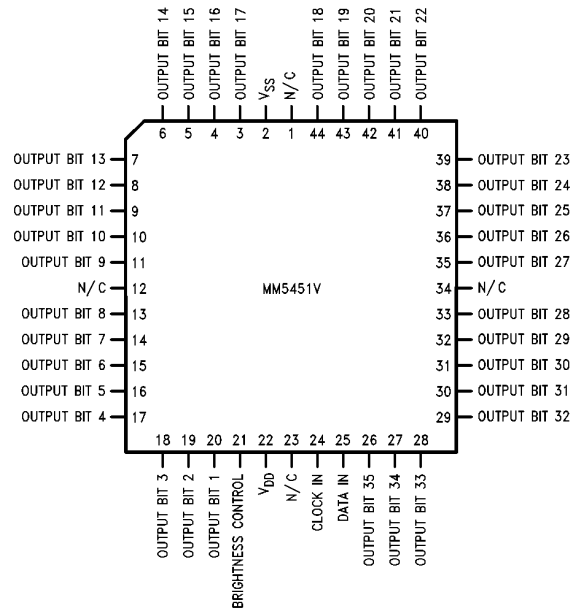
Plastic Chip Carrier



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Top View

Plastic Chip Carrier



TL/F/6136-14

Top View

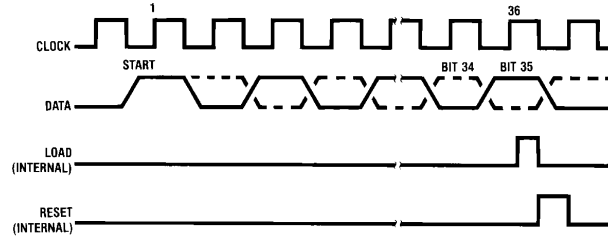
Figure 4 shows the input data format. A start bit of logical “1” precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

$$\theta_{JA} \text{ (Board Mount)} = 49^{\circ}\text{C/W}$$

The timing diagram illustrates the relationship between three signals: CLOCK, DATA, and DATA ENABLE (MM5450). The CLOCK signal is a periodic waveform with high level V_H and low level V_L . Its timing parameters include high pulse width t_{H1} , high-to-low transition time t_{DH} , low pulse width t_{L1} , low-to-high transition time t_{DL} , and rise time t_r . The DATA signal is shown as a bus with high level V_H and low level V_L , exhibiting a crossing transition. The DATA ENABLE (MM5450) signal is active-low, with high level V_H and low level V_L . Its timing parameters include setup time t_{DS} before the data transition and hold time t_{DES} after the data transition.

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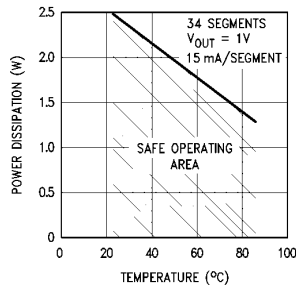
Functional Description (Continued)



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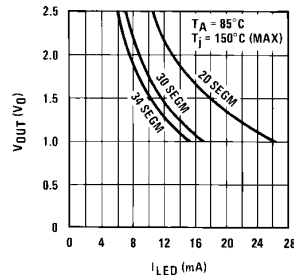
FIGURE 4. Input Data Format

Typical Performance Characteristics



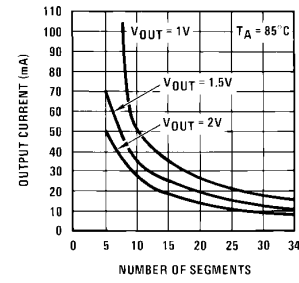
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FIGURE 5



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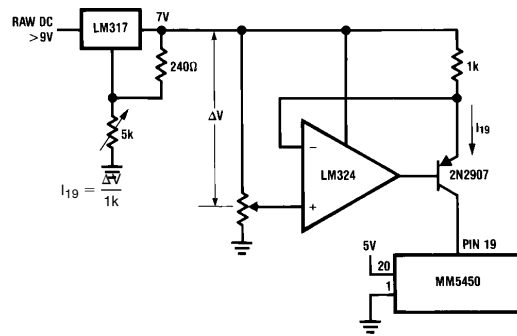
FIGURE 6



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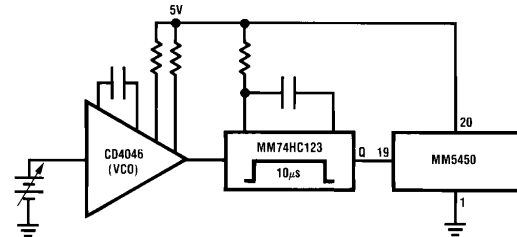
FIGURE 7

Typical Applications



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FIGURE 8. Typical Application of Constant Current Brightness Control

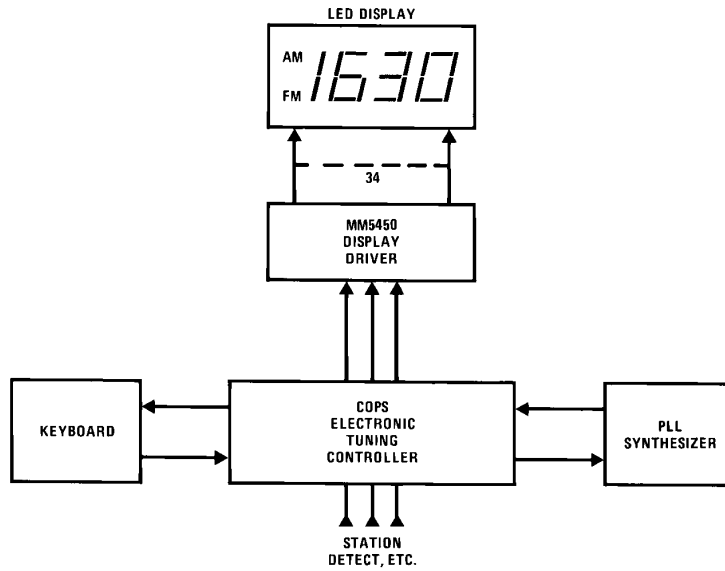


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FIGURE 9. Brightness Control Varying the Duty Cycle

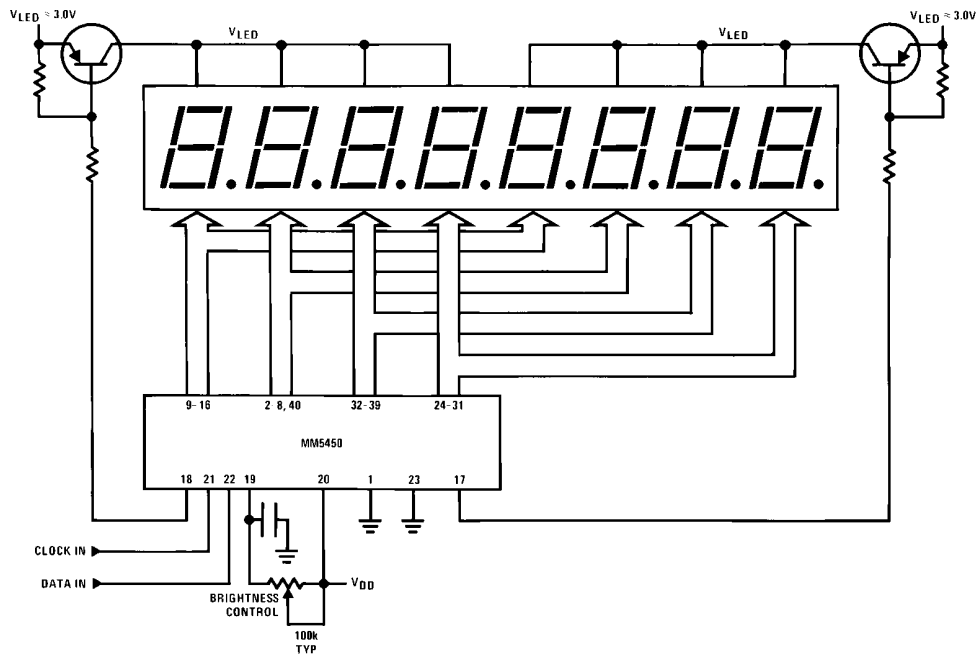
Typical Applications (Continued)

Basic Electronically Tuned Radio System



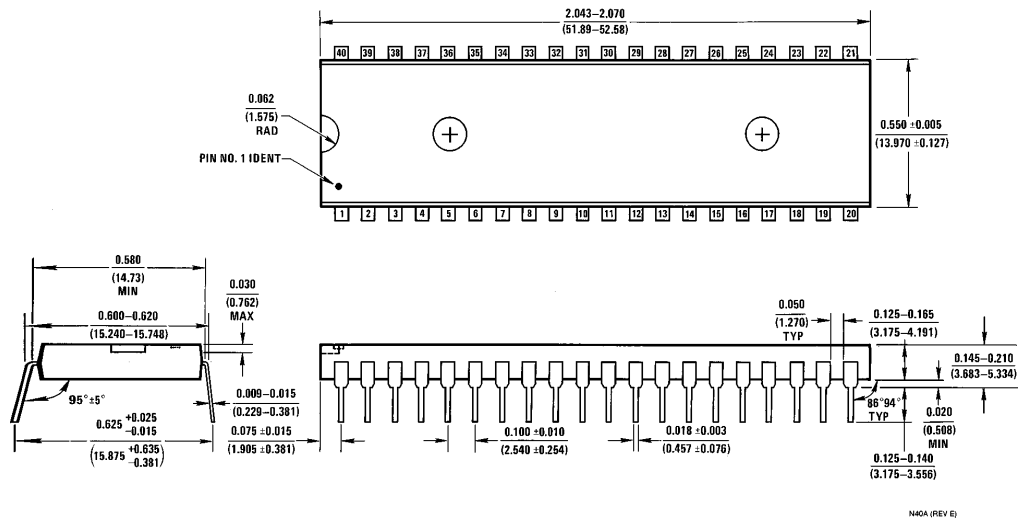
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Duplexing 8 Digits with One MM5450



TL/F/6136-12

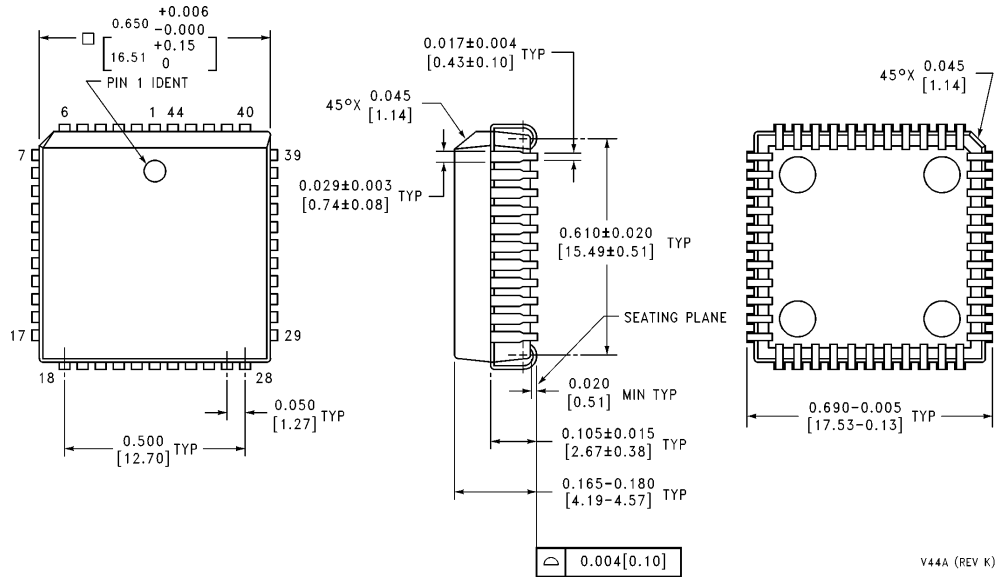
Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number MM5450N or MM5451N
NS Package Number N40A

MM5450/MM5451 LED Display Drivers

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier (V)
Order Number MM5450V or MM5451V
NS Package Number V44A

V44A (REV K)

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