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MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Designer's™ Data Sheet
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

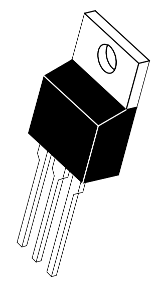
MTP50N06V

Motorola Preferred Device

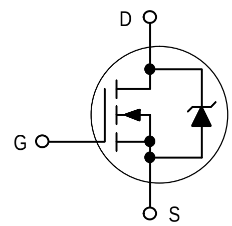
TMOS POWER FET
42 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.028 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

TMOS V™



CASE 221A–06, Style 5
TO–220AB



New Features of TMOS V

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \leq$ 10 ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \leq$ 10 µs)	I_D I_D I_{DM}	42 30 147	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	125 0.83	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 42 Apk, L = 0.454 µH, R_G = 25 Ω)	E_{AS}	400	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

E–FET, Designer's and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 µAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 —	— 69	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	— —	— —	10 100	µAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 µAdc) Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	2.7 3.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 21 Adc)	$R_{DS(on)}$	—	0.025	0.028	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 42 Adc) (I_D = 21 Adc, T_J = 150°C)	$V_{DS(on)}$	— —	1.4 —	1.7 1.6	Vdc
Forward Transconductance (V_{DS} = 6.25 Vdc, I_D = 20 Adc)	g_{FS}	16	23	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1644	2320	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	465	660	pF
Reverse Transfer Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{rss}	—	112	230	pF
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time (V_{DD} = 25 Vdc, I_D = 42 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	20	ns
Rise Time	t_r	—	122	250	ns
Turn–Off Delay Time	$t_{d(off)}$	—	64	110	ns
Fall Time	t_f	—	54	90	ns
Gate Charge (See Figure 8) (V_{DS} = 48 Vdc, I_D = 42 Adc, V_{GS} = 10 Vdc)	Q_T	—	47	70	nC
	Q_1	—	9	—	
	Q_2	—	21	—	
	Q_3	—	16	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (1) (I_S = 42 Adc, V_{GS} = 0 Vdc) (I_S = 42 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	— —	1.06 0.99	2.5 —	Vdc
Reverse Recovery Time (See Figure 14) (I_S = 42 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs)	t_{rr}	—	84	—	ns
	t_a	—	73	—	
	t_b	—	11	—	
Reverse Recovery Stored Charge	Q_{RR}	—	0.28	—	µC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_D	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

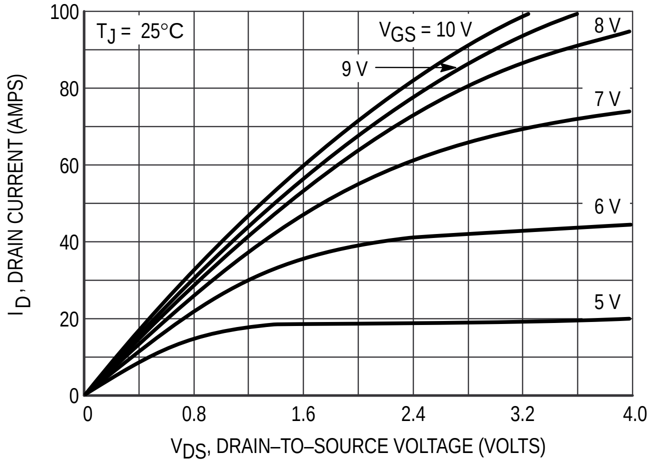


Figure 1. On–Region Characteristics

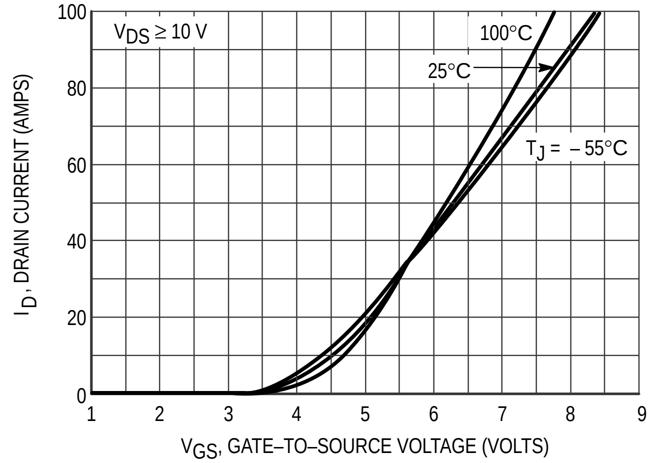


Figure 2. Transfer Characteristics

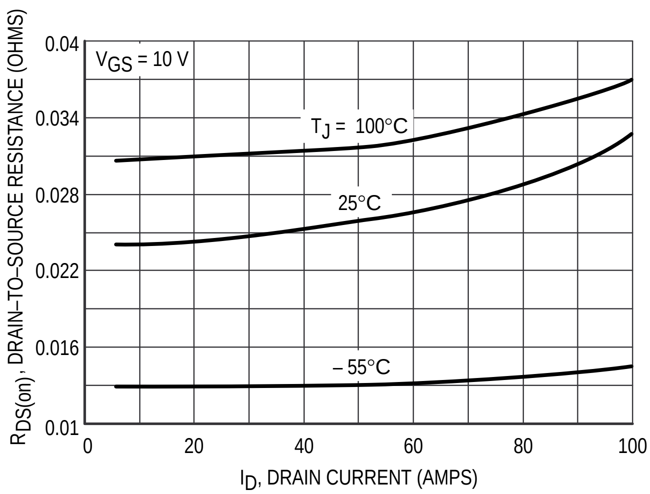


Figure 3. On–Resistance versus Drain Current and Temperature

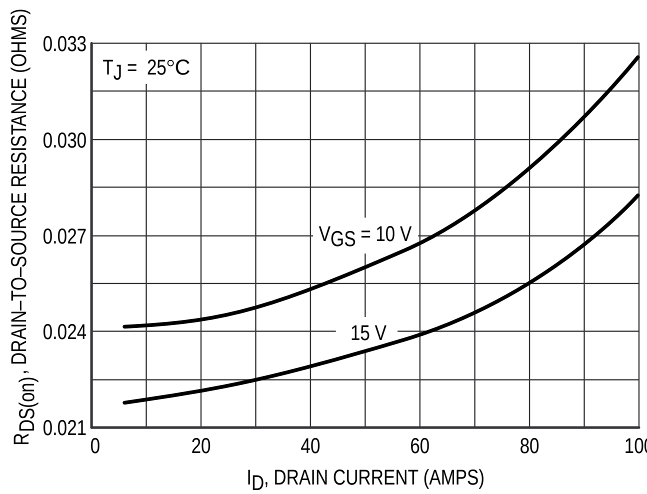


Figure 4. On–Resistance versus Drain Current and Gate Voltage

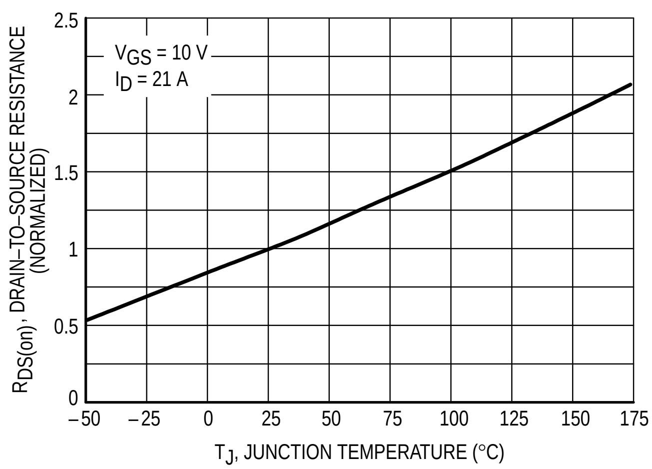


Figure 5. On–Resistance Variation with Temperature

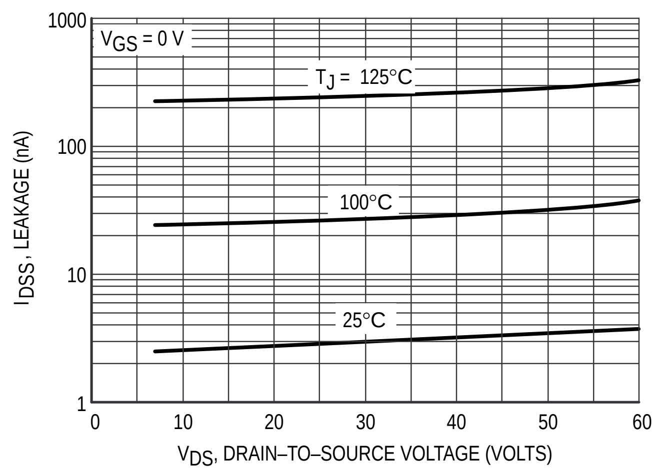


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \ln\, [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\, C_{iss}\, \ln\, (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

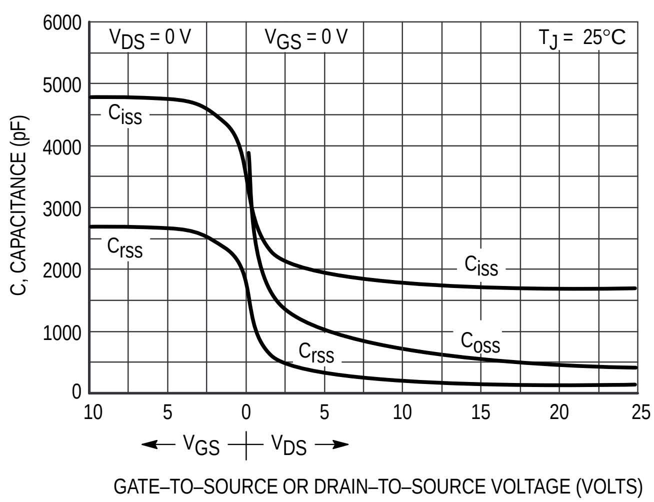


Figure 7. Capacitance Variation

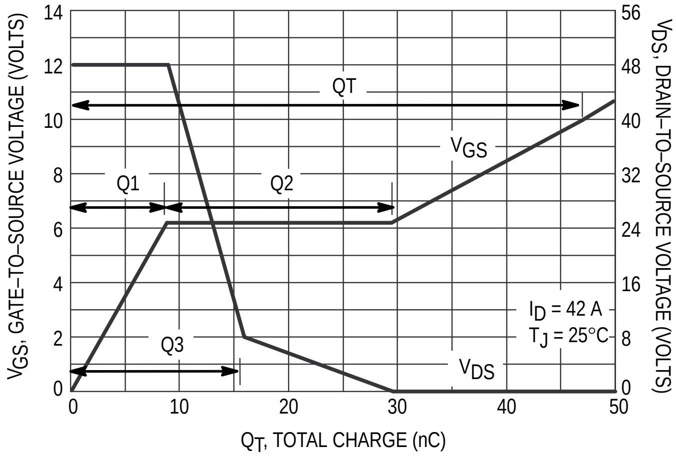


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

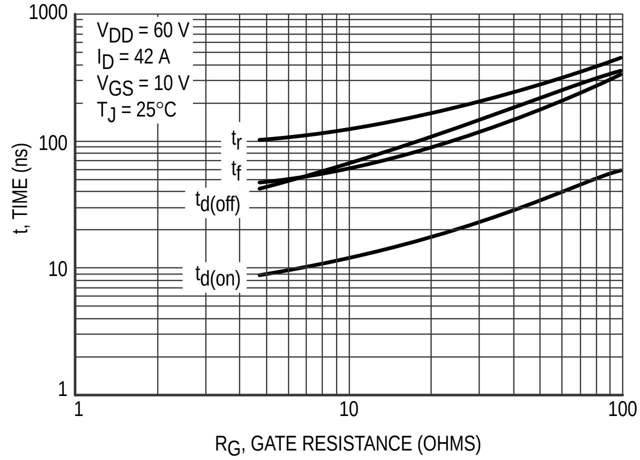


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

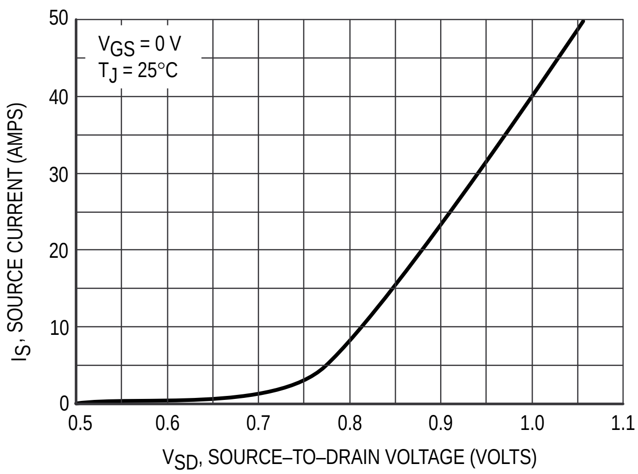


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

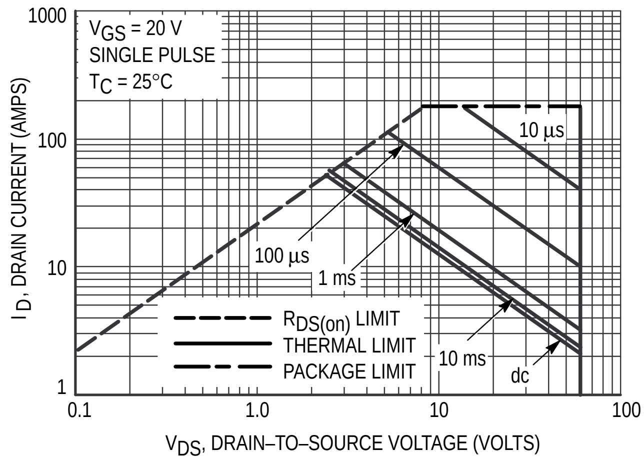


Figure 11. Maximum Rated Forward Biased Safe Operating Area

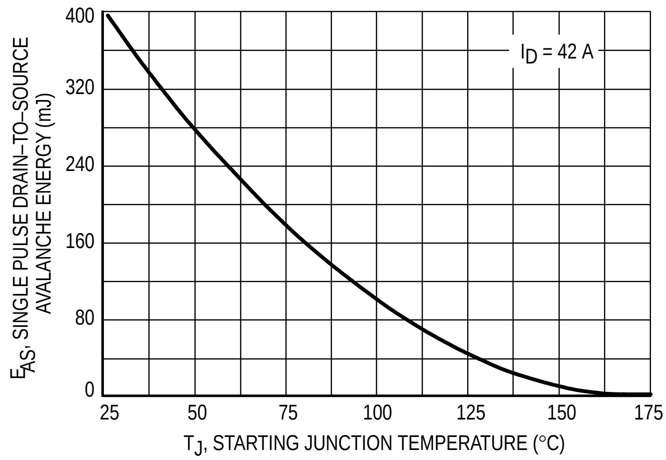


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

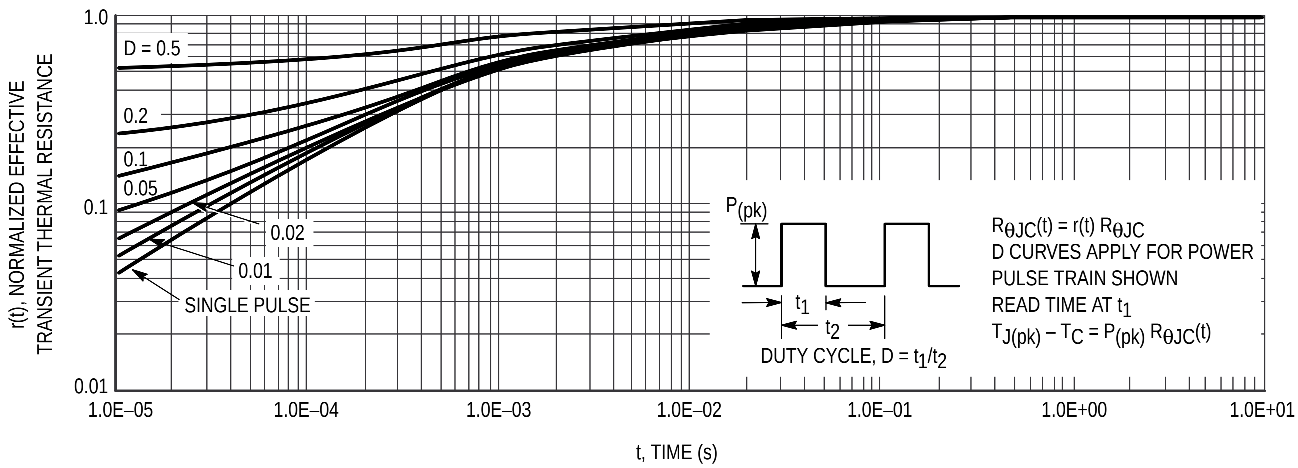


Figure 13. Thermal Response

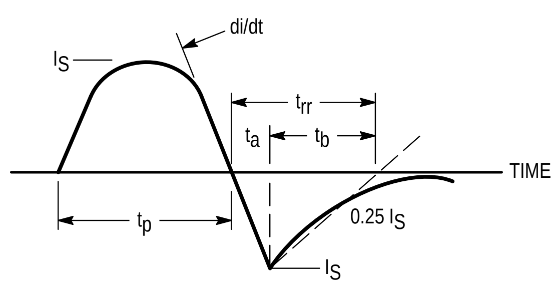
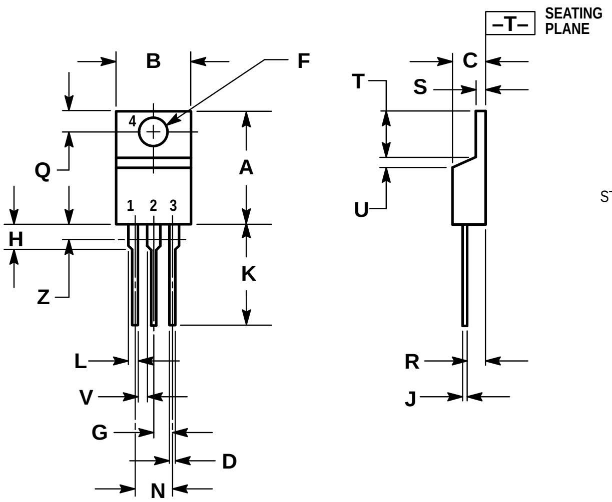


Figure 14. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A–06
ISSUE Y

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