NE555
# SA555 - SE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER^{o}C

DESCRIPTION
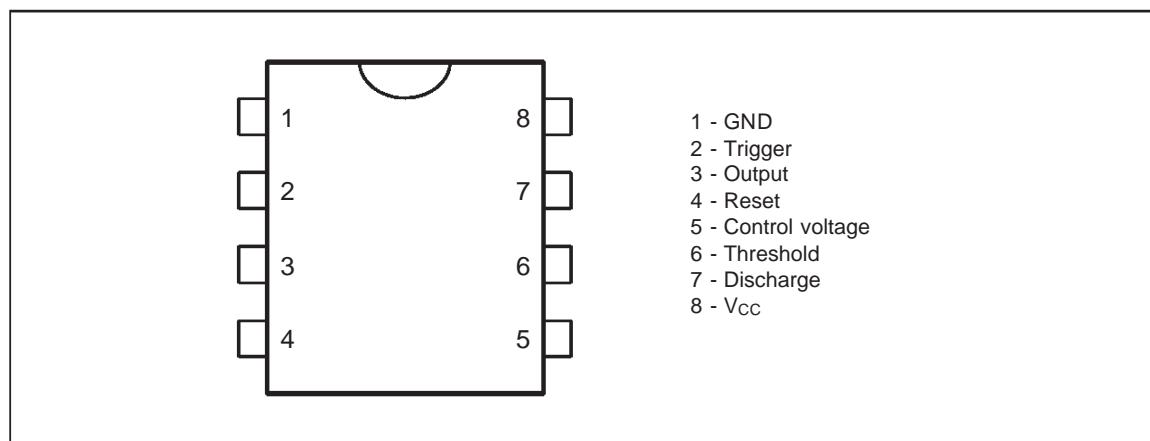
The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.


N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

ORDER CODES
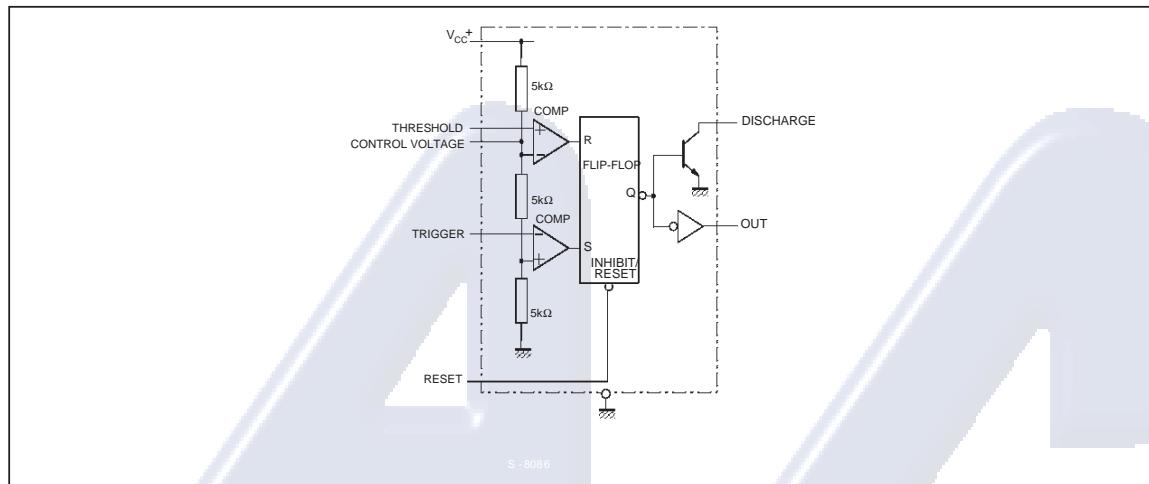
Part Number	Temperature Range	Package	
		N	**D**
NE555	0°C, 70°C	•	•
SA555	–40°C, 105°C	•	•
SE555	–55°C, 125°C	•	•

PIN CONNECTIONS (top view)

1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V$_{CC}$
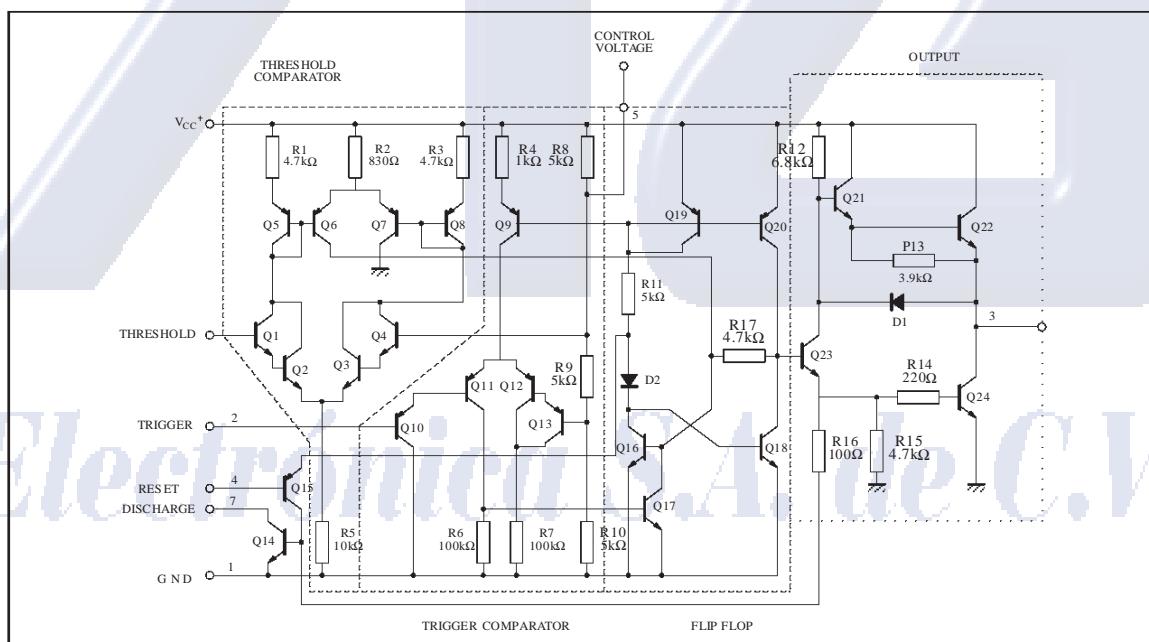
NE555/SA555/SE555

BLOCK DIAGRAM

SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{cc}	Supply Voltage		18	V
T_{oper}	Operating Free Air Temperature Range	for NE555 for SA555 for SE555	0 to 70 −40 to 105 −55 to 125	°C
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		−65 to 150	°C

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OPERATING CONDITIONS

Symbol	Parameter	SE555	NE555 - SA555	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

ELECTRICAL CHARACTERISTICS

$T_{amb} = +25^{o}C$, $V_{CC} = +5V$ to $+15V$ (unless otherwise specified)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current ($R_L \infty$) (- note 1) Low State $V_{CC} = +5V$ $V_{CC} = +15V$ High State $V_{CC} = 5V$		3 10 2	5 12		3 10 2	6 15	mA
	Timing Error (monostable) ($R_{A} = 2k$ to $100k\Omega$, $C = 0.1\mu F$) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		0.5 30 0.05	2 100 0.2		1 50 0.1	3 0.5	% ppm/°C %/V
	Timing Error (astable) (R_A, $R_B = 1k\Omega$ to $100k\Omega$, $C = 0.1\mu F$, $V_{CC} = +15V$) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		1.5 90 0.15			2.25 150 0.3		% ppm/°C %/V

V_{CL}	Control Voltage level
	           $V_{CC} = +15V$
	           $V_{CC} = +5V$
		9.6
		2.9
			10
			3.33
				10.4
				3.8
					9
					2.6
						10
						3.33
							11
							4
								V

V_{th}	Threshold Voltage
	           $V_{CC} = +15V$
	           $V_{CC} = +5V$
		9.4
		2.7
			10
			3.33
				10.6
				4
					8.8
					2.4
						10
						3.33
							11.2
							4.2
								V

I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA

V_{trig}	Trigger Voltage
	           $V_{CC} = +15V$
	           $V_{CC} = +5V$
		4.8
		1.45
			5
			1.67
				5.2
				1.9
					4.5
					1.1
						5
						1.67
							5.6
							2.2
								V

I_{trig}	Trigger Current ($V_{trig} = 0V$)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V

I_{reset}	Reset Current
	           $V_{reset} = +0.4V$
	           $V_{reset} = 0V$
			0.1
			0.4
				0.4
				1
						0.1
						0.4
							0.4
							1.5
								mA

V_{OL}	Low Level Output Voltage
	$V_{CC} = +15V$, $I_{O(sink)} = 10mA$
	                $I_{O(sink)} = 50mA$
	                $I_{O(sink)} = 100mA$
	                $I_{O(sink)} = 200mA$
	$V_{CC} = +5V$, $I_{O(sink)} = 8mA$
	                $I_{O(sink)} = 5mA$
			0.1
			0.4
			2
			2.5
			0.1
			0.05
				0.15
				0.5
				2.2
				
				0.25
				0.2
						0.1
						0.4
						2
						2.5
						0.3
						0.25
							0.25
							0.75
							2.5
							
							0.4
							0.35
								V

V_{OH}	High Level Output Voltage $V_{CC} = +15V$, $I_{O(source)} = 200mA$ $I_{O(source)} = 100mA$ $V_{CC} = +5V$, $I_{O(source)} = 100mA$	 13 3	12.5 13.3 3.3		 12.75 2.75	12.5 13.3 3.3		V

Notes :   1. Supply current when output is high is typically 1mA less.
          2. Tested at $V_{CC} = +5V$ and $V_{CC} = +15V$.
          3. This will determine the maximum value of $R_A + R_B$ for +15V operation the max total is $R = 20M\Omega$ and for 5V operation the max total $R = 3.5M\Omega$.

NE555/SA555/SE555

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis\,(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		180 80	480 200		180 80	480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering
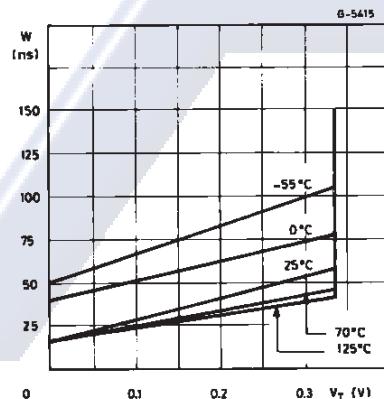
Figure 2 : Supply Current versus Supply Voltage
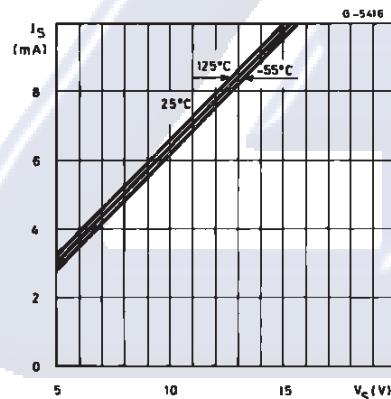
Figure 3 : Delay Time versus Temperature
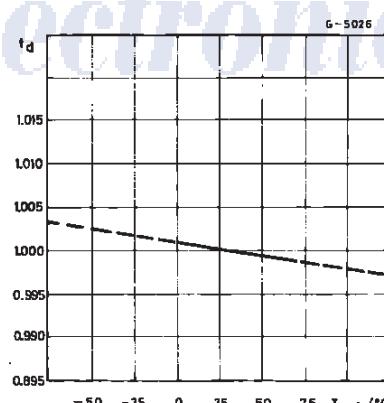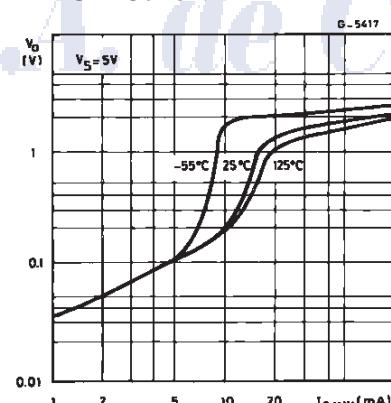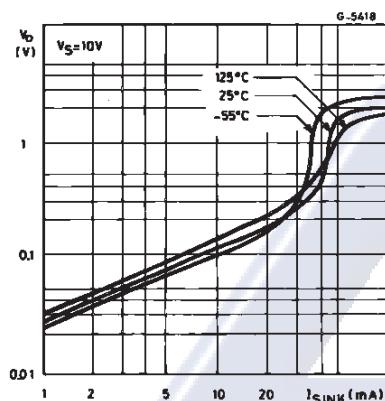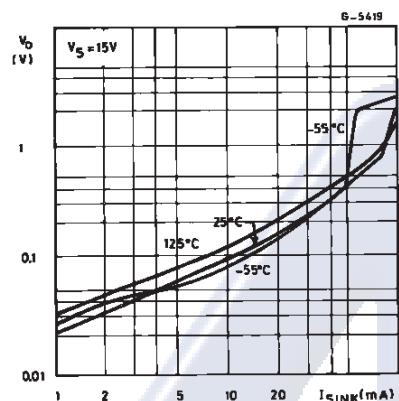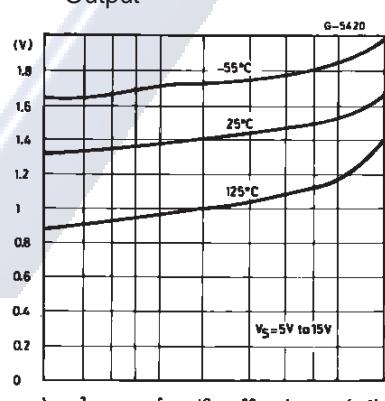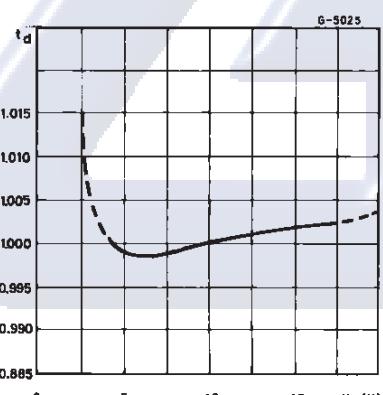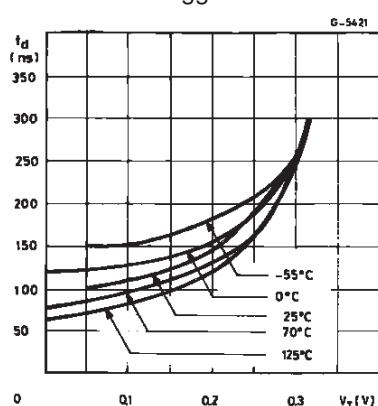
Figure 4 : Low Output Voltage versus Output Sink Current

Figure 5 : Low Output Voltage versus Output Sink Current


Figure 6 : Low Output Voltage versus Output Sink Current


Figure 7 : High Output Voltage Drop versus Output

**Figure 8 :** Delay Time versus Supply Voltage

**Figure 9 :** Propagation Delay versus Voltage Level of Trigger Value
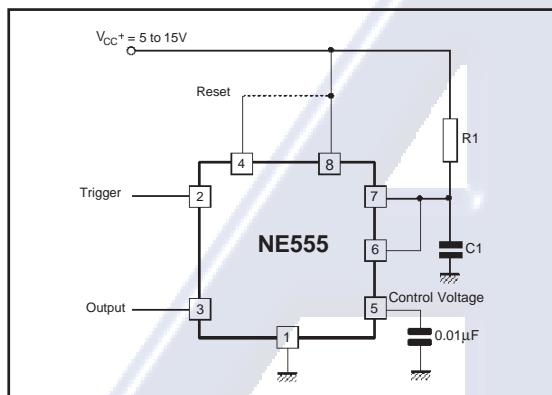
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APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 10

The circuit triggers on a negative-going input signal when the level reaches $1/3$ Vcc. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1 C_1$ and is easily determined by figure 12.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1 C_1$. When the voltage across the capacitor equals $2/3\ V_{cc}$, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11

t = 0.1 ms / div
INPUT = 2.0V/div
OUTPUT VOLTAGE = 5.0V/div
CAPACITOR VOLTAGE = 2.0V/div
$R1 = 9.1k\Omega$, $C1 = 0.01\mu F$, $R_L = 1k\Omega$
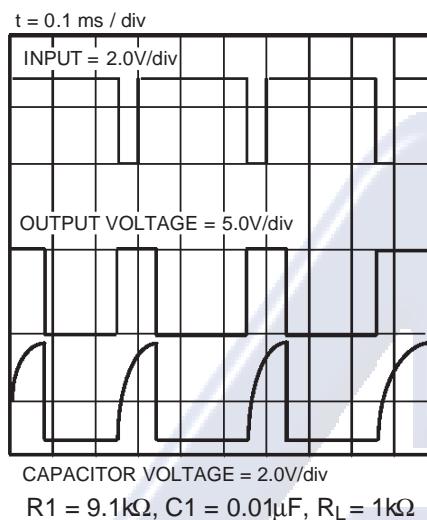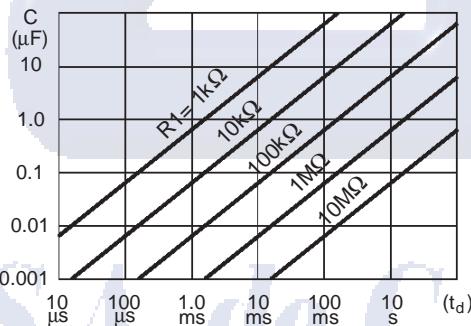
Figure 12

ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between $1/3\ V_{cc}$ and $2/3$ Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.
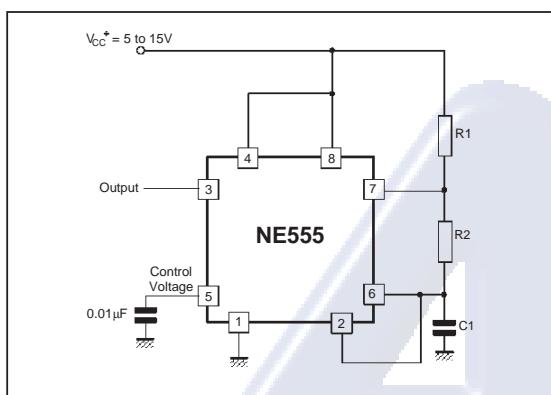
Figure 13

Figure 14 shows actual waveforms generated in this mode of operation.
The charge time (output HIGH) is given by :
$t_1 = 0.693 (R_1 + R_2) C_1$
and the discharge time (output LOW) by :
$t_2 = 0.693 (R_2) C_1$
Thus the total period T is given by :
$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$
The frequency of oscillation is them :
$f = \dfrac{1}{T} = \dfrac{1.44}{(R_1 + 2R_2) C_1}$
and may be easily found by figure 15.
The duty cycle is given by :
$D = \dfrac{R_2}{R_1 + 2R_2}$
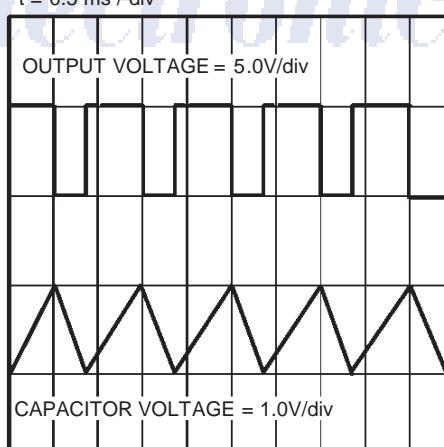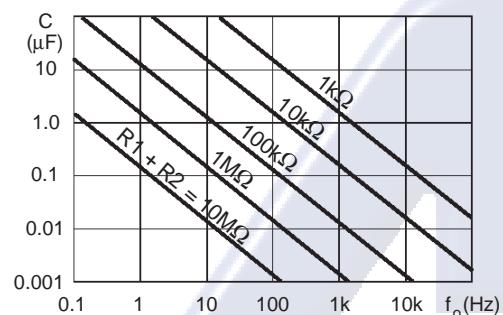
Figure 14
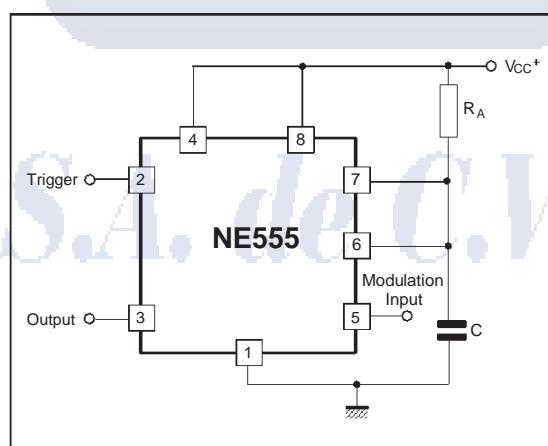
$R1 = R2 = 4.8k\Omega$, $C1 = 0.1\mu F$, $R_L = 1k\Omega$

Figure 15 : Free Running Frequency versus R_1, R_2 and C_1

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.

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LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.
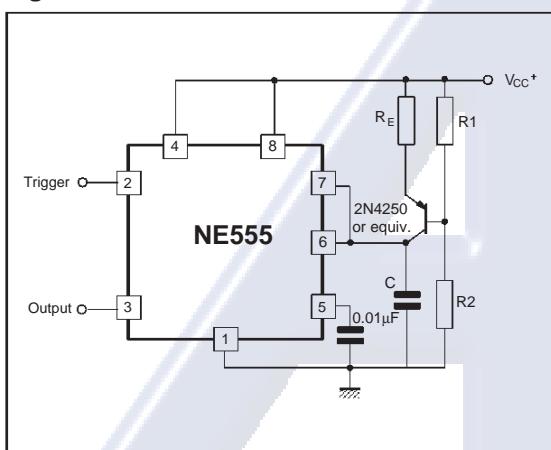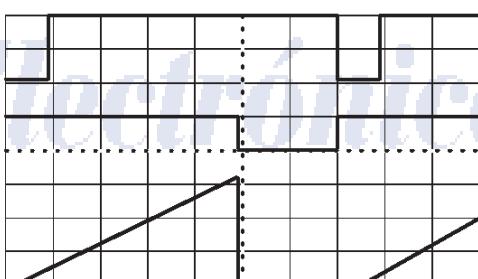
Figure 18 shows waveforms generator by the linear ramp.
The time interval is given by :

$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_{1+}\ R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_{1+}\ R_2)}\ V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.

$V_{CC} = 5V$
Time $= 20\mu s/DIV$
$R_1 = 47k\Omega$
$R_2 = 100k\Omega$
$R_E = 2.7k\Omega$
$C = 0.01\mu F$

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage
1V/DIV

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle the resistors R_A and R_E may be connected as in figure 19. The time preriod for the output high is the same as previous,
$t_1 = 0.693\ R_A\ C$.
For the output low it is $t_2 =$
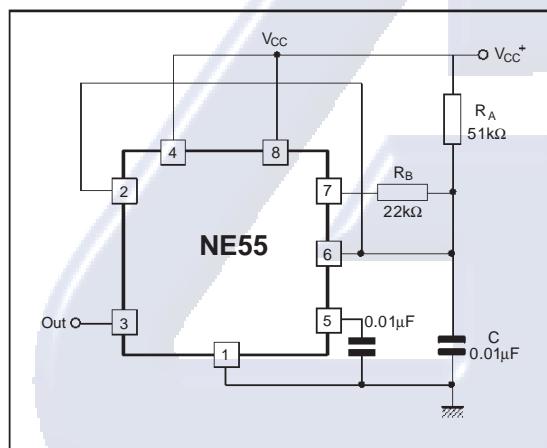
$$[(R_A R_B)/(R_A + R_B)]\ CLn\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \dfrac{1}{t_1 + t_2}$

Note that this circuit will not oscillate if R_B is greater

**Figure 19 :** 50% Duty Cycle Oscillator.
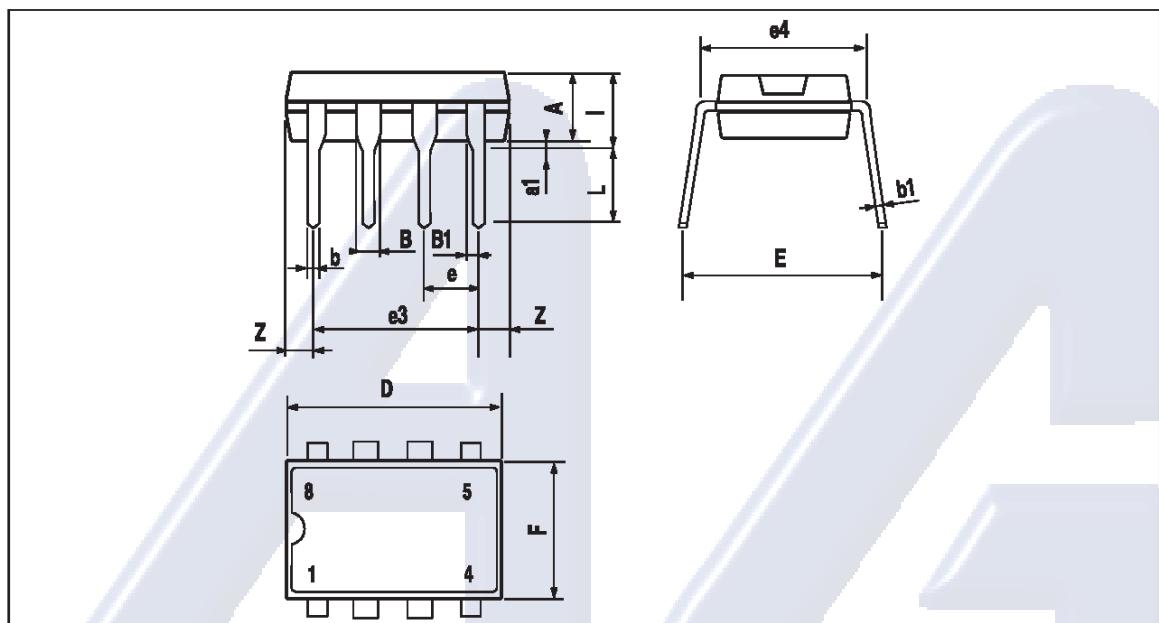
than $1/2\ R_A$ because the junction of R_A and R_B cannot bring pin 2 down to $1/3\ V_{CC}$ and trigger the lower comparator.

ADDITIONAL INFORMATION
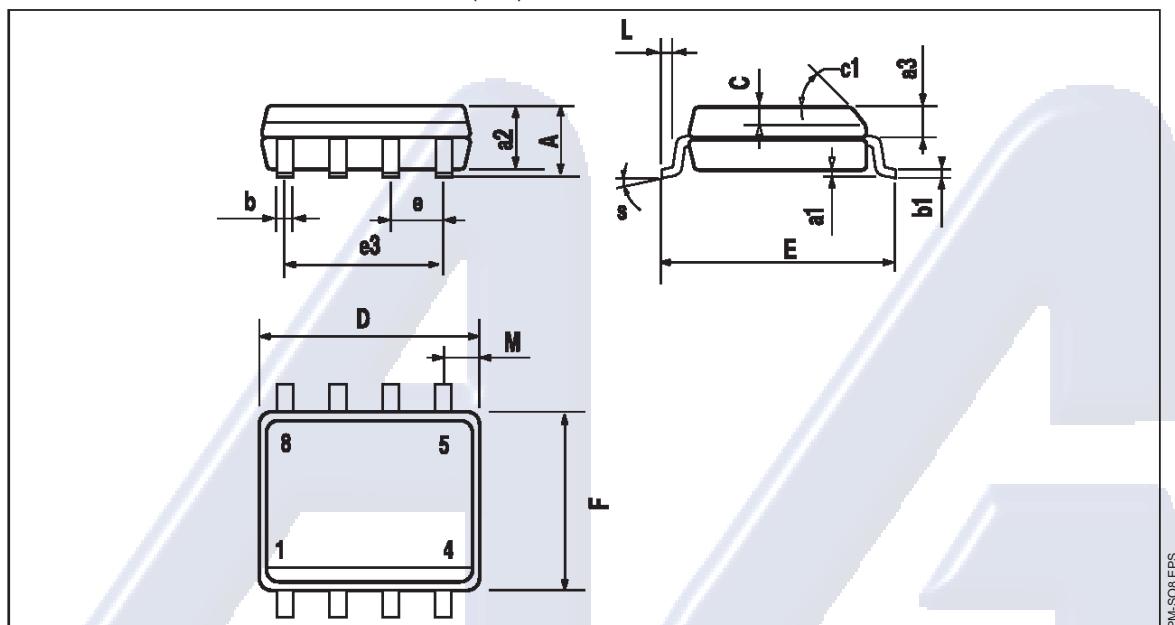
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is $0.1\mu F$ in parallel with $1\mu F$ electrolytic.

**NE555/SA555/SE555**

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

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PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					