

NTE5437 & NTE5438

Silicon Controlled Rectifier (SCR)

8 Amp

Description:

The NTE5437 and NTE5438 are silicon controlled rectifiers (SCR) in a TO220 type package designed for general purpose high voltage applications where gate sensitivity is required.

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Repetitive Peak Off-State Voltage ($T_J = -40^\circ$ to $+125^\circ\text{C}$, $R_{GK} = 1\text{k}\Omega$), V_{DRM} , V_{RRM}	
NTE5437	400V
NTE5438	600V
On-State Current (All Conducting Angles, $T_C = +85^\circ\text{C}$), $I_{T(RMS)}$	
8A	
Average On-State Current (Half Cycle, $\Theta = 180^\circ$, $T_C = +85^\circ\text{C}$), $I_{T(AV)}$	
5.1A	
Non-Repetitive On-State Current, I_{TSM}	
Half Cycle, 60Hz	88A
Half Cycle, 50Hz	80A
Fusing Current ($t = 10\text{ms}$, Half Cycle), I^2t	
32A ² s	
Peak Reverse Gate Voltage ($I_{GR} = 50\mu\text{A}$), V_{GRM}	
8V	
Peak Gate Current (10 μs Max), I_{GM}	
2A	
Peak Gate Dissipation (10 μs Max), P_{GM}	
5W	
Gate Dissipation (20ms Max), $P_{G(AV)}$	
0.5W	
Operating Junction Temperature Range, T_J	
-40° to $+125^\circ\text{C}$	
Storage Temperature Range, T_{stg}	
-40° to $+125^\circ\text{C}$	
Lead Temperature (During Soldering, 1.6mm from case, 10sec Max), T_L	
$+250^\circ\text{C}$	
Thermal Resistance, Junction-to-Case, R_{thJC}	
4K/W	
Thermal Resistance, Junction-to-Ambient, R_{thJA}	
60K/W	

Electrical Characteristics: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Off-State Leakage Current	I_{DRM} , I_{RRM}	$V_{DRM} + V_{RRM} = \text{Rated Voltage,}$ $R_{GK} = 1\text{k}\Omega$	$T_J = +125^\circ\text{C}$	–	0.5	mA
			$T_J = +25^\circ\text{C}$	–	5.0	μA

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
On-State Voltage	V_T	$I_T = 16\text{A}$, $T_J = +25^{\circ}\text{C}$	–	1.95	V
On-State Threshold Voltage	$V_{T(TO)}$	$T_J = +125^{\circ}\text{C}$	–	1.05	V
On-State Slope Resistance	r_T	$T_J = +125^{\circ}\text{C}$	–	65	$\text{m}\Omega$
Gate Trigger Current	I_{GT}	$V_D = 7\text{V}$	–	200	μA
Gate Trigger Voltage	V_{GT}	$V_D = 7\text{V}$	–	2.0	V
Holding Current	I_H	$R_{GK} = 1\text{k}\Omega$	–	10	mA
Latching Current	I_L	$R_{GK} = 1\text{k}\Omega$	–	20	mA
Critical Rate of Voltage Rise	dv/dt	$V_D = .67 \times V_{DRM}$, $R_{GK} = 1\text{k}\Omega$, $T_J = +125^{\circ}\text{C}$	5	–	$\text{V}/\mu\text{s}$
Critical Rate of Current Rise	di/dt	$I_G = 10\text{mA}$, $di_G/dt = 0.1\text{A}/\mu\text{s}$, $T_J = +125^{\circ}\text{C}$	100	–	$\text{A}/\mu\text{s}$
Gate Controlled Delay Time	t_{gd}	$I_G = 10\text{mA}$, $di_G/dt = 0.1\text{A}/\mu\text{s}$	–	500	ns
Commutated Turn-Off Time	t_q	$T_C = +85^{\circ}\text{C}$, $V_D = .67 \times V_{DRM}$, $V_R = 35\text{V}$, $I_T = 5.1\text{A}$	–	100	μs

