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## NTE5498 & NTE5499 Silicon Controlled Rectifier (SCR) 12 Amp

**Description:**

The NTE5498 and NTE5499 silicon controlled rectifiers are high performance glass passivated PNP devices in a TO220 type package designed for general purpose high current applications where moderate gate sensitivity is required.

**Absolute Maximum Ratings:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Peak Repetitive Off-State Voltage ( $T_J = -40^\circ$ to $+125^\circ\text{C}$ , $R_{GK} = 1\text{k}\Omega$ ), $V_{DRM}$ , $V_{RRM}$	400V
NTE5498 .....	400V
NTE5499 .....	800V
RMS On-State Current (All Conduction Angles, $T_C = +85^\circ\text{C}$ ), $I_{T(RMS)}$	12A
Average On-State Current (Half Cycle, $180^\circ$ Conduction Angle, $T_C = +85^\circ\text{C}$ ), $I_{T(AV)}$	7.6A
Non-Repetitive On-State Current (Half Cycle, 60Hz), $I_{TSM}$	132A
Non-Repetitive On-State Current (Half Cycle, 50Hz), $I_{TSM}$	120A
Circuit Fusing Considerations (Half Cycle, $t = 10\text{ms}$ ), $I^2t$	72A <sup>2</sup> s
Peak Gate Current (10 $\mu\text{s}$ Max), $I_{GM}$	4A
Peak Gate Dissipation (10 $\mu\text{s}$ Max), $P_{GM}$	10W
Average Gate Dissipation (20ms Max), $P_{G(AV)}$	1W
Operating Junction Temperature Range, $T_J$	$-40^\circ$ to $+125^\circ\text{C}$
Storage Temperature Range, $T_{stg}$	$-40^\circ$ to $+125^\circ\text{C}$
Thermal Resistance, Junction-to-Case, $R_{thJC}$	3K/W
Thermal Resistance, Junction-to-Ambient, $R_{thJA}$	60K/W
Lead Temperature (During Soldering, 1.6mm from case, 10sec max), $T_L$	$+250^\circ\text{C}$

**Electrical Characteristics:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Off-State Leakage Current	$I_{DRM}$ , $I_{RRM}$	$V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{k}\Omega$	$T_J = +125^\circ\text{C}$	–	–	1.5	mA
			$T_J = +25^\circ\text{C}$	–	–	5.0	$\mu\text{A}$
On-State Voltage	$V_T$	$I_T = 24\text{A}$ , $T_J = +25^\circ\text{C}$	–	–	1.8	V	
On-State Threshold Voltage	$V_{T(TO)}$	$T_J = +125^\circ\text{C}$	–	–	1.0	V	
On-State Slope Resistance	$r_T$	$T_J = +125^\circ\text{C}$	–	–	36	$\text{m}\Omega$	
Gate-Trigger Current	$I_{GT}$	$V_D = 7\text{V}$	5	–	10	mA	
Gate-Trigger Voltage	$V_{GT}$	$V_D = 7\text{V}$	–	–	2.0	V	

**Electrical Characteristics (Cont'd):** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Holding Current	$I_H$	$R_{GK} = 1\text{k}\Omega$	-	-	40	mA
Latching Current	$I_L$	$R_{GK} = 1\text{k}\Omega$	-	-	30	mA
Critical Rate of Voltage Rise	$dv/dt$	$V_D = .67 \times V_{DRM}$ , $R_{GK} = 1\text{k}\Omega$ , $T_J = +125^\circ\text{C}$	100	-	-	V/ $\mu\text{s}$
Critical Rate of Current Rise	$di/dt$	$I_G = 50\text{mA}$ , $di_G/dt = 0.5\text{A}/\mu\text{s}$ , $T_J = +125^\circ\text{C}$	100	-	-	A/ $\mu\text{s}$
Gate Controlled Delay Time	$t_{gd}$	$I_G = 50\text{mA}$ , $di_G/dt = 0.5\text{A}/\mu\text{s}$	-	-	500	ns
Commutated Turn-Off Time	$t_q$	$V_D = .67 \times V_{DRM}$ , $V_R = 35\text{V}$ , $I_T = I_{T(AV)}$ , $T_C = +85^\circ\text{C}$	-	-	50	$\mu\text{s}$

