# NVMFD5C478NL

## Power MOSFET
### 40 V, 14.5 mΩ, 29 A, Dual N−Channel

**Features**

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5C478NLWF – Wettable Flanks Product
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 40 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4) | Steady State | $T_C$ = 25°C | $I_D$ | 29 | A |
| | | $T_C$ = 100°C | | 20.6 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3) | | $T_C$ = 25°C | $P_D$ | 23 | W |
| | | $T_C$ = 100°C | | 12 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4) | Steady State | $T_A$ = 25°C | $I_D$ | 10.5 | A |
| | | $T_A$ = 100°C | | 7.5 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3) | | $T_A$ = 25°C | $P_D$ | 3.1 | W |
| | | $T_A$ = 100°C | | 1.5 | |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 98 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | −55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 19 | A |
| Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 1.4 A) | | | $E_{AS}$ | 48 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case – Steady State (Note 3) | $R_{\theta JC}$ | 6.4 | °C/W |
| Junction−to−Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 48.8 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.
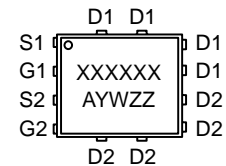
## ON Semiconductor®

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| 40 V | 14.5 mΩ @ 10 V | 29 A |
| | 25 mΩ @ 4.5 V | |

**Dual−Channel**
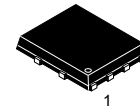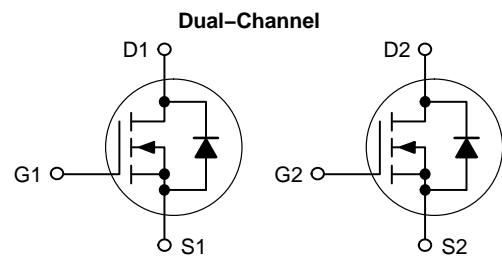


**DFN8, 5x6 (S08FL) CASE 506BT**

**MARKING AND PIN CONNECTION DIAGRAM**



XXXXXX = 5C478L (NVMFD5C478NL) or 478LWF (NVMFD5C478NLWF)
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 40 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V | $T_J$ = 25°C | | | 10 | μA |
| | | | $T_J$ = 125°C | | | 250 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | | 100 | nA |
| **ON CHARACTERISTICS** (Note 5) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 20 μA | | 1.2 | | 2.2 | V |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 7.5 A | | | 12.1 | 14.5 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 7.5 A | | | 20 | 25 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 15 V, $I_D$ = 15 A | | | 25 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 25 V | | | 420 | | pF |
| Output Capacitance | $C_{oss}$ | | | | 185 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 9 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 7.5 A | | | 8.1 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.0 | | nC |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 1.7 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 1.2 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 32 V, $I_D$ = 7.5 A | | | 3.9 | | nC |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 7.5 A, $R_G$ = 1 Ω | | | 6 | | ns |
| Rise Time | $t_r$ | | | | 14 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 18 | | |
| Fall Time | $t_f$ | | | | 3.5 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 7.5 A | $T_J$ = 25°C | | 0.84 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.72 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_S$/dt = 100 A/μs, $I_S$ = 7.5 A | | | 17 | | ns |
| Charge Time | $t_a$ | | | | 7.0 | | |
| Discharge Time | $t_b$ | | | | 10 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 6 | | nC |

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

# NVMFD5C478NL

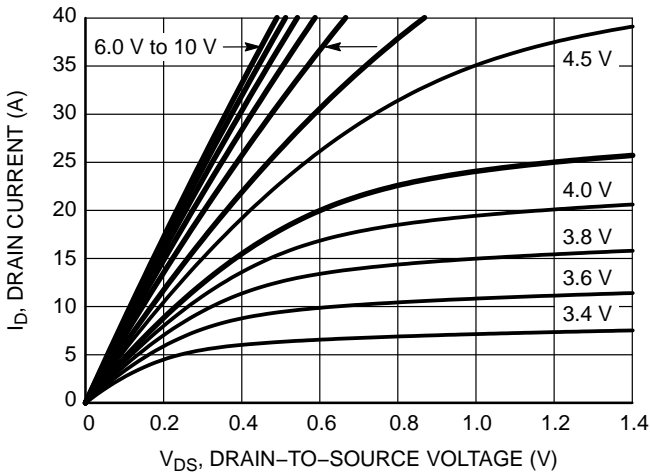## TYPICAL CHARACTERISTICS



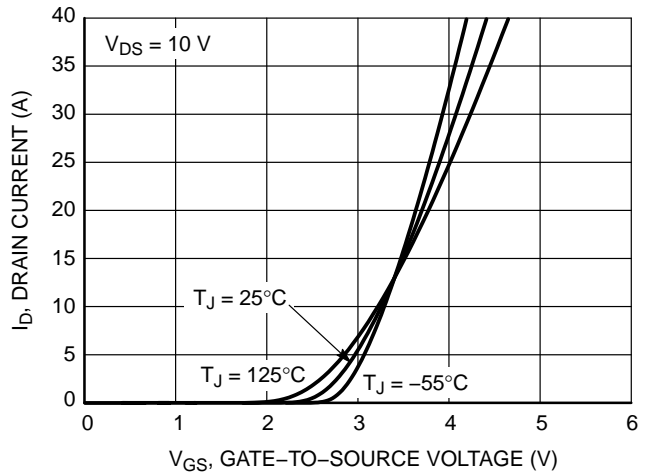Figure 1. On−Region Characteristics
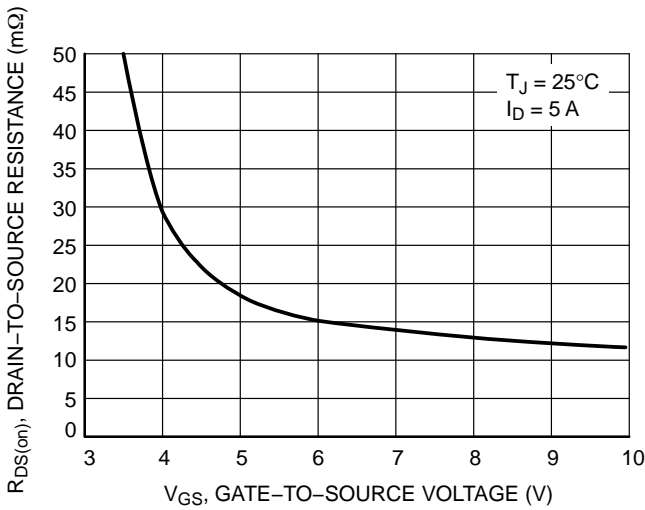


Figure 2. Transfer Characteristics



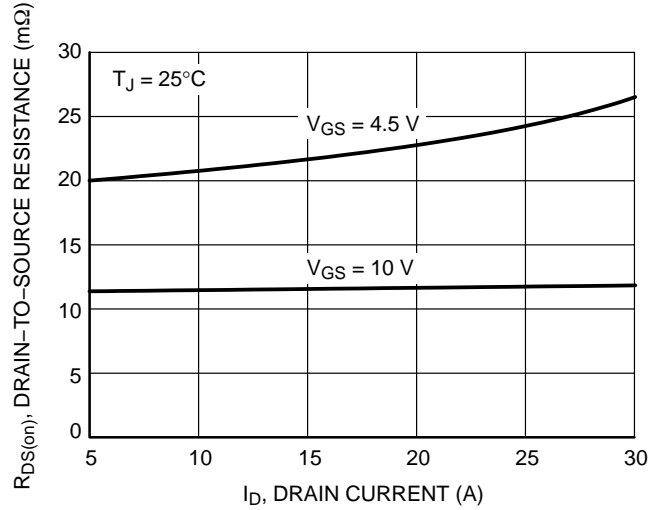Figure 3. On−Resistance vs. Gate−to−Source Voltage



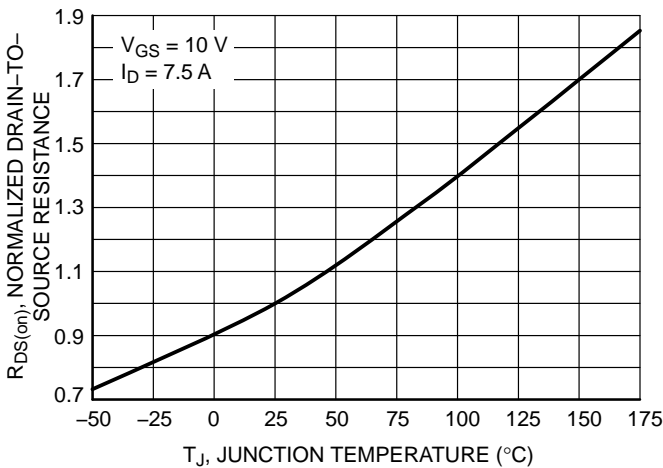Figure 4. On−Resistance vs. Drain Current and Gate Voltage
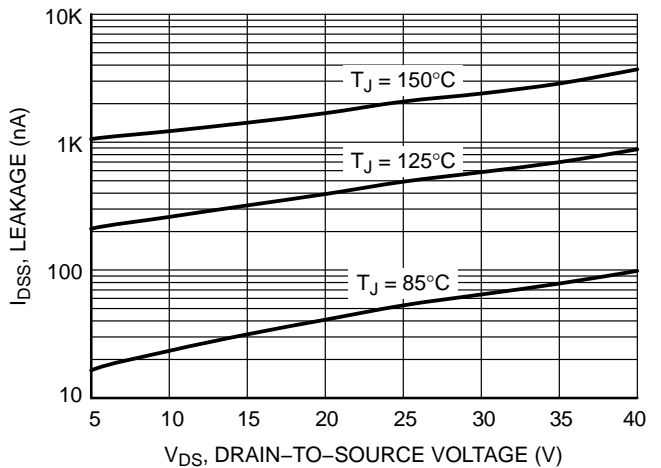


Figure 5. On−Resistance Variation with Temperature



Figure 6. Drain−to−Source Leakage Current vs. Voltage

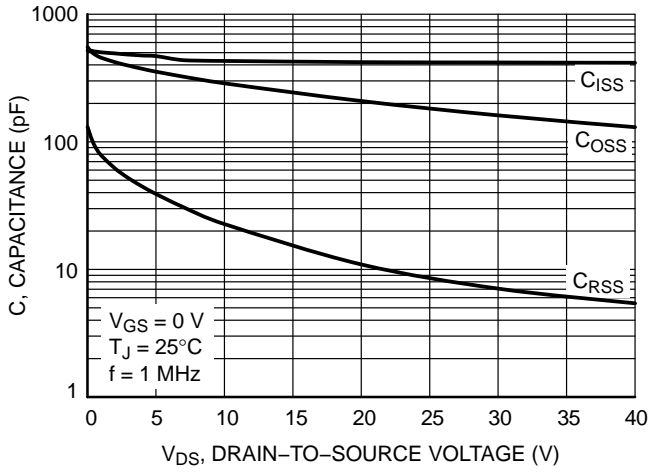# NVMFD5C478NL

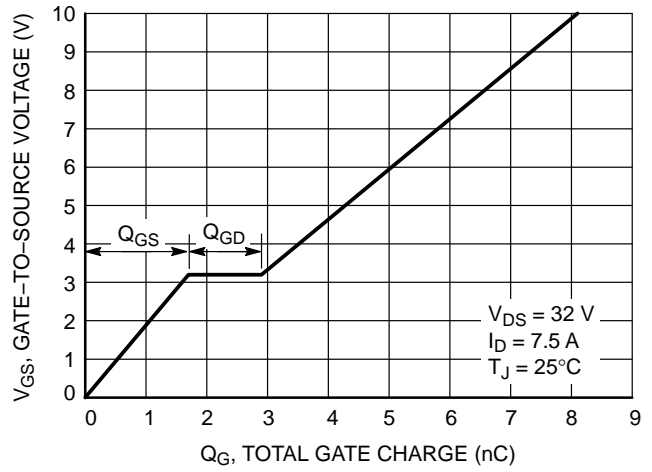## TYPICAL CHARACTERISTICS



**Figure 7. Capacitance Variation**
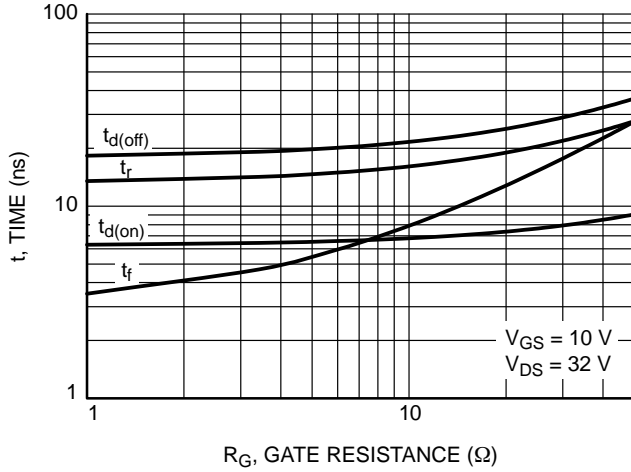


**Figure 8. Gate−to−Source Voltage vs. Total Charge**



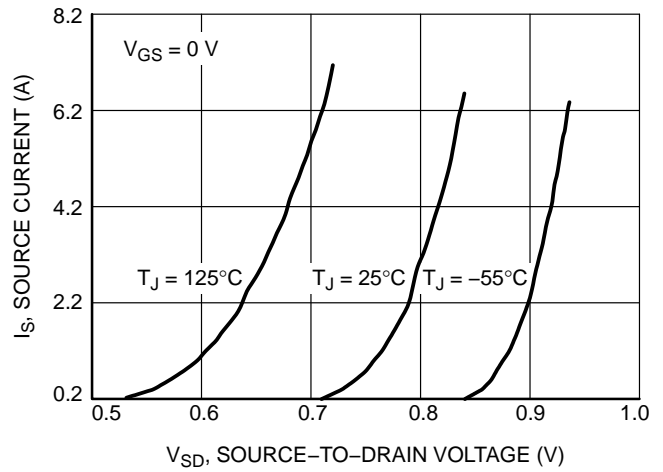**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



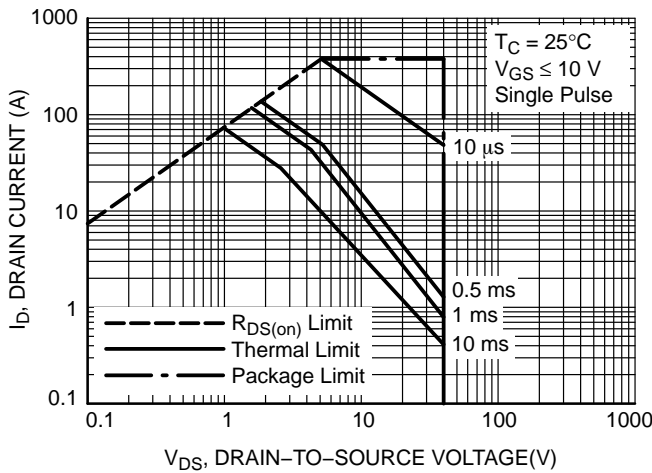**Figure 10. Diode Forward Voltage vs. Current**



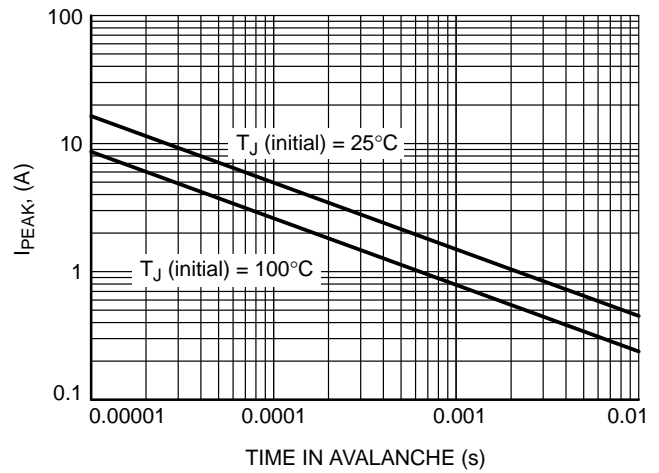**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. I$_{PEAK}$ vs. Time in Avalanche**
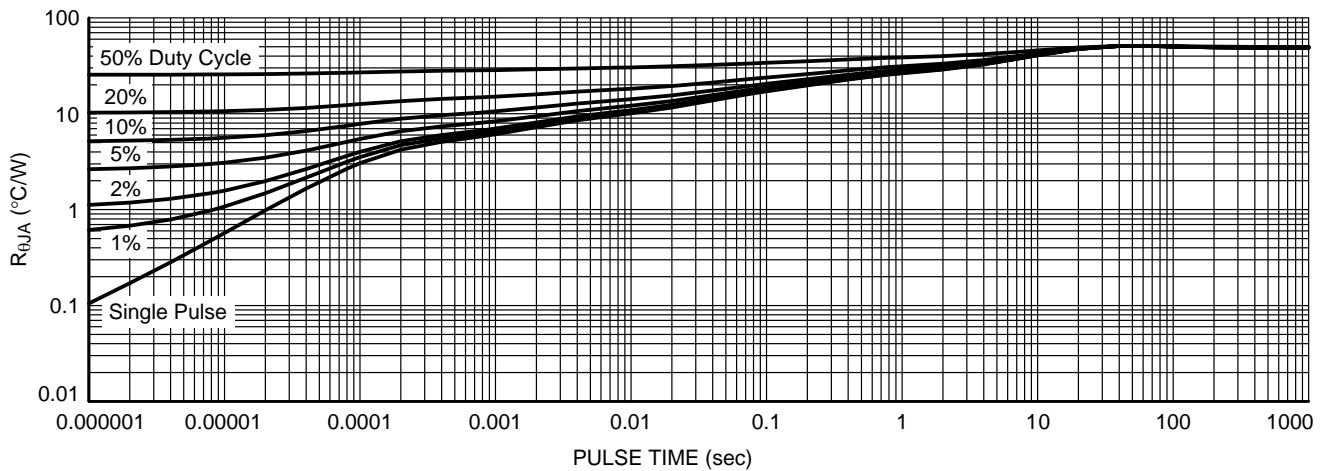
# NVMFD5C478NL

## TYPICAL CHARACTERISTICS



**Figure 13. Thermal Characteristics**
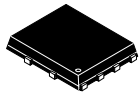
## DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| NVMFD5C478NLT1G | 5C478L | DFN8 (Pb–Free) | 1500 / Tape & Reel |
| NVMFD5C478NLWFT1G | 478LWF | DFN8 (Pb–Free) | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
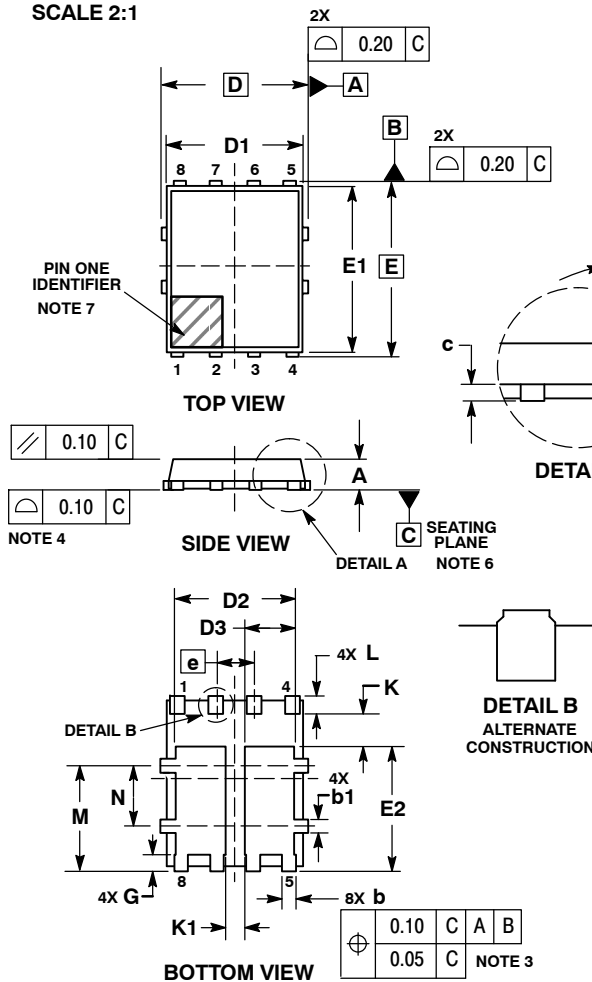
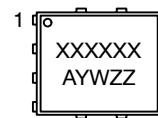**DFN8 5x6, 1.27P Dual Flag (SO8FL–Dual)**
CASE 506BT
ISSUE E

DATE 26 FEB 2013

**SCALE 2:1**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

**TOP VIEW**

PIN ONE IDENTIFIER NOTE 7

**SIDE VIEW**

NOTE 4

DETAIL A   SEATING PLANE NOTE 6

**DETAIL A**

**BOTTOM VIEW**

DETAIL B

**DETAIL B**
**ALTERNATE CONSTRUCTION**

| | 0.10 | C | A | B |
|---|---|---|---|---|
| | 0.05 | C | | NOTE 3 |

**GENERIC MARKING DIAGRAM\***

XXXXXX
AYWZZ

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | MAX | MAX |
| A | 0.90 | --- | 1.10 |
| A1 | --- | --- | 0.05 |
| b | 0.33 | 0.42 | 0.51 |
| b1 | 0.33 | 0.42 | 0.51 |
| c | 0.20 | --- | 0.33 |
| D | 5.15 BSC | | |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.90 | 4.10 | 4.30 |
| D3 | 1.50 | 1.70 | 1.90 |
| E | 6.15 BSC | | |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.90 | 4.15 | 4.40 |
| e | 1.27 BSC | | |
| G | 0.45 | 0.55 | 0.65 |
| h | --- | --- | 12 ° |
| K | 0.51 | --- | --- |
| K1 | 0.56 | --- | --- |
| L | 0.48 | 0.61 | 0.71 |
| M | 3.25 | 3.50 | 3.75 |
| N | 1.80 | 2.00 | 2.20 |

**SOLDERING FOOTPRINT\***
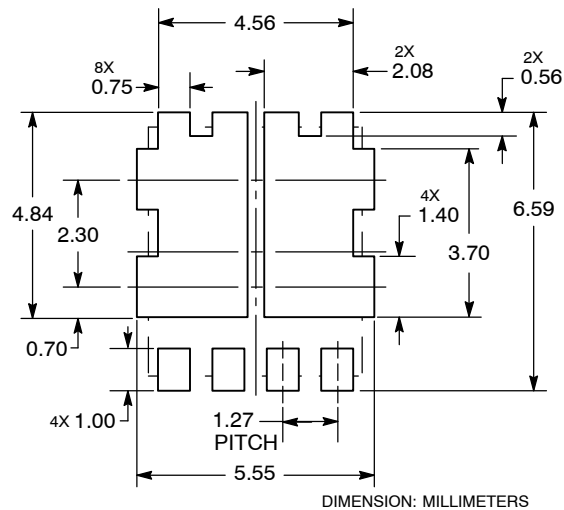
DIMENSION: MILLIMETERS

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98AON50417E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| STATUS: | ON SEMICONDUCTOR STANDARD | |
| NEW STANDARD: | | |
| DESCRIPTION: | DFN8 5X6, 1.27P DUAL FLAG (SO8FL–DUAL) | PAGE 1 OF 2 |

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION. REQ. BY M. RAMOS. | 16 APR 2010 |
| A | CORRECTED SOLDER FOOTPRINT. REQ. BY I. CAMBALIZA. | 16 FEB 2011 |
| B | CORRECTED ERROR IN SOLDER FOOTPRINT SHAPE. REQ. BY I. CAMBALIZA. | 29 JUN 2011 |
| C | CORRECTED MARKING DIAGRAM TO ADD LOT TRACEABILITY. REQ. BY J. CARTER. | 12 APR 2012 |
| D | ADDED DIMENSION K1 TO BOTTOM VIEW AND TABLE. REQ. BY D. TRUHITTE. | 11 JAN 2013 |
| E | MODIFED DIMENSIONS D1 & E1 AND ADDED NOMINAL VALUES. REQ. BY I. MARIANO. | 26 FEB 2013 |
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## PUBLICATION ORDERING INFORMATION

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# Mouser Electronics

Authorized Distributor


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